



Faculty of Engineering

Development of Rapid Alignment Polisher's Hand (RAPH) for Cross-section Polishing in Physical Failure Analysis

Handie Bin Ahmatau

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Development of Rapid Alignment Polisher's Hand (Raph) for Cross-Section Polishing in Physical Failure Analysis

Handie Bin Ahmataku

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DECLARATION

I declare that the work in this thesis was carried out in accordance with the regulations of Universiti Malaysia Sarawak. Except where due acknowledgements have been made, the work is that of the author alone. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.



.....

Signature

Name: Handie Bin Ahmatau

Matric No.: 16020092

Faculty of Engineering

Universiti Malaysia Sarawak

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ABSTRACT

X-FAB uses patented process technology to produce analog/mixed-signal ICs. As a pure-play foundry, X-FAB does not produce its own integrated circuits (ICs), instead manufacturing them using designs produced by its clients or other parties in collaboration, mostly using X-FAB's portfolio of modular, highly specialized proprietary process technologies and intellectual property (IP). Chemical Mechanical Polishing (CMP) cross-sectioning technique has been recognized for many years as failure analysis fundamental tool for examining depth-related profile of a sample. Therefore, it is a precious tool in semiconductor industry as its exclusive characteristic of providing entry into a third dimension in a two-dimension world. Process levels can be micro sectioned and capability to inspect layer-by-layer made this method crucial in gathering information on fabrication parameters and on defects. Another advantage of CMP cross-sectioning is its wide area of observation as compared to other cross-sectioning methods such as Focus Ion Beam (FIB). CMP cross-sectioning requires high skilled failure analyst and require couple of hours to complete a section of reasonable complexity of target. Typically, CMP cross-sectioning is performed in three basic steps: physical mounting, coarse grind and final polish. These three steps are time consuming particularly during coarse grind, the analyst need to realign the target before it reaches to final polish. Any technology that can reduce the polishing turnaround time is most welcomed on this day. Allied High-Tech Products. Inc. is a well-known maker of precision grinders and polishers. This research will provide a new idea of design and fabrication of the anticipated polisher fixture called Rapid Alignment Polisher Stage (RAPS), which will assist a fast, controllable, and accurate target alignment which current method is lacked off. This product is believed able to decrease the polishing turnaround time significantly.

Keywords: Physical Failure Analysis (PFA), Silicon on Insulator (SOI), Chemical Mechanical Polishing (CMP)

***Pembangunan Rapid Alignment Polisher's Hand (Raph) untuk Penggilapan Keratan
Rentas dalam Analisis Kegagalan Fizikal***

ABSTRAK

Teknik penarataan kimia dan mekanikal (CMP) telah diiktiraf selama bertahun-tahun sebagai alat analisis kegagalan asas untuk memeriksa profil kedalaman. Ia adalah alat eksklusif dalam industri semikonduktor sebagai pengukuran ke dimensi ketiga dalam dunia dua dimensi. Tahap penganalisan adalah pada skala micro sectioned dan kemampuan untuk memeriksa lapisan demi lapisan membuat kaedah ini penting dalam mengumpul parameter fabrikasi dan kecacatan. Satu lagi kelebihan CMP ialah keluasan pemerhatiann yang lebih berbanding dengan kaedah keratan rentas yang lain seperti Focus Ion Beam (FIB). Penganalisis yang mahir memerlukan beberapa jam untuk melengkapkan satu kerja keratan rentas struktur sasaran. Secara tipikal, CMP keratan rentas dilakukan dalam tiga langkah asas: pemasangan fizikal, penrataan kasar (rough polishing) dan penrataan akhir (final polishing). Langkah ini memakan masa terutama untuk penjajaran penrataan kasar. Penganalisis perlu memastikan penjajran yang tempat sebelum mencapai penrataan akhir. Teknologi yang boleh mengurangkan masa penjajaran rataaan adalah sangat diperlukan sekarang untuk meningkatkan produktiviti penrataan. Penyelidik mempunyai pengalaman selama 14 tahun menggunakan alat Allied MultiPrep TM Polishing. Allied High Tech Products. Inc. adalah pembuat terkenal dan terbaik alat penrataan (polishing machine). Penyelidikan ini akan memberikan idea baru reka bentuk dan fabrikasi satu bahagian dalam mesin penrataan yang dipanggil Rapid Alignment Polisher's Hand (RAPH). Ini justeru membantu mengurangkan masa penjajaran sasaran dengan kawalan yang cepat dan tepat disamping mengekalkan mutu penrataan keratan rentas (cross-section polishing).

Kata kunci: *Kegagalan Fizikal (PFA)l, Silikon Pada Penebat (SOI), Penrataan Kimia Mekanikal (CMP).*

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LIST OF ABBREVIATIONS

adj	Adjusted
ANOVA	Analysis of variance
BHF	Buffered Oxide Etch
BOX	Buried oxide
CDA	Compress dry air
CH ₃ COOH	Acetic Acid
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Polishing
Cu	Copper
CVD	Chemical Vapor Disposition
DI	De-ionized
DOE	Design of Experiment
DTI	Deep Trench Isolation
EBR	Edge Bead Removal
FA	Failure Analysis
FLGT	Floating gate
GOX	Gate Oxide
HF	Hydrofluoric
H ₂ O	Water
H ₂ O ₂	Hydrogen Peroxide
IBM	International Business Machine
IC	Integrated circuits
ILD	Inter-level dielectric layer

IMD	Intermetal Dielectric
IP	intellectual property
Lab	Laboratory
NCD	Nanocrystalline diamond
NHO ₃	Nitric Acid
NH ₄ OH	Ammonium Hydroxide
PFA	Physical failure analysis
PFIB	Plasma Focus Ion Beam
PI	Polyimide
RAPH	Rapid Alignment Polisher Hand
R _{cu}	Copper polishing rate
RFIC	Radio frequency integrated circuits
RIE	Reactive Ion Etching
ROI	Region of interest
R _{ox}	Oxide polishing rate
rpm	Radius per minute
SC1	Standard Clean 1
SEM	Scanning Electron Microscopy
SiO ₂	Silicon Dioxide
SOC	Systems-on-chip
SOI	Silicon on Insulator
SRAM	Random-Access Memory
stdev	Standard deviation
STI	Shallow Trench Isolation
TMAH	Tetramethylammonium hydroxide

una

Unadjusted

CHAPTER 1

INTRODUCTION

1.1 Research Background

Chemical Mechanical Polishing (CMP) is a basic approach to allow extremely flat and smooth surface be produced at several critical steps in semiconductor manufacturing process flow (Banerjee et al., 2008). International Business Machine (IBM) invented CMP in the semiconductor industry in late 80's to enable more metal layers to be included in their integrated circuits (IC) (Woodie, 2007). The idea was to perform planarization of oxide inter-level dielectric layers (ILD) by depositing metal layer and add another layer of oxide. These layers of oxides must be smooth and not wavy to enable more metal layers to be stacked in IC. Without CMP, layers stacking will follow previous material's topology. This will cause metal short if multiple metal layers are deployed in IC. CMP has been carried out by means of the special liquids containing particles of an abrasive material and alkaline chemical substances (Khmelev et al., 2006). CMP process is used to planarize ILD since last two decades and currently it is employed for tungsten contacts, vias, shallow trench isolation (STI), and for copper interconnects in dual damascene architecture (Banerjee et al., 2008). In X-Fab Sarawak Sdn. Bhd. Failure Analysis (FA) laboratory, Allied Multi-Prep Polisher machine Figure 1.1 uses CMP process to perform a physical sample de-processing. De-processing is a process to remove thin film layers which applied in the wafer fab in reverse order during physical failure analysis (PFA) (Wagner, 2001). Allied Multi-Prep Polisher machine is capable to perform sample de-processing using parallel lap and cross-section polishing techniques. Parallel lap polishing technique is employed to delayer or remove thin layers such as Nitrides, Oxides, Aluminium, and low dielectric constant materials inside the

IC. Parallel lap polishing technique also review top-down surface of layer on IC as shown in Figure 1.2. On the other hand, a cross-section technique is used to cut IC to reveal each of its layers. Layer in IC consist of oxides layers, metal layers, vias and contacts and passivation layers as shown in Figure 1.3.



Figure 1.1: Multi-prep polisher machine

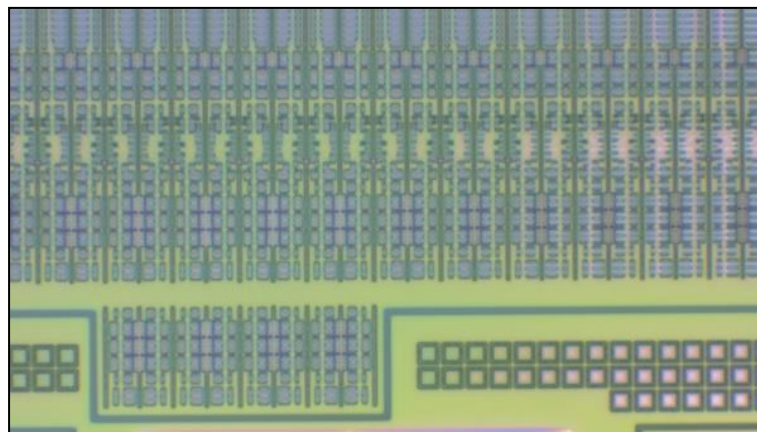


Figure 1.2: A parallel lap polishing optical image on IC surface

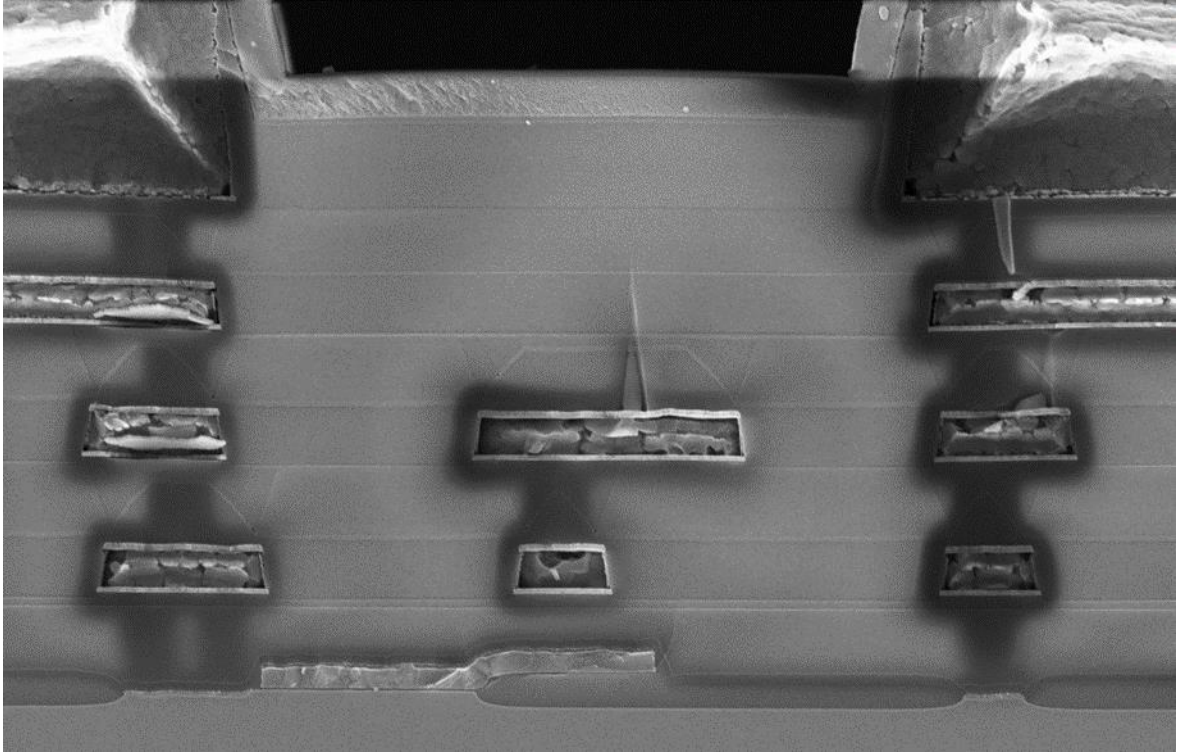


Figure 1.3: Cross-section scanning electron microscopy's image inside ic which consist of active layer, STI layer, ILD layer, intermetal dielectric (IMD) layer, metal layer and passivation layer

Both parallel lapping and cross-sectioning technique are good approach to perform PFA for new chip demand of Silicon on Insulator (SOI) wafer.

1.2 Problem Statement

The benefits of SOI technology are to reduce parasitic device capacitance, improving performance as well as smaller build area (Vandana, 2013). Current delayering method to reveal polysilicon using 49% Hydrofluoric (HF) concentration is not suitable for SOI wafer. Furthermore, the method cannot remove small, thin, and dense gate poly such as in Static Random-Access Memory (SRAM) cells. The implication of the current method will cause Top Silicon to be damaged (Ahmataku et al., 2018).

Furthermore, current cross-section polishing sample die mounting on aluminium stage and die alignment are done manually by hand using tool such as tweezers. The process is hard to control since alignment of the sample die or interest structure needs to be precise to get accurate results. Error in alignment will lead to imprecision width measurement and degrade the polishing quality. Perfect alignment is also vital to cut through structures of interest in a wide area of observation for apple-to-apple profile comparison. Thus, with the current technique, the accuracy of polishing is highly dependent on human expertise in the field.

Challenges are how to invent a new Polisher's Hand which is adjustable for obtaining a super straight cross-section polishing line which is not capable in current Polisher's Hand. The challenge is to polish a very long line approximately 1mm from Start Point to End Point.

In summary, there are three problems to be addressed:

- i. Currently, there is no solution for the delayering of SOI wafer types. Current wet etch procedure is only compatible for bulk Complementary Metal Oxide Semiconductor (CMOS) wafer types.
- ii. A polisher hand like the Rapid Alignment Polisher Hand (RAPH) which allows precision calibration of polishing straightness, granting the capability to polish relatively long structure with a very narrow width, that is, structures whose width to length ratio $W:L$ is roughly in the order of 1:1000 is still not developed.

- iii. The integration of parallel lap polishing and RAPH to solve very long Deep Trench Isolation (DTI) line in SOI technology is considered as a new challenge.

1.3 Objectives

The objectives of this research are:

- i. To investigate suitable technique for delayering of SOI wafers.
- ii. To design and fabricate a new prototype of polisher hand for cross-sectioning Long and Narrow DTI in SOI wafer with high capability and accuracy.
- iii. To evaluate the performance of the developed polisher hand compared to conventional polisher's hand.

1.4 Research Limitation

This research focuses on solution to delayer SOI wafer. The wet etching rate might vary based on acid concentration and dipping time which done manually. The parallel lap polishing rate also might vary due to different material contact, depth, slurry used, spindle rotation speed and pad used. Continuous checking under microscope is needed to ensure delayering accuracy. Physical tests are conducted on the prototype until it fits the purpose of the study. The study is limited to comparing the improvement made by RAPH as compared to conventional polisher hands.

1.5 Organization of the Thesis

This thesis divided into 5 chapters which is as follow:

- i. Chapter 1, Introduction delivers history, idea of CMP in semiconductor industry. Then the chapter describes the CMP process being used in polisher

machine in Failure Analysis laboratory at X-Fab Sarawak Sdn. Bhd. and the challenges in PFA.

- ii. Chapter 2, Literature Review highlight and describes previous and current study related to the new improvement of the delaying method and RAPH. This chapter provides required information and technology, identify challenges or problems faced. The end of this chapter, it provides conclusion of the highlights, challenges, and future improvement.
- iii. Chapter 3, Methodology, describes the flow of methodology in conducting this research. All the methodology procedures are explained in detail in this chapter.
- iv. Chapter 4, Results and Discussion deliberates the result and findings of this research. In this chapter, challenges, and solution of SOI delaying are discussed. The conceptual design, testing and performance evaluation of RAPH also included.
- v. Chapter 5, Conclusion accomplished the results and findings of this research. The recommendation for the future RAPH improvements also describes in this chapter.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

The literature review gathers information related to chemical-mechanical polishing, CMP as used in the semiconductor industry and its mechanisms from previous and current studies. Further down the scope of CMP in the semiconductor industry, the literature review delves further down into CMP-based failure analysis in the field of Physical Failure Analysis, PFA.

This literature review chapter is divided into two parts. The first part gives an overview of CMP methods with the intention of delayering SOI wafers. The second part focuses on current machine or fixtures that assist in polishing straightness calibration.

2.2 CMP in General

In the realm of physical failure analysis, PFA, much data has been collected regarding polisher machines which are widely used in Failure Analysis laboratories to do sample de-processing analyses such as delayering and cross-sectioning. Delayering and cross-sectioning are crucial CMP techniques in PFA, and they are interrelated.

Before discussing the need for CMP in failure analysis, the application of CMP in fabrication will be reviewed. CMP is used in the fabrication side of the semiconductor industry as a method of planarization or flattening of wafers (Shen et al., 2015). The only current global planarization method that is truly efficient is chemical mechanical polishing (Zhao et al., 2020). In the context of fabrication, CMP helps in high-throughput removal of materials from the wafer while also eliminating topographical defects from etching and filling

processes, such as Chemical Vapor Deposition (CVD) and diffusion. Achieving a nano-scale smooth surface can be accomplished using CMP (Lu et al., 2020). However, the use of CMP in fabrication also leaves some degree of non-uniform thickness, usually in the range of tens of nanometres, which leads to decrease in yields as feature dimensions are continually shrunk down (Shen et al., 2015).

The need for CMP in the delayering and cross-sectioning of wafer samples will be discussed in this section. According to (Chen et al., 2016), chemical polishing alone can achieve high surface accuracy and low surface damage, but at the cost of low material removal efficiency and poor surface uniformity. On the other hand, mechanical polishing alone can achieve good surface uniformity and high grinding efficiency, but at the cost of surface damage. (Chen et al., 2016) then proposes the method of chemical-mechanical polishing, a micro-fabrication technique which as the name implies combines chemical and physical polishing methods into one process, to utilize the advantages of these two polishing techniques and minimize their disadvantages.

According to (Rajan et al., 1997), CMP specifically removes material from the wafer substrate through a combination of structural degradation of the substrate surface via slurry chemistry and physical removal of material via abrasion from slurry particles. In addition, the mechanism by which material is removed from the substrate is a function of surface roughness and the wear rate of the surface being polished (Liu et al., 2019). Besides physical abrasion, another important point in CMP performance is the useful lifetime of the slurry used during polishing. For example, newly applied slurry is more effective in CMP than recirculated and reused slurry, due to pH and ionic concentration changes during the recirculation of the slurry which in turn is caused by chemical dissolution of the surface during CMP (Rajan et al., 1997).

The action of slurry particles on the wafer surface layer is illustrated in the following Figure 2.1(a). The higher pressure will cause more abrasive particle contact area as depicted in Figure 2.1 (b).

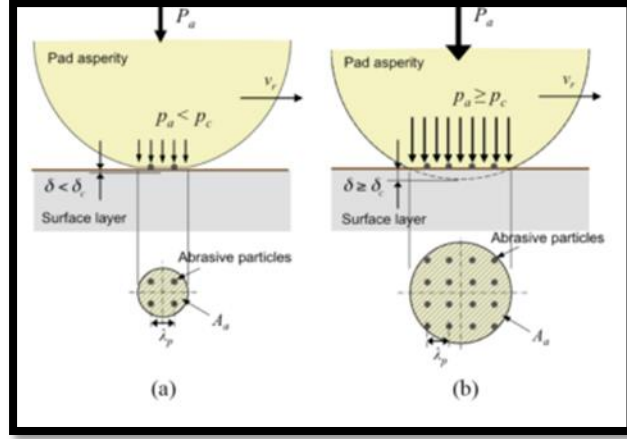


Figure 2.1: Low and high-pressure particle (Kim et al., 2014)

The increase the amount of particle contact with the increased amount of pressure will then increase the surface plowing by the abrasive particles as shown in Figure 2.2. Volumetric material removal rate by particle, $dVr, a/dt$, can be written as

$$\frac{dVr, a}{dt} = \frac{Aa}{\lambda^2} \frac{dVr, p}{dt} \quad \text{Equation 2.1}$$

A relation between removal rate per particle and the asperity contact pressure is derived then the volumetric material removal rate due to a single sliding particle that has radius Ra , Young's modulus Ea , and hardness Ha is derived as a function of the approach distance, δ .

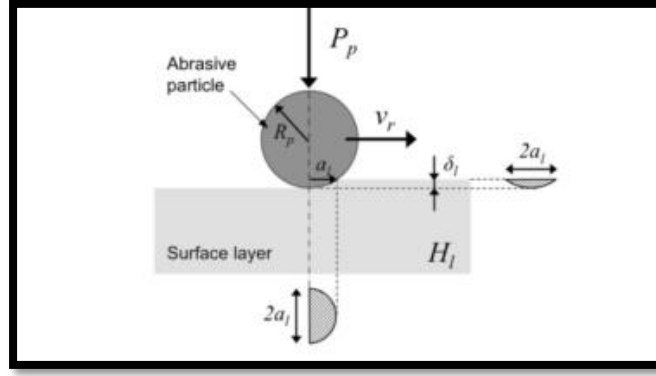


Figure 2.2: Surface layer plowing by abrasive particle (Kim et al., 2014)

Figure 2.3 shows a development of particle contact as the pressure increases. (a) At low contact pressure ($P_a < P_c$). (b) At critical contact pressure ($P_a = P_c$). (c) At high contact pressure ($P_a > P_c$). Thus, the normal load on particle, P_p , written as

$$P_p = \frac{1}{2} \pi a_l^2 H_l \quad \text{Equation 2.2}$$

Where the influences of chemical reactions are reflected in the effective hardness of the surface layer, H_l .

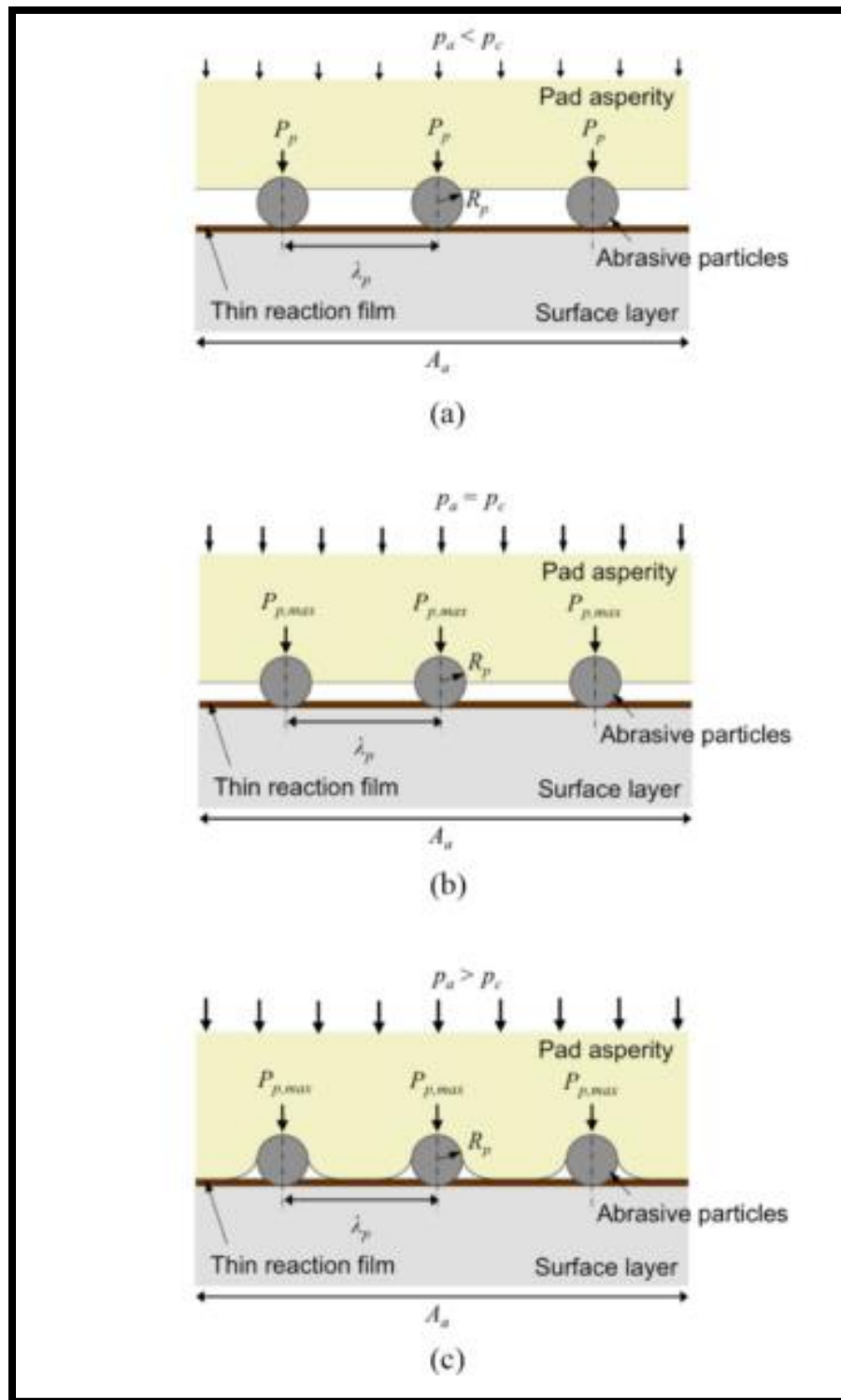


Figure 2.3: Development of particle contact with increased pressure (Kim et al., 2014)

One implementation of the CMP technique is the rotary-type CMP system. As described by (Zhao et al., 2013), the rotary-type CMP system consists of a polishing plate, wafer carrier, pad conditioner, and a slurry delivery mechanism. The plate and the wafer carrier rotate in the same axial direction while at the same time the carrier moves along the radial direction of the plate. During CMP, a rotating wafer sample is held against the rotating plate that is in turn padded with a polymer polishing pad. The carrier applies polishing pressure to the back of the wafer to press the wafer to the pad, while a slurry containing chemicals and nanometer-scale particulates is injected on top of the padded plate. The combination of the chemicals in the slurry and abrasion from the nanoparticles removes micromaterials and results in a smooth planarized wafer surface or edge (Zhao et al., 2013). A basic diagram illustrating the usual rotary-type CMP setup is shown in Figure 2.4.

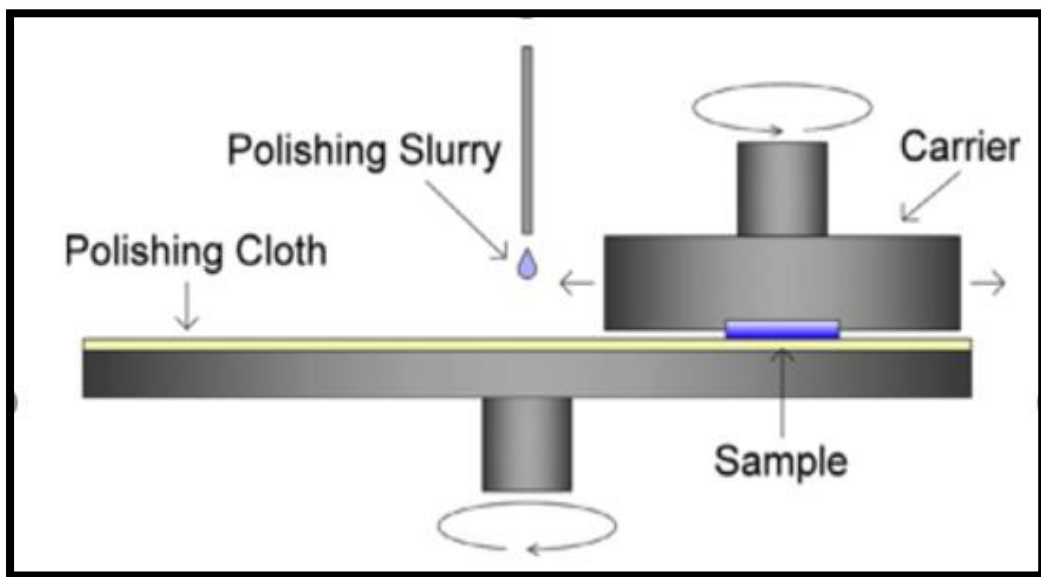


Figure 2.4: Rotary-type CMP tool schematic. schematic diagram of CMP tool

Sample held in rotating carrier and swept across counter rotating polishing cloth.
Slurry distributed continually onto top of polishing cloth (Zhao et al., 2012)

2.3 CMP Challenges in the Semiconductor Industry

The application of CMP to failure analysis and semiconductor production is not without issues of its own. As detailed by (Kawaguchi et al., 2014), CMP polishing uses a polymer polishing pad to perform the actions of grooving and hole processing to ensure uniform planarization. The usage of the polishing pad in this manner however means that over time the pad gets worn out. When the polishing pad is worn out, slurry will not adhere to the pad as efficiently as it does when it is new, due to the holes and grooves on the polishing pad being clogged with the particulate matter from the slurry. When this worn pad is used to polish the substrate wafers, it will result in irregular planarization of the substrate. For this reason, a polisher pad that has been used in several thousand polishing jobs is discarded, which poses a burden to costs and waste management (Kawaguchi et al., 2014). Problems specific to CMP cross-sectioning and parallel lapping will be touched upon in the next two sections, followed by researchers' solutions to these problems.

2.4 CMP Cross-Sectioning, Parallel Lapping Methods, Techniques, and Steps

CMP is most often used in the manufacturing side of the semiconductor industry as a method of planarizing wafer surfaces prior to further processes in chip manufacture. However, another common use of CMP is in the cross-sectioning of the edges of wafer samples in failure analysis laboratory settings, for example with the objective of exposing a certain structure on the chip for observation & analysis with electron microscopy systems. This section will focus on the methods used in CMP cross-sectioning and Parallel Lapping.

In the Failure Analysis Laboratory at the X-FAB Kuching, the CMP cross-sectioning of wafer edges is done using the Allied Multi-Prep Polisher machine, as shown in Figure

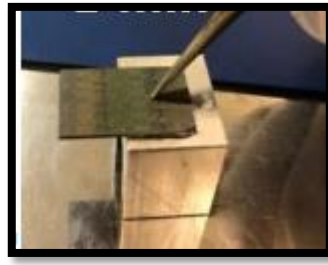
2.5(a). This machine requires both a polisher film attached to the top of the platen and a soft felt pad attached to the platen to perform a complete wafer edge cross-sectioning job. The typical steps in the cross-sectioning of a wafer sample based on the standard operating procedures of the FA laboratory will be discussed in Section 2.4.1 to 2.4.3.



(a)



(b)



(c)

Figure 2.5: (a) Allied multi-prep polisher machine. (b) A polisher which capable to do cross-section polishing and parallel lap polishing. (c) Polisher's arm equipped with precision stylus to measure sample feeds (Allied High Tech, 2021)

2.4.1 CMP Cross-sectioning Methods, Techniques, and Steps

1. The area on the wafer in which the failure analysis work is to be done is marked with a marker pen or a felt tip pen, but not directly on the feature to be analyzed, rather around it.
2. The wafer is manually cleaved, first broken up into small pieces on tabletop, then further cleaved using the auto-cleaver machine.
3. The cleaved wafer sample is mounted on a flat polisher stage as shown in Figure 2.5 (c), using hot paraffin wax as the adhesive. The wafer is adjusted so that it is as perpendicular as possible.
4. Before placing the polisher stage to the machine, the first platen is attached to the lower spindle of the machine, Figure 2.6 (a), then a 30-micrometre grade polishing film is applied to the top of the platen as shown in Figure 2.6 (b).

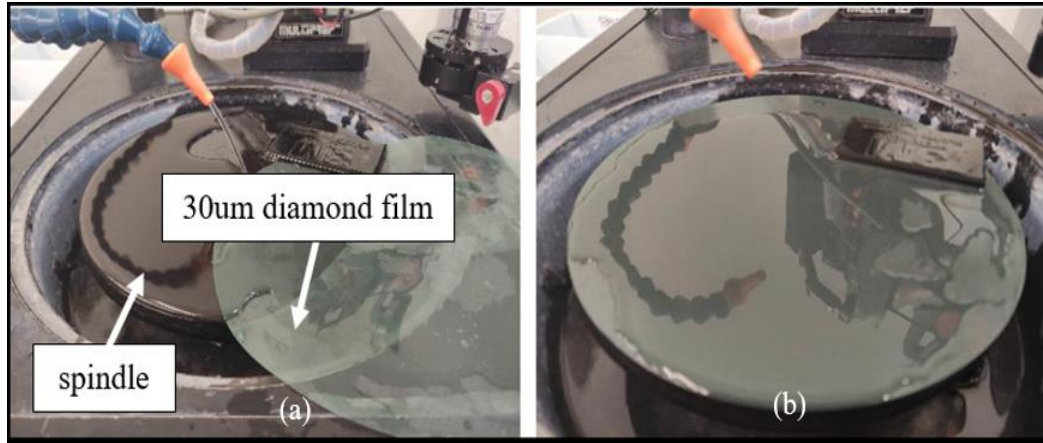


Figure 2.6: Attaching 30μm diamond film onto spindle

5. The polisher stage with the wafer sample attached on it is then mounted onto the polisher hand of the machine as shown in Figure 2.7.

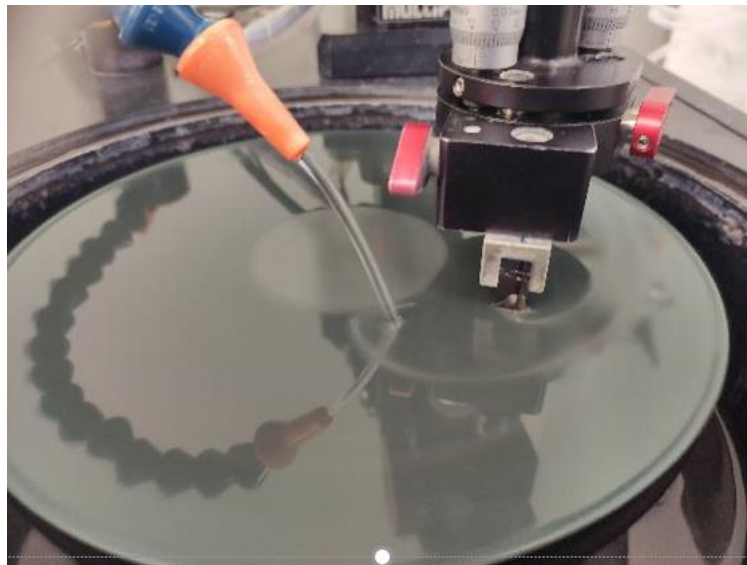


Figure 2.7: Sample mounting for cross-sectioning

6. The polisher machine lower spindle motor is started, then the upper spindle of the machine arm is slowly lowered into the polishing film until contact is made and abrasion starts.

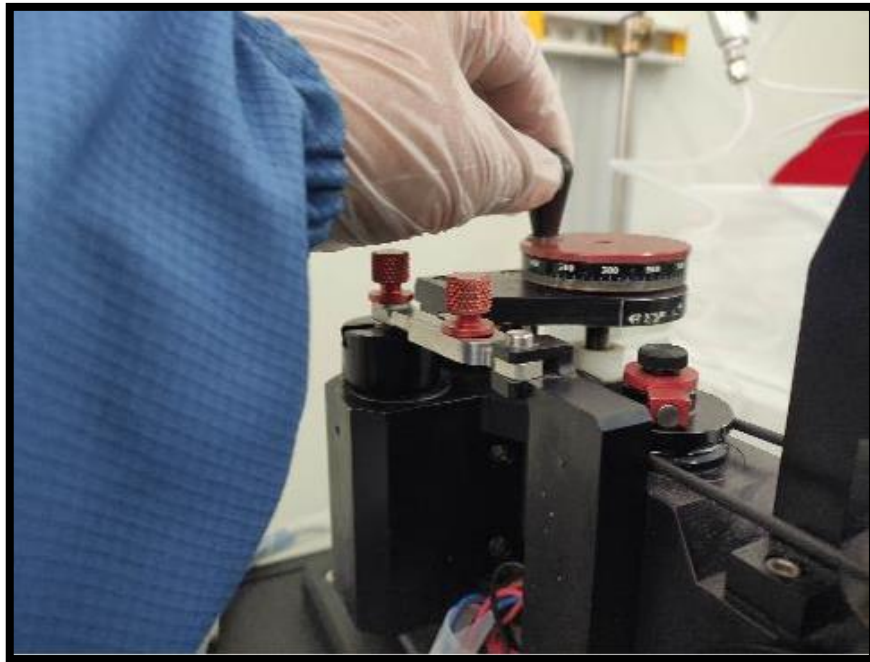


Figure 2.8: Sample feeding by lowering polisher arm.

7. The upper spindle is lowered until the wafer sample is cross-sectioned close to the target structure, in the coarse cross-sectioning of the wafer edge as shown in Figure 2.8.
8. Once the target structure is close, the upper spindle is raised, and the lower spindle motor is stopped.
9. The 30-micron polisher pad on the platen is replaced with polisher pads of progressively smaller grades, and the cross-section polishing steps are repeated, this time as the fine cross-sectioning steps. For example, from 30 to 9 μm diamond film grain. The diamond different colour is indicating the grain size. 30 μm the colour is green, and 9 μm is pinkish shown in Figure 2.9.

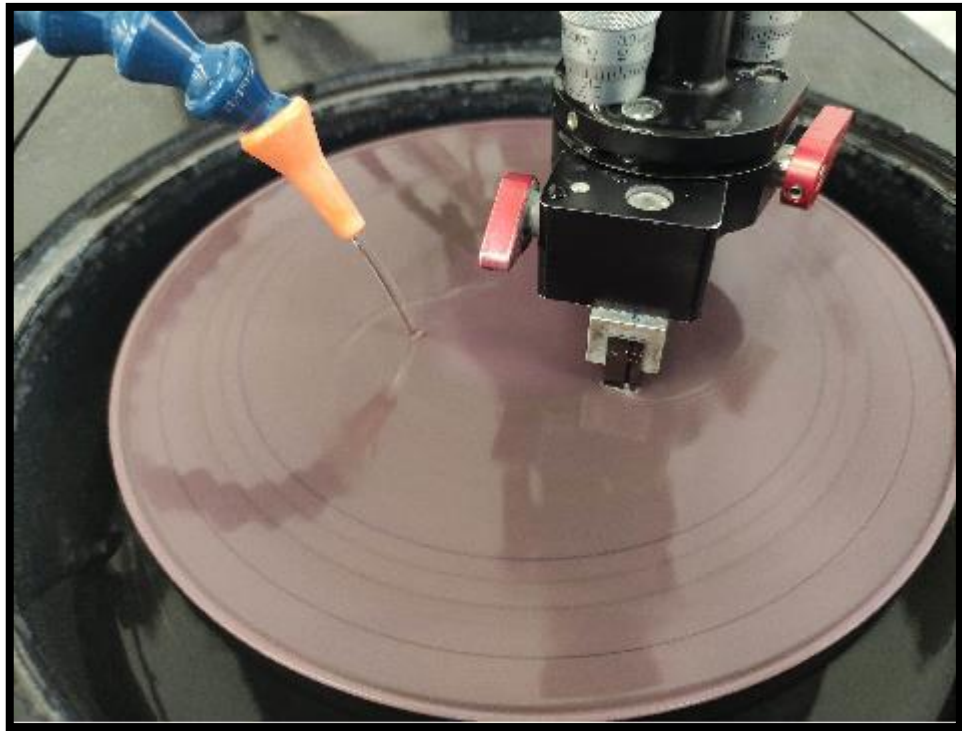


Figure 2.9: 9 μ m diamond film

10. Once the smallest grade polishing pad has been used, the platen is replaced with a second platen, this time with soft pelt covering on top of it.
11. The lower spindle motor is once again started up, and before the upper spindle is lowered, nanoparticle-loaded slurry is applied to the spinning platen.
12. The upper spindle is then lowered until the wafer edge barely touches the soft red polishing pad. While the spindle is rotating, Colloidal Silica slurry is added for final polishing as shown in Figure 2.10 (a). The Colloidal Silica blue diamond slurry size is 0.01 μ m stored in a bottle shown in Figure 2.10 (b).

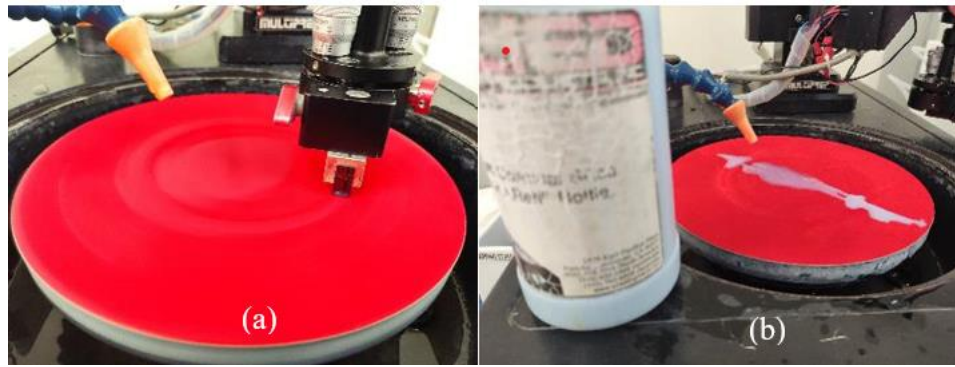


Figure 2.10: Final red polishing pad is used with 0.01µm colloidal silica slurry.

13. Once the CMP step is done, the upper spindle is raised, and the lower spindle is stopped.

2.4.2 CMP Parallel Lapping Methods, Techniques, and Steps

1. First, calibrate the polisher machine such that the lapping surface is parallel to the polishing disc using Mitutoyo lapping micrometers as shown in Figure 2.11.

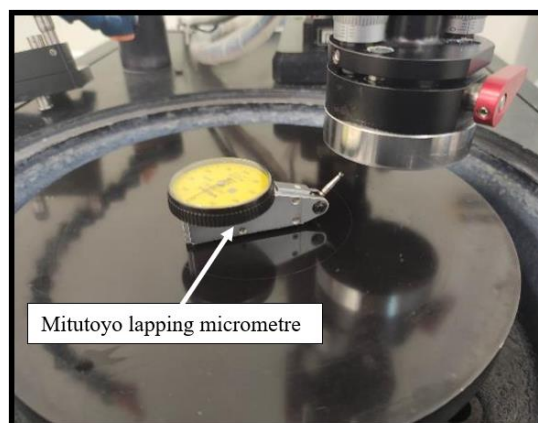


Figure 2.11: Dial test indicator, horizontal type 0.2mm, 0.002mm, 8mm stem calibration

2. Attach the wafer sample to a lapping stage using double-sided tape, then press the wafer-side of the lapping stage on a padded polishing disc to ensure the wafer sample adheres to the stage as shown in Figure 2.12.

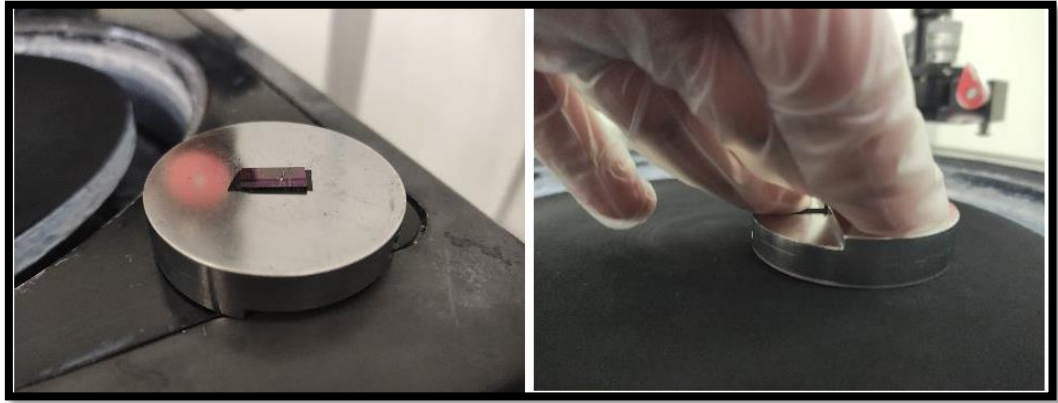


Figure 2.12: Parallel lapping sample padded on polishing disc

3. Attach the lapping stage to the polisher hand as shown in Figure 2.13.

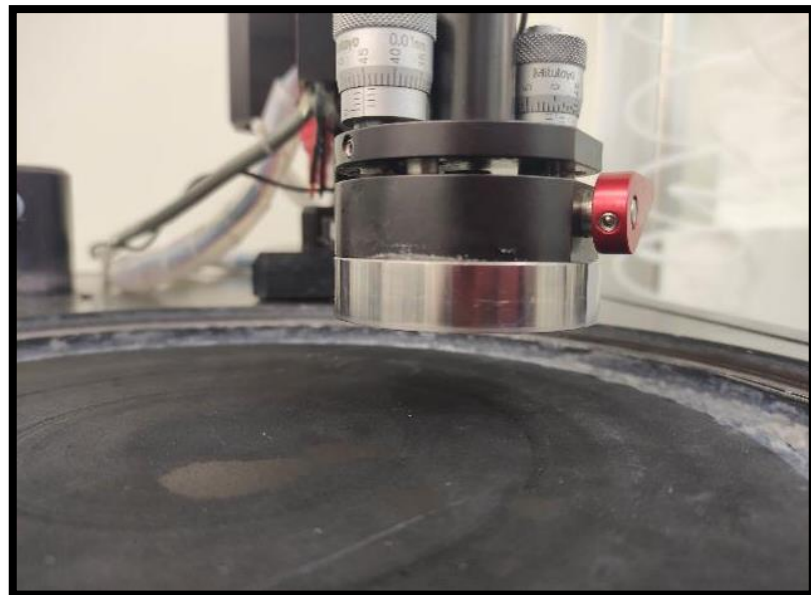


Figure 2.13: Parallel lapping sample mounted on fixture

4. Attach a padded disc to the lower spindle, then squirt a line of colloidal silica suspension on the disc as shown in Figure 2.14.



Figure 2.14: Parallel lapping pad with colloidal silica suspension slurry

5. Turn on the polisher machine and start spinning. Then slowly lower the upper spindle parallel fixture until its surface contacts the lapping pad as shown in Figure 2.15.
6. Let the lapping process proceed until it reaches the target.

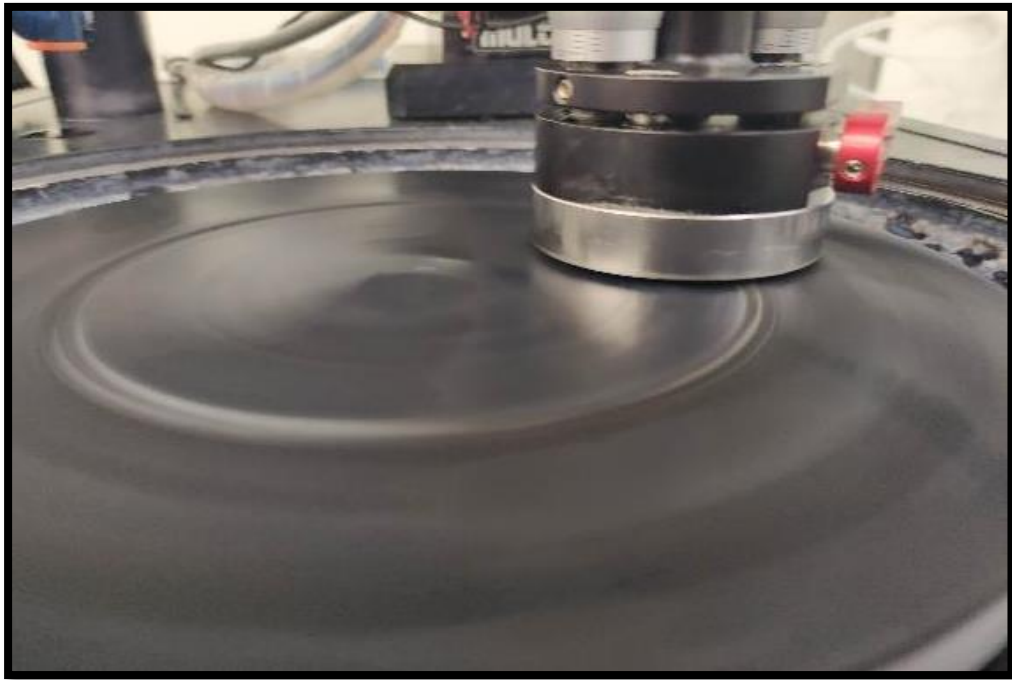


Figure 2.15: Parallel lapping pad contacts with upper spindle with fixture attached

7. When lapping is done, raise the upper spindle then remove the lapping stage from the polisher hand. Then, the sample target under optical microscope is checked as shown in Figure 2.16.

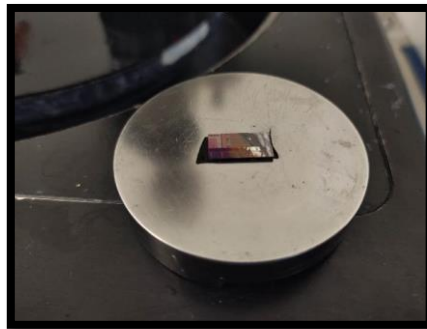


Figure 2.16: Checking the sample target under optical microscope

Certain layer gives different colour under optical microscope. For instance, when reach polysilicon layer, the structure looks pinkish. This is one of the indicators for when we should stop polishing. The other indicator is to look at the dial. The dial stylus gives the amount of sample feeding in millimetres.

2.4.3 Chemical Mechanical Polishing application in semiconductor industry.

To planarize various types of surfaces, CMP parallel lapping is used for efficient planarization. This section will touch on various CMP parallel lapping methodologies. One example by (Thomas et al., 2014) touches upon the planarization of a wafer surface that contains nanocrystalline diamond (NCD) as shown in Figure 2.17. In their study, the problem was that the NCD rough surface evolves with its thickness. The objective of their study then was to polish this NCD film using CMP to remove film roughness which evolves with film thickness.

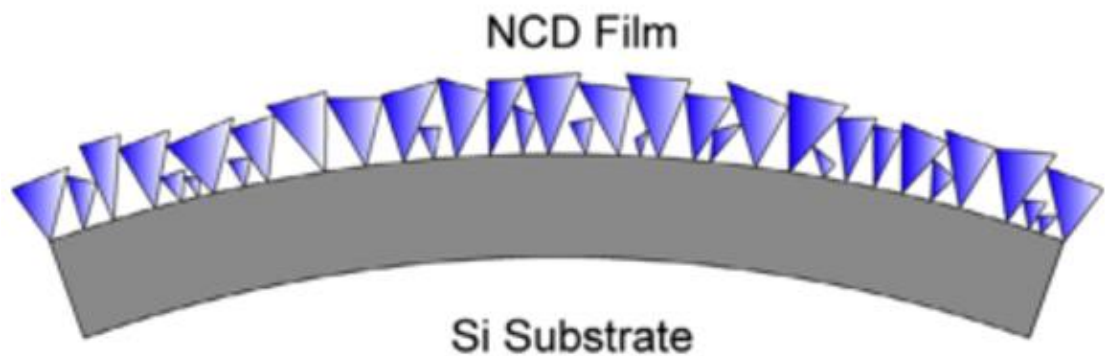


Figure 2.17: Nanocrystalline diamond film surface to be polished with CMP.

Schematic of exaggerated wafer bow seen with NCD films. Due to the differing coefficients of thermal expansion of diamond and silicon, upon cooling from growth temperatures significant bowing will occur (Thomas et al., 2014).

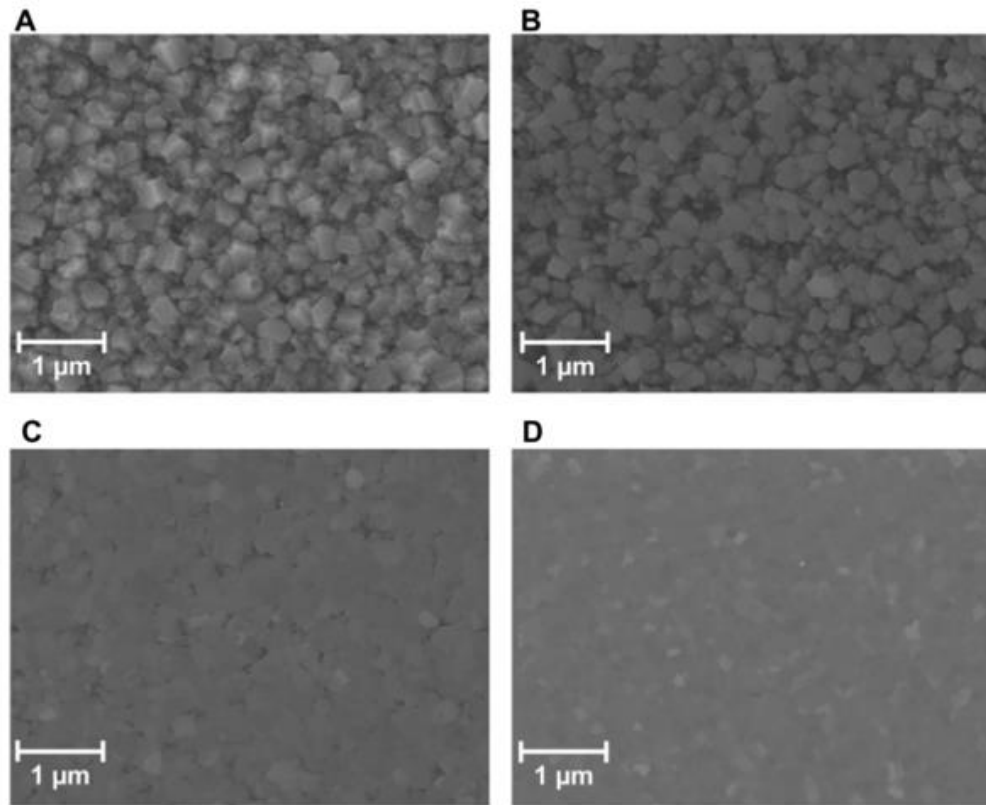


Figure 2.18: CMP smoothness on NCD film. SEM micrographs of as grown and polished films. CMP was used on three different films for the indicated amount of time under identical conditions. (A) As grown, (B) 1 h CMP film, (C) 2 h, and (D) 4 h. (Thomas et al., 2014)

To polish this film, the CMP method is used, specifically with a Logitech Tribo CMP tool equipped with a polyurethane polishing cloth and an alkaline colloidal silica fluid.

By using the CMP method, (Thomas et al., 2014) were able to smoothen the NCD film, such that the root-mean-square roughness value is reduced from 18.3 nm to 1.7 nm over a surface area of 25 μm^2 as shown in Figure 2.18. In general, the main problem with planarization of wafer surfaces lies in particle abrasion distribution. According to (Zhao et al., 2013), in rotary-type CMP, a greater distribution of particle abrasion occurs at the edge of the wafer surface, which leads to uneven wafer surface polishing, since this causes the

polishing rate at the wafer edge to be greater. To solve this, the team proposes using kinematic analysis to find out the particle trajectories in rotary-type CMP machines. Their statistical calculations of the trajectory density give a quantitative description of the particle trajectory distribution. By assuming that the particles are embedded in the rotary pad and that the velocity at the centre of the wafer is uniform, (Zhao et al., 2013) optimized the parameters of speed ratio and period ratio to get the best uniformity of polish between the centre and edge of the wafer surface.

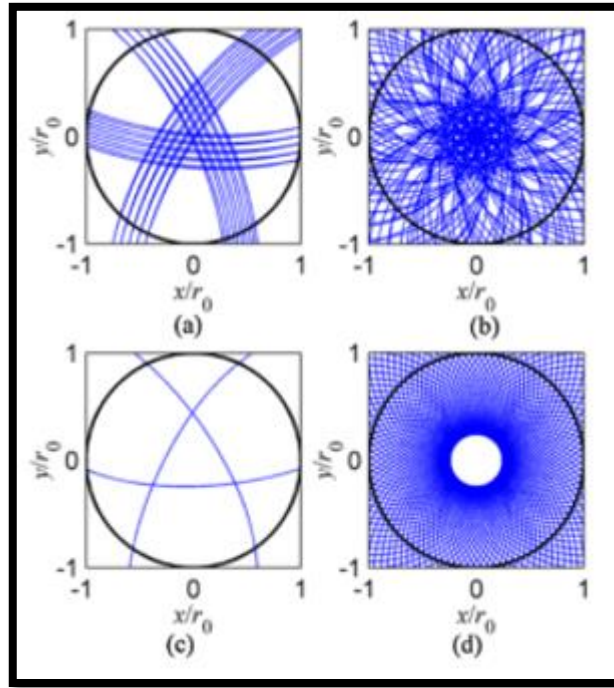


Figure 2.19: Kinematic trajectory analysis results. Single particle sliding trajectory at different kinematic conditions, particle position $R=180\text{mm}$, polishing time $t= 60\text{ s}$; (a) $\alpha=2/3$, $kro=10$; (b) $\alpha=0.97$, $kro= 10$; (c) $\alpha = 1$; (d) $\alpha = 0.97$, $kro = 1$. (Zhao et al., 2013)

The resulting kinematic analysis for rotary-type CMP shows that trajectory distributions are significantly affected by speed ratio and period ratio as shown in Figure 2.19. Trajectory density is higher at wafer edge than wafer center. Based on the experiment, a range of speed ratio from 0.91~0.93 and period ratio 5~7 is preferred to obtain better polishing uniformity.

Next is the parallel lapping of wafers containing copper (Cu). As is usual, planarization at extreme wafer edge is harder as compared to center, and in the case of Cu loaded wafers, is due to increased Cu density, layer density and pattern density. To reduce the failure rate at edge of wafer, dual wafer polishers that are suitable for Cu plating and lithography was employed (Lin et al., 2014) as shown in Figure 2.20.

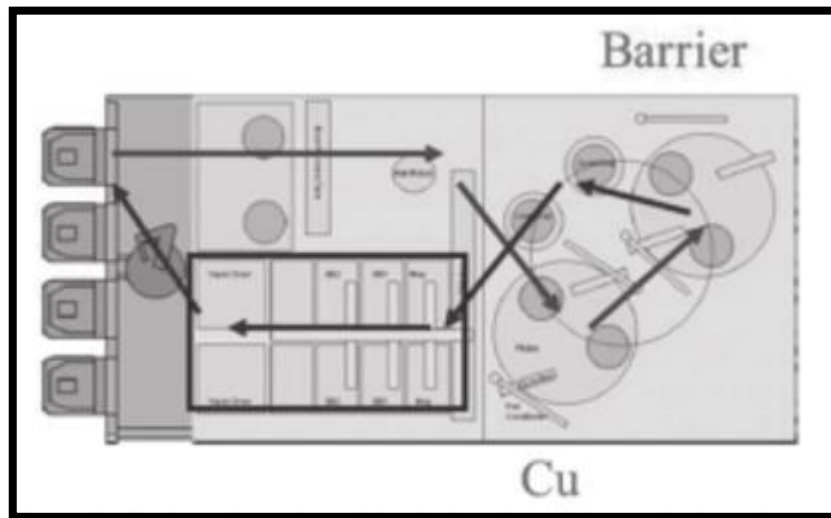


Figure 2.20: Dual wafer polisher setup

The tool configuration of the dual wafer polisher and robust Cu-CMP process (AMAT reflection GT) (Lin et al., 2014)

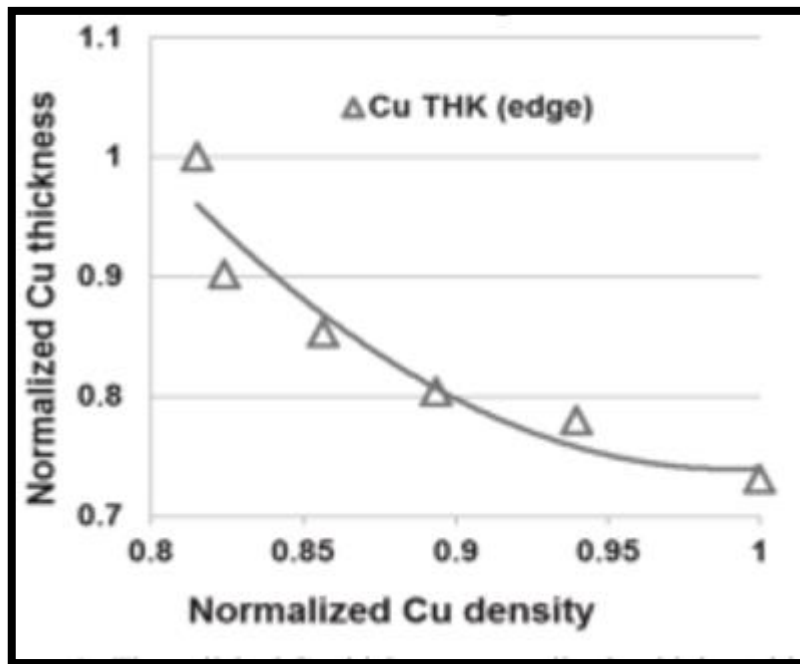


Figure 2.21: Polished Cu thickness normalized to highest thickness vs Cu density normalized to highest density (Lin et al., 2014)

Figure 2.21 shows Cu density and thickness are inversely related. The theory is that thinner polished Cu pads were produced as a result of the Copper (Cu) density increasing via layers.

The team successfully reduced these metrology issues by reducing the Edge Bead Removal (EBR) distance of Cu plating and photoresist coating, as well as optimizing the Cu/ULK selectivity of barrier slurry at the Cu-CMP.

2.5 Etchant to remove Polysilicon

The removal polysilicon structure, a floating gate (FLGT) using tetramethylammonium hydroxide (TMAH), and hydrofluoric (HF) solution shown in Figure 2.22, Figure 2.23 and Figure 2.24.

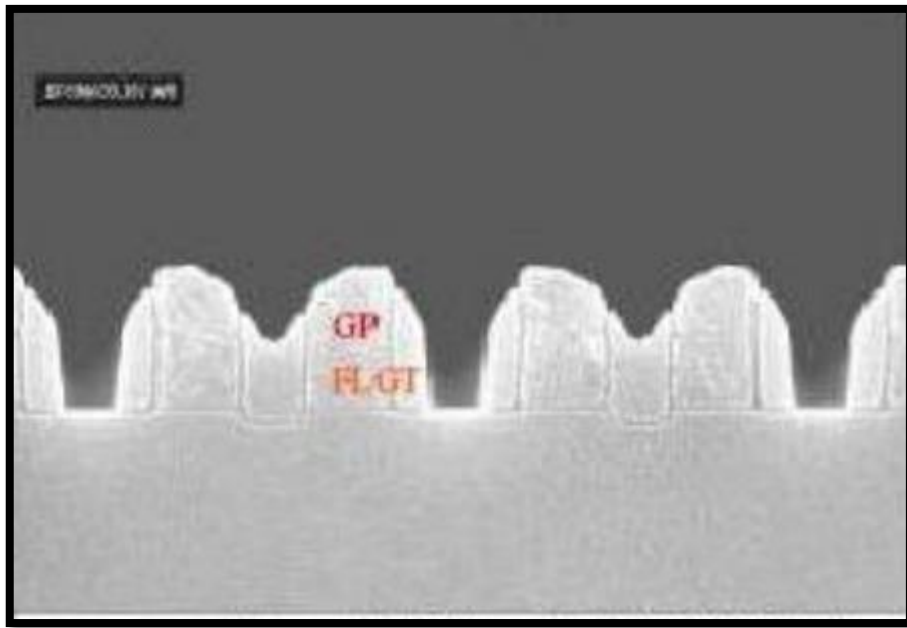


Figure 2.22: Memory structure (Scanning Electron Microscopy cross-section view) (Wong and Fong, 2006)

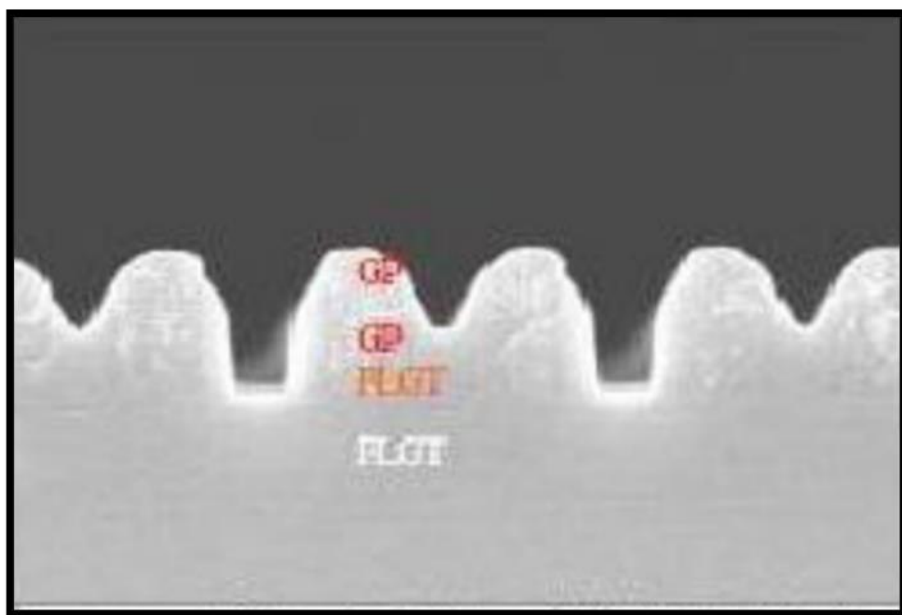


Figure 2.23: Post TMAH in scanning electron microscopy (SEM) cross-section image view (Wong and Fong, 2006)

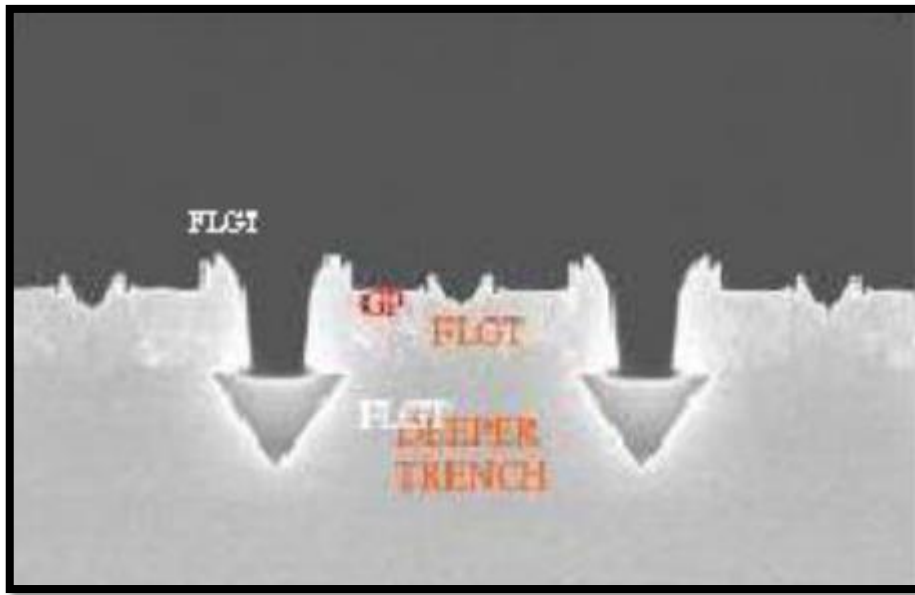


Figure 2.24: Post HF → TMAH (scanning electron microscopy cross-section view) (Wong and Fong , 2006)

(C Koh et al., 2004) also introduced a method to remove bulk polysilicon was developed in Chartered Failure Analysis Laboratory. The procedure consists of only three steps, firstly HF (49%) de-processing for about 3 minutes (varying with different devices), then secondly using SC1 rinse at temperature of 50⁰C and thirdly followed by polysilicon etch (20HN03:8CH3COOH: 1HF) for 8 seconds, the bulk polysilicon can be removed easily and expose the defect under the polysilicon.

The indicator whether etching is reaching polysilicon is by looking at poly capacitor colour under microscope as shown in Figure 2.24, Figure 2.25, Figure 2.26, Figure 2.27, Figure 2.28 and 2.29. When reach bulk polysilicon, poly capacitor looks pinkish in colour. Total removal of polysilicon shows poly capacitor colour changed from pinkish to white as shown in Figure 2.31 (Ahmataku et al., 2018).

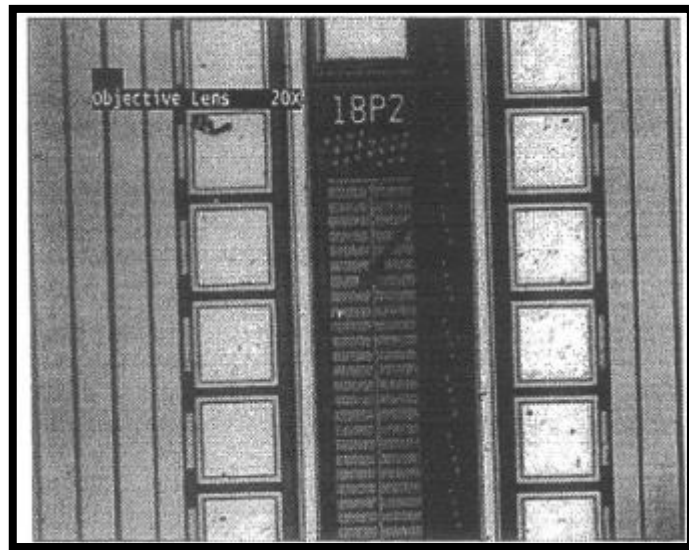


Figure 2.25: Defect localization using emission microscope.

The hot spot was found at failing P-bulk capacitor structure (C. K. Oh et al., 2004)

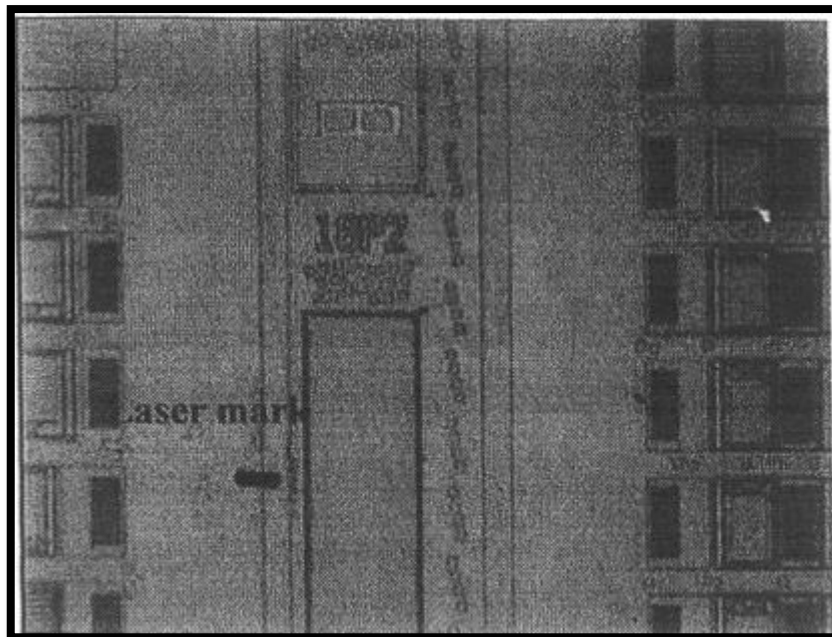


Figure 2.26: Optical micrograph of capacitor structure after HF DI. Poly capacitor looks pinkish colour (C. K. Oh et al., 2004)

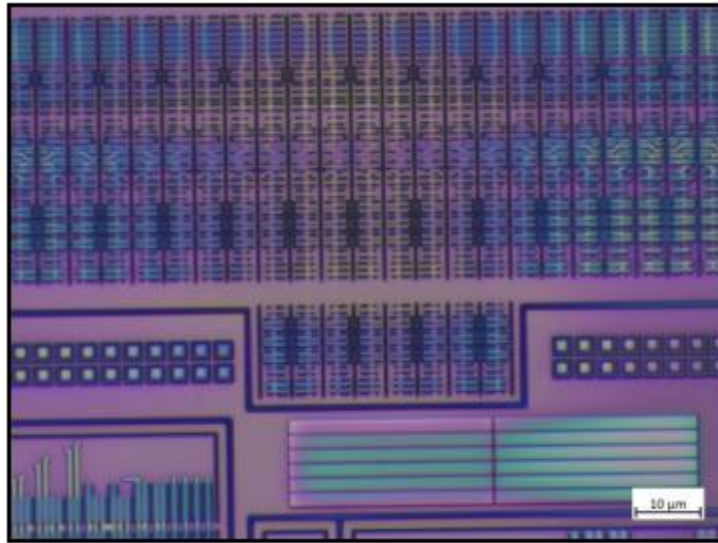


Figure 2.27: Optical micrograph of capacitor structure after SC1 dip. Poly capacitor looks colour changed from pinkish to white (Ahmataku et al., 2018)

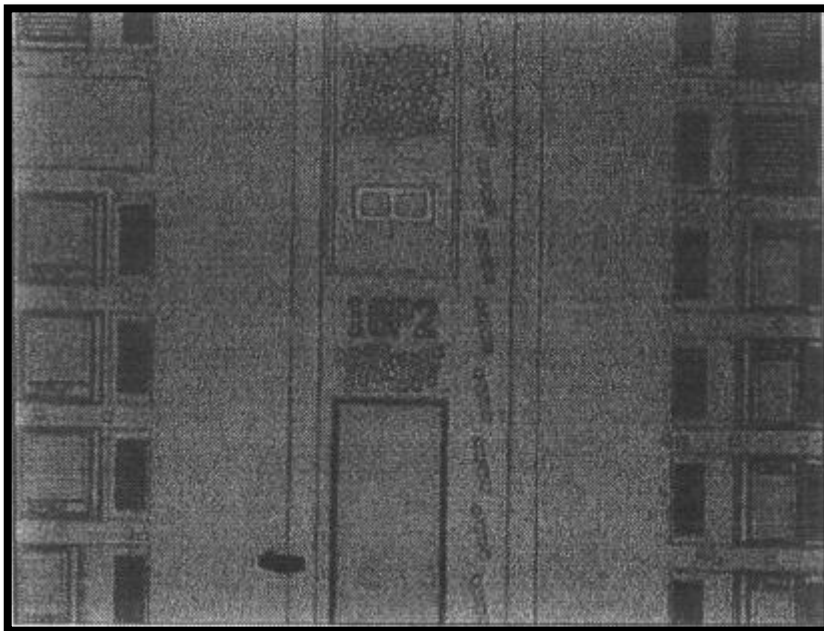


Figure 2.28: Optical micrograph of capacitor structure after SC1 dip. Poly capacitor looks pinkish color (C. K. Oh et al., 2004)

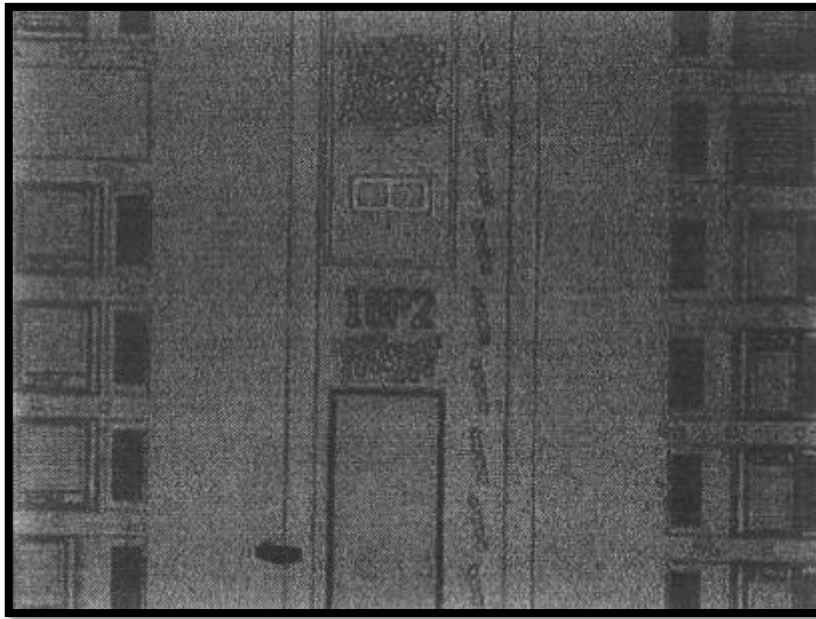


Figure 2.29: Optical micrograph of capacitor structure after SC1 dip. Poly capacitor looks colour changed from pinkish to white (Ahmataku et al., 2018)

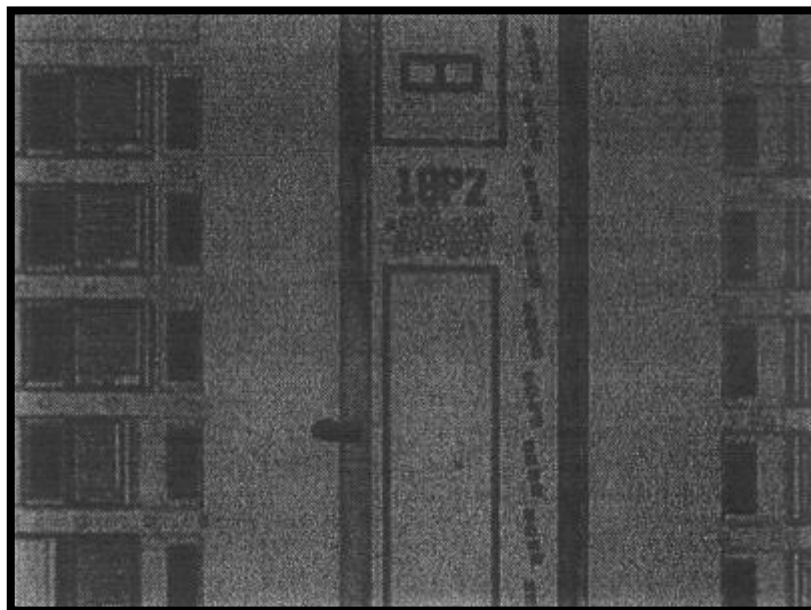


Figure 2.30: Optical micrograph of capacitor structure after Polysilicon etch. Poly capacitor looks white colour indicating disappearance of polysilicon (Oh et al., 2004)

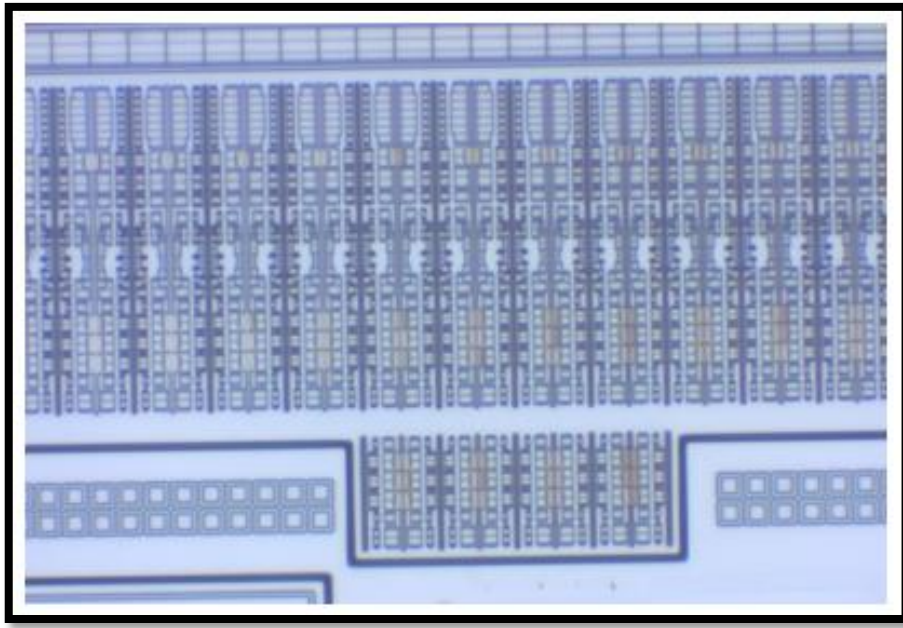


Figure 2.31: An optical image after removing ILD Oxide layer using 20% HF concentration for 10 minutes. Polysilicon layer (Ahmataku et al., 2018)

(Wong and Fong, 2006) and (C. K. Oh et al., 2004) also shows it is possible to remove polysilicon using both TMAH + HF and also HF alone with the concentration of 49% for 10 minutes as shown in Figure 2.30. Both papers suggest using HF to remove remaining oxide layer after the remove of polysilicon.

2.6 Etchant to Remove Oxide

(Ma et al., 2013) investigated the CMP process being difficult to control, with the speed, pressure, and slurry flow rate affects wafer surface topography severity. In this study, it was also noted that dishing and erosion of wafer surface features occur at different pattern density, and that there exists a slurry selectivity on material. This last bit is important, for it forms the basis for their experimental objective, namely, to study the influence of slurry selectivity on pattern effects for Cu interconnect CMP. The team used three different slurries

in the CMP process for different selectivity, for P1, P2 and P3 stages. Figure 2.33 shown the surface topography after three CMP stages.

Table 2.1: Slurries used in different stages of CMP process (Ma et al., 2013)

Process stage	Process condition I	Process condition II
P1	Only R_{Cu} related	Only R_{Cu} related
P2	Slurry with higher R_{Cu}	Slurry with higher R_{Cu}
P3	Slurry with higher R_{Cu}	Slurry with higher R_{ox}

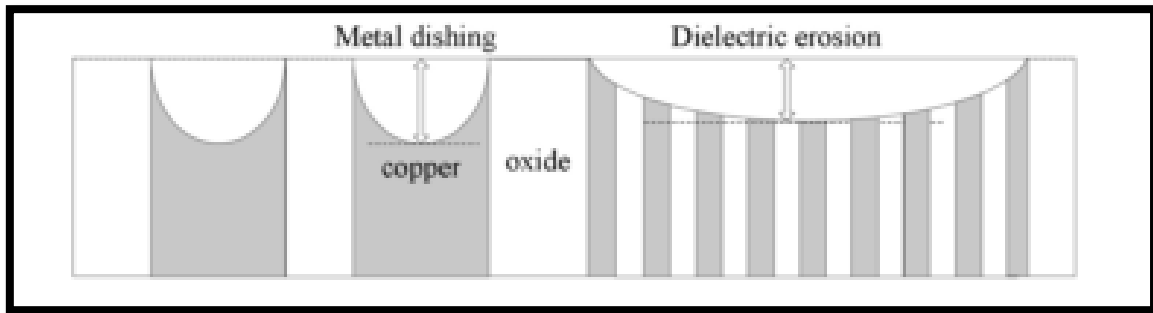


Figure 2.32: Metal dishing and dielectric erosion (Ma et al., 2013)

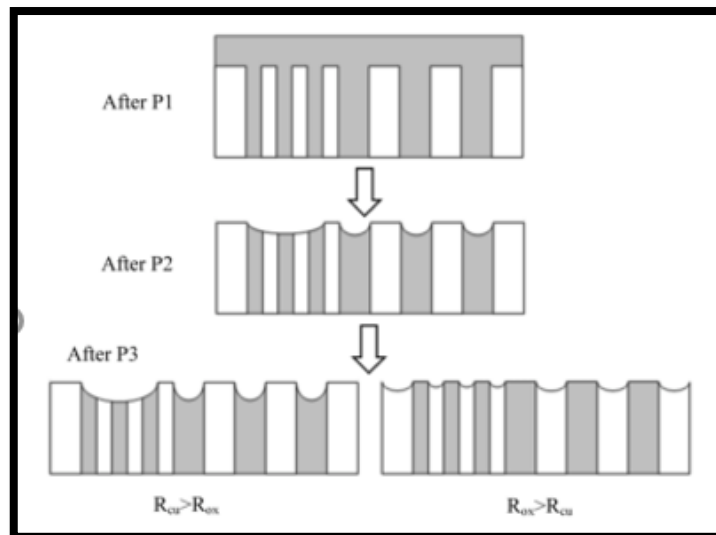


Figure 2.33: Surface topography after three CMP stages (Ma et al., 2013)

There may be two different slurry types in P3 (Ma et al., 2013).

In the P1 stage, the bulk copper is removed, in P2 copper and barriers are removed, and in P3 the barrier and oxides are removed. Note from the Table 2.1 that in the stage where the oxides are removed, the slurry used has higher R_{Cu} (Copper polishing rate) and R_{Ox} (Oxide polishing rate) In short, the best etchant for oxides is an etchant with high oxide selectivity.

2.7 Silicon-On-Insulator, SOI

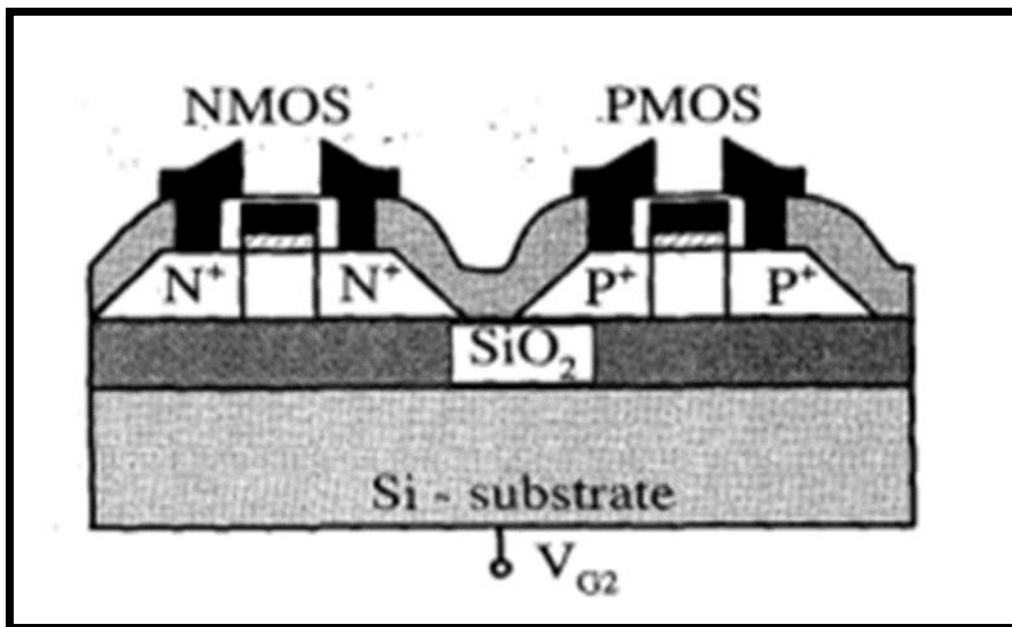


Figure 2.34: Topology of SOI MOSFETS (Cristoloveanu, 1998)

The focus of the CMP technologies and methodologies described here is on the polishing of Silicon-on-insulator, SOI wafers. SOI is a chip-making technology in which bulk silicon wafers that are usually about 0.75 mm thick are replaced with three-layered wafers; the first is a thin surface layer of silicon where the actual transistors are fabricated, the second is the titular insulating layer made of silicon dioxide, SiO_2 , and referred to as the buried oxide (BOX), and the third is a supporting silicon layer. Besides silicon dioxide,

another choice of material for the insulating layer is sapphire, which has been in use since 1970, but has since been largely superseded by Silicon Dioxide (SiO₂). Noto et al. (2014) Figure 2.34 shows the topology of SOI MOSFETS.

2.7.1 Advantages of SOI over Bulk Silicon

The SOI technology has several advantages compared to conventional bulk silicon substrates. First is allowing for more compact devices. According to (Cristoloveanu, 1998), the lateral isolation of devices on an SOI substrate as shown in the Figure 2.32 allows for more compact designs and technologies than it is possible in conventional bulk silicon.

Second is the ability to prevent latch-ups. According to Vivian Ma (n.d.), SOI reduces the capacitance at source and drain junctions by preventing the depletion regions from extending into the substrate due to being suppressed by the insulator layer, which in turn reduces RC delay due to parasitic capacitance. This results in SOI CMOS devices having higher speed performance compared to bulk devices, particularly at low power supply voltages.

Third, SOI has the advantage of offering high resistivity values. According to (Raskin, 2014), SOI substrates offer resistivity values higher than 1 k Ω -cm, which makes it attractive for use in SOC technologies, RFIC, and mixed signal applications. To make high performance radio-frequency circuits, it is necessary to use SOI substrates, as introducing high resistivity silicon into bulk silicon MOSFETs will result in unwanted latch-up. The BOX layer in the SOI substrate isolates the top silicon from the bottom silicon substrate, allowing the top layer to be modified to increase its resistivity without impacting the IC performance.

Fourth is energy efficiency. According to (Adan et. al., 1998), CMOS devices implemented on SOI substrates has their power consumption reduced to one-fifths of that of bulk silicon CMOS, while the speed performance of SOI CMOS is generally one generation ahead of bulk silicon CMOS. Owing to the suppressed back bias effect and the possibility to reduce V_{th} due to the abrupt subthreshold characteristic, SOI MOSFETs can operate at a lower supply voltage than bulk silicon CMOS operating at the same speed. SOI technology is thus ideal for low-voltage, low-power, high-performance devices.

2.7.2 SOI Challenges in PFA Technique in Laboratory

Because SOI technology is built differently than Bulk CMOS, new difficulties in PFA arise (Z. G. Song, 2016). The Buried Oxide (BOX) layer that is present between the "handle wafer" and the top silicon and is connected to DTI oxide makes the removal of polysilicon more difficult. The DTI trench oxide is now being etched by the same chemical that is expected to be used to etch GOX. The worst-case situation is that etching could potentially penetrate further into the BOX layer, releasing the Top Silicon attachment from the BOX surface. As a result, during the supersonic clean, the Top Silicon plate will peel off, causing a loss of important data that is necessary to identify the physical reason of the failure (Ahmataku et al., 2018).

Therefore, only BulkCMOS wafers can be used to remove all layers, including polysilicon, utilising wet etch delayering using, for example, 49%HF. Since HF will etch ILD oxide all the way down to BOX and leave Top Silicon unconnected, this approach cannot be utilised with SOI wafers. Therefore, resulting Top Silicon structures to be damaged, crack and unclean (Misra et al., 2002). This problem will not happen in BulkCMOS wafer since structure builds on bulk silicon wafer (Ahmataku et al., 2018).

The CMP is the only process which can delayer and at the same time do planarization on a global scale (Lane et al., 2012). A comparable delayering and planarization technique called parallel lapping as explained in Section 2.4.2 is employed in PFA.

2.8 Machines or Fixtures that used Calibration in Failure Analysis Laboratory.

Table 2.2 shows variety of polishing machines that commonly used in failure analysis laboratory. All of them are not have features that supporting a cross-section straightness calibration. This is the motivation to design and fabricate RAPH fixture that allow cross-section straightness or angular calibration.

Table 2.2: Polishing tool's model and features.

Manufacturer	Model Name	Features
Allied Hi Tech Products Inc.	MultiPrep 8" PRECISION POLISHING SYSTEMS	Digital dial indicator measures sample thickness in 1-micron increments. Parallel Pyrex mounting surface enables preparation of several samples simultaneously. Hands-free operation. Sample stops grinding when desired point is reached. No angle adjustments are necessary during the polishing procedure
Pace Technologies	NANO-2000S	NANO-2000S double wheel grinder polisher bench top polisher for 8 and/or 10-inch wheels
Pace Technologies	NANO-1000S	NANO-1000S single wheel grinder polisher bench top polisher for 8 and/or 10-inch wheels
Pace Technologies	NANO-1200T	12 or 14-inch Single Wheel, Bench Top Grinder/Polishers NANO-1200T single wheel grinder polisher bench top polisher for 12 and/or 14-inch wheels
Pace Technologies	250 Pro	The models 250 and 250 Pro are designed for 8" or 10" diameter platens and sample diameters up to 40 mm.
JH Technologies	Automet 300	The Automet 300 accommodates 10" or 12" platens and sample diameters up to 50 mm
Ultra Tec Manufacturing, Inc.	ULTRAPOL BASIC	- Cost-effective manual polisher - High Torque mechanism - In-built coolant system - Can be used with manual tools

	MANUAL LAPPING & POLISHING MACHINE	• Upgradeable with Long Arm Positioner • High Quality Build
Ultra Tec Manufacturing, Inc.	ULTRAPOL End & Edge Polisher	• Fully Angle adjustable – produces specific wedge angles for parallel lapping only. • Quick Release Interface allow for fast and repeatable mounting and demounting. • Holders available for most components • Fast process times
Taiwan Nakazawa Co., Ltd.	TNP-1020FR-A3/A5, TNP-1025FR-A3/A5, TNP-2020FR-A3/A5, TNP-2025FR-A3/A5	• Metallographic samples and tools can be placed to keep the desktop fresh and avoid laboratory clutter
Taiwan Nakazawa Co., Ltd.	TNP-1020FR /TNP-1025FR/ TNP-2020FR /TNP-2025FR	• Manual Metallographic Grinding & Polishing Machine
HANSUN Corporation	UNIPOL-1210	• stepless speed regulation, digital display rotation, easy to operate. • beautiful appearance, smooth operation, low noise.

Figure 2.35 shows Ultra Pol end and edge polisher fixture for parallel lap. There's no fixture that design to control the straightness cross-section polishing.



Figure 2.35: ULTRA POL End and edge polisher fixture for parallel lapping only (Ultra Tec Manufacturing, 2020)

Allied has more variety of fixture for parallel and cross-section polishing. However, none of them are designed to assist the straightness polishing for cross-sectioning as shown in Figure 2.36.

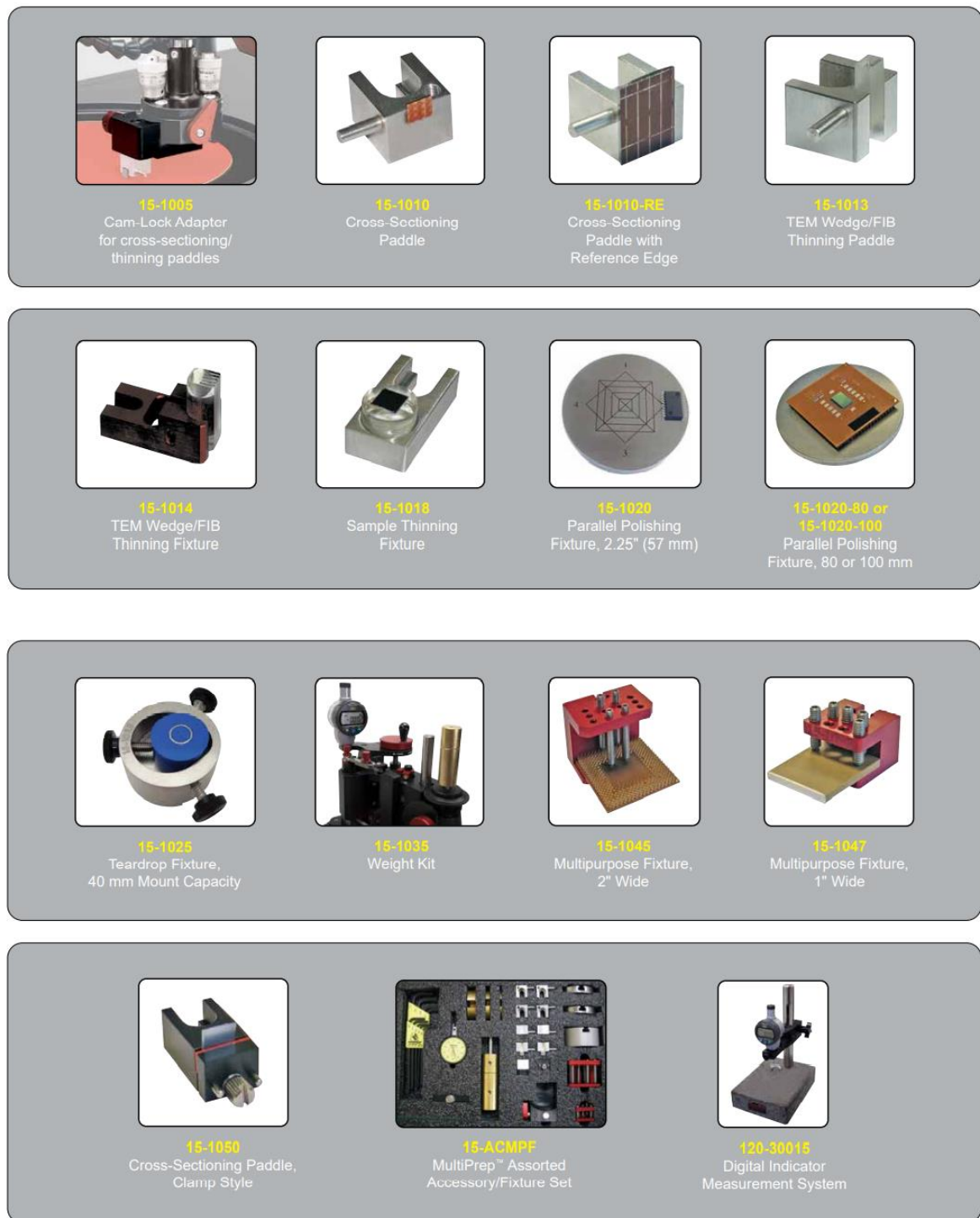


Figure 2.36: Allied multi-prep polisher fixture cross-section and parallel lapping (Allied High Tech, 2021)

Most of manufactured that produce laboratory polishing machine focused on parallel lapping fixtures. Few manufacturers like Allied Inc. and Ultra Tec Manufacturing, Inc had produced

fixtures also for cross-section polishing like shown in Figure 2.35 and Figure 2.36. However, these cross-sectioning fixtures still do not help in assisting straightness or angular calibration like RAPH does.

2.9 Summary

Although there is an advanced method for PFA delayering such as using PFIB or Laser milling, CMP machine still relevantly used in FA laboratory. In the other hand, CMP method is still widely used in semiconductor industry as a method of planarization or flattening of wafers. Currently, CMP is the only method to efficiently do the wide scale of planarization of wafer. The combination of CMP method, wet and dry etch in FA lab will open the window of more advancement in delayering method. Example of wet etch is used acid etchant to remove oxide layer. Even though CMP advantages, this method also has its weakness such as worn out of polishing pad. In FA lab, CMP method used are parallel lapping and cross-sectioning. Whenever the polishing pad is worn out, it will be replaced with a new one. This is to ensure good polishing quality of sample surface. SOI technology is deployed in semiconductor industry because it allows more compact devices, giving higher speed performance at low power supply voltages, offers high resistivity value, and energy efficient. From the literature review, there is no fixture of polishing machine in the market that can assist in polishing straightness calibration. Therefore, this is the main motivation to develop RAPH to perform cross-sectioning for long and narrow structure like DTI in SOI wafer with high capability and accuracy.

CHAPTER 3

RESEARCH METHODOLOGY

3.1 Overview

This chapter is divided into three main parts. The first part focuses on pre-processing; a method to delayer using a parallel lap polishing combined with wet etching technique. This delayering technique is to remove layer on a die to allow visibility on region ROI or target underneath that layer to perform further cross-section polishing analysis.

The second part presents improvement in a cross-section polishing method by inventing RAPH. The RAPH graphical models: fabrication materials, prototype's experimental and performance evaluation were presented and explained.

Finally, the chapter will also explain on the performance evaluation measurement employed for SOI wafer pre-processing performance and RAPH cross-sectioning performance.

3.2 Project Plan

The reason for using parallel lap polishing instead of wet etching alone is that this technique allows wide planarization of various material on a wafer (Luo et al., 2013) or a die. CMP process in parallel lapping offers a smooth and even die surface, which allows precise wet etching method to be carried out later (Liechty et al., 2005). Another benefit of parallel lap polishing is to uncover ROI or targets which are previously not visible under optical microscopes. This visibility is crucial when the target is relatively small and limited, for instance tiny defects. With random cross-section polishing, the tiny defects are easily

missed or over polished. Therefore, a precise cross-section polishing is required to reveal under layer targets or defects.

Flow chart of RAPH research methodology is shown in Figure 3.1.

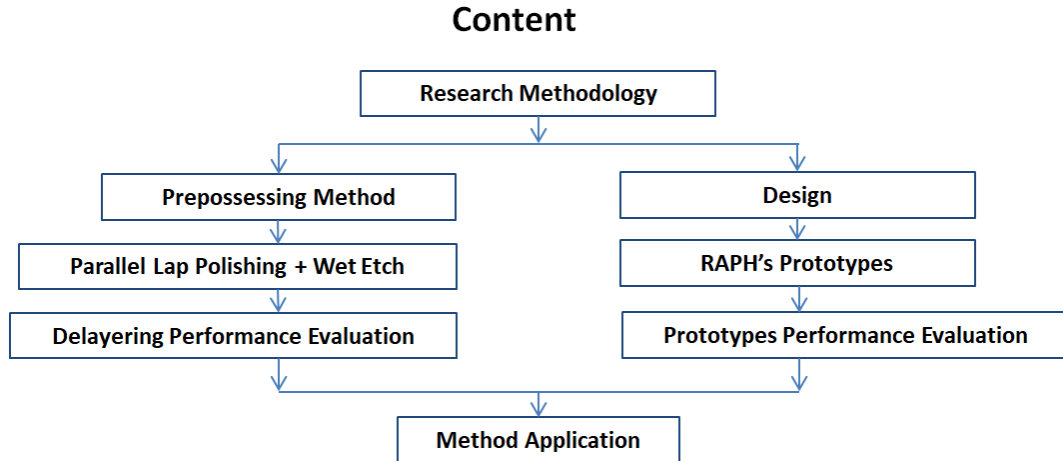


Figure 3.1: Overall research methodology flow chart

3.3 Research Methodology Flow

Pre-processing is a method to remove layer on a die to allow visibility on ROI or target underneath that layer to perform further cross-section polishing analysis. For Bulk CMOS wafer delayering, proposed to use 49% HF + SC1 Solution + Poly Etchant Solution. While for SOI wafer delayering, parallel lapping combined with wet etch delayering are required. The experiment's objectives are to investigate suitable technique for delayering of CMOS and SOI wafers.

The proposed experimental procedures are illustrated in Figure 3.2. Two experiments designed are i) to perform assessment of Bulk CMOS wafer front-end delayering method into SOI wafer. ii) to employ CMP technique or known as parallel lapping to improve surface uniformity. Then, need to find an effective spot between HF concentrations and etching rate.

The optimal HF concentration and etching time effectively remove oxides, detach the gate poly, and preserve the top silicon at the same time.

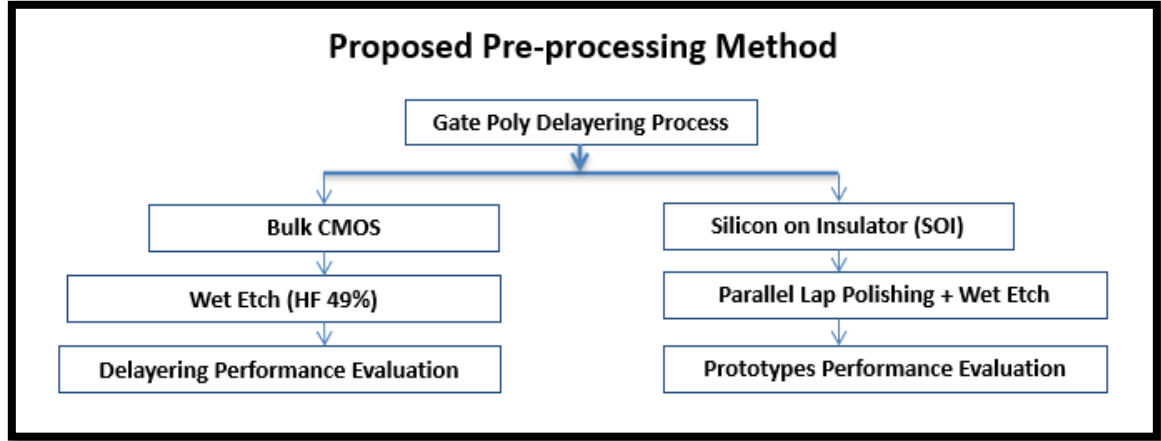


Figure 3.2: Proposed pre-processing experimentation.

3.3.1 Delayer Sample Preparation

A full processed die sample size of 20mm x 20mm is prepared by using manual cleaving method as shown in Figure 3.3. An optical microscope was employed to distinguish reaching different layer in full processed sample. For an example, when polysilicon layer is exposed, it will look pinkish.

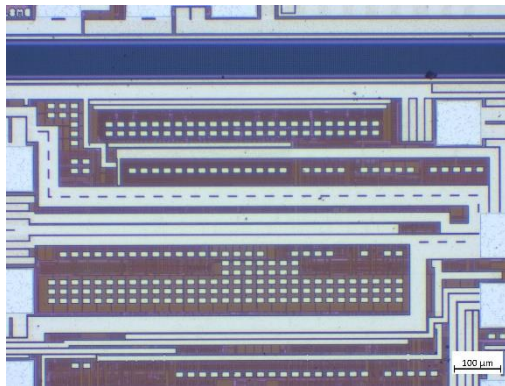


Figure 3.3: Full process die

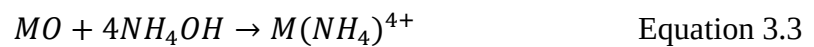
3.3.2 Assessment of Bulk CMOS Delayering Method

A small, thin, and dense gate polysilicon such as in SRAM cells was selected as the experiment sample. As shown in Figure 3.4, a full process of die sample was dipped in HF with concentration of 49% for 2 minutes to expose polysilicon.



Figure 3.4: The gate poly delayering process

Gate poly delayering process in Bulk CMOS is shown in Figure 3.4. The method can be considered as the fastest way to remove all stacked layers of Intermetallic Dielectric (IMD). High concentrations of HF acid (49%) is commonly used in this process. This works best when top metal line is exposed to the HF wet etching. Before applying the high concentration of HF, RIE was employed to remove the passivation layer such as PI. This front-end Bulk CMOS delayering technique works for wide poly such as P-bulk capacitors. An optical microscope was employed to distinguish polysilicon layer. After that, the sample was immersed into SC1 solution (1NH₄OH:1H₂O₂:5H₂O) for 3 minutes at temperature of 50°C. The reason for using SC1 solution is to remove organic compound and metallic particles. The samples were then cleaned with acetone. The chemical reactions are shown in Equation 3.3:



Next, poly-etchant solution was employed to etch polysilicon layer. The polysilicon etch solution was derived by Equation 3.4

$$20HNO_3:8CH_3COOH:1HF \quad \text{Equation 3.4}$$

3.3.3 Proposed Pre-Processing Delayering of SOI Wafer

The existing bulk CMOS techniques are unable to remove thin and dense polysilicon on SOI Wafer. Thus, a few trial-and-error experimentations need to be conducted to investigate the best technique to achieve this objective.

Parallel lapping is used to improve surface flatness while exposing the polysilicon layer. Subsequently, Poly-etchant is employed to etch the exposed polysilicon and remaining the oxides. An optimal HF concentration and etching time is crucial to etch the remaining oxides while protecting the top silicon from damage during SOI delayering process. A clean active silicon surface is vital for wet etchant solution to be carried out successfully to reveal silicon defects. The flowchart in Figure 3.5 shows the proposed experimental process of the delayering gate poly with parallel lapping method.

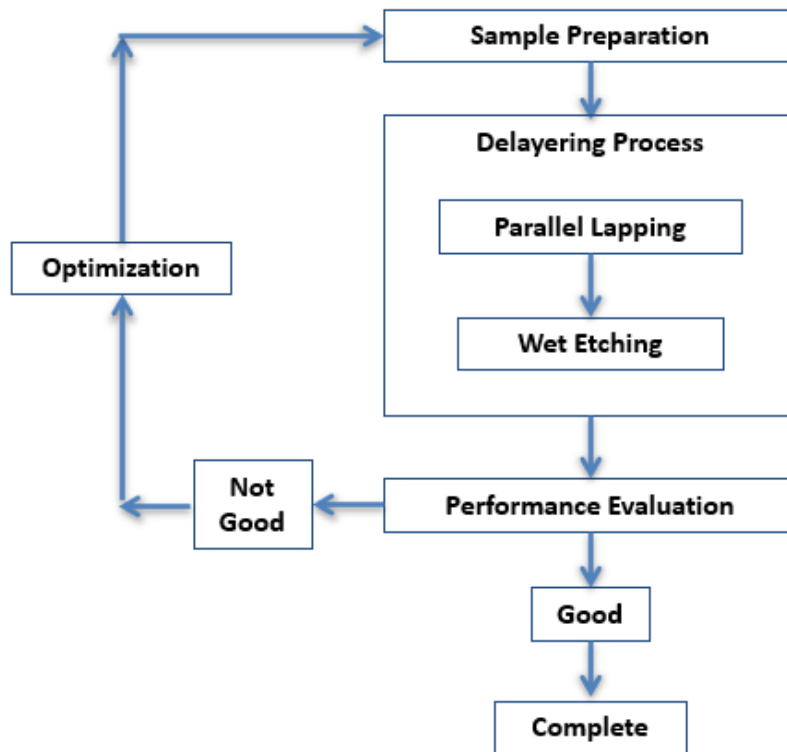


Figure 3.5: The gate poly delayering process flow chart

3.3.4 Parallel Lap Polishing

The parallel lap polishing is a CMP process. It was carried out using Allied Multi-Prep Polisher machine as shown in Figure 3.6. A parallel lap polishing fixture was used by sticking a die onto parallel lap fixture. The sticking method using double sided tap is shown in Figure 3.7 and Figure 3.8.

A cotton swap is used, and a small amount of pressure is applied on to the sample surface to ensure the sample is firmly stick onto the parallel lap fixture as shown in Figure 3.9.

Beside the double-sided tape, wax also can be employed to stick the die onto the fixture as shown in Figure 3.10. However, before applying the wax, it needs to be melted.

The parallel lap fixture must first be heated on the heater. The idle heater temperature is 100⁰ C for about 7 minutes. Next, cotton swab is applied to spread the melted wax on parallel lap fixture as shown in Figure 3.11. Finally, tweezers are employed to put and adjust the sample on to parallel lap fixture. Ensure to put the sample in between center and edge of parallel lap fixture as shown in Figure 3.12. This is to ensure even lapping and optimize the CMP process.

After that, the parallel lap fixture is mounted onto polisher hand as shown in Figure 3.13.



Figure 3.6: Allied multi-prep polisher machine

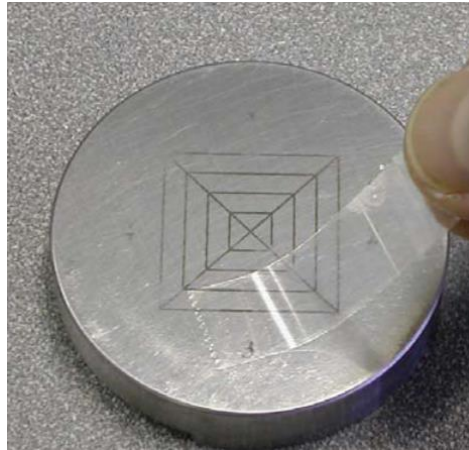


Figure 3.7: Put double sided tape on fixture surface

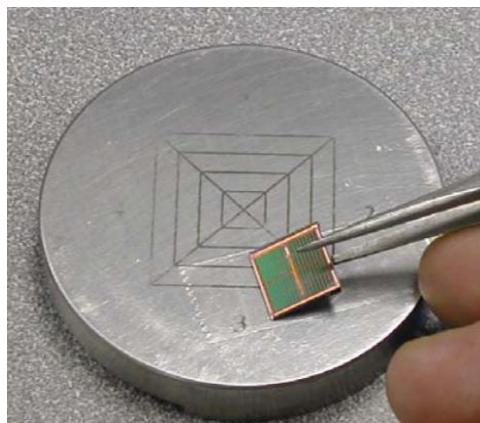


Figure 3.8: Mounting a die on allied multi-prep polisher machine



Figure 3.9: Use cotton swab to pressure the die down to make sure stick firmly

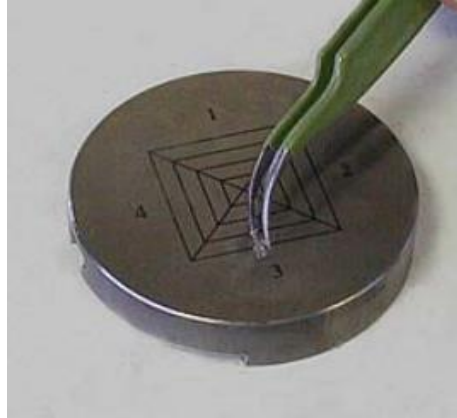


Figure 3.10: Parallel lap fixture is heated on hotplate and wax is put on it

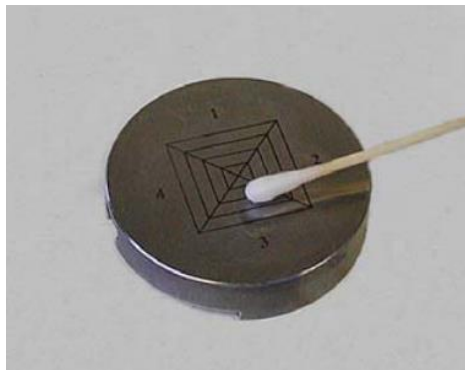


Figure 3.11: Cotton swab is used to spread and thin the wax

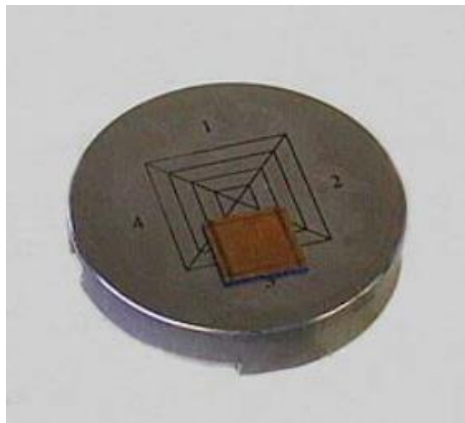


Figure 3.12: Fixture is removed from hot plate and sample align in between centre and edge of parallel lap fixture

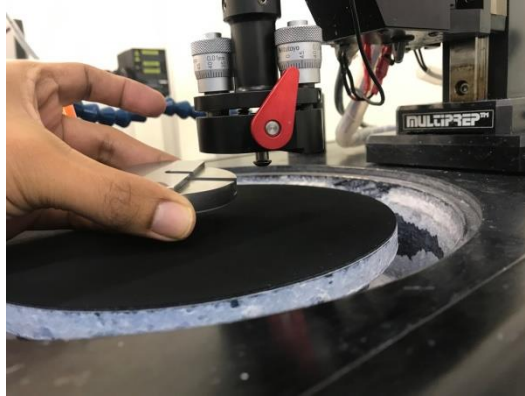


Figure 3.13: Mount the parallel lap fixture onto polisher's hand

A final polishing cloth is used for parallel lap delayering. The cloth surface made to be abrasive. This cloth is used with Colloidal Silica as the slurry. The spinning of the platen and rotation of parallel lap fixture and having contact will cause the CMP to happen. Figure 3.14 shows the parallel lap polishing cloth.

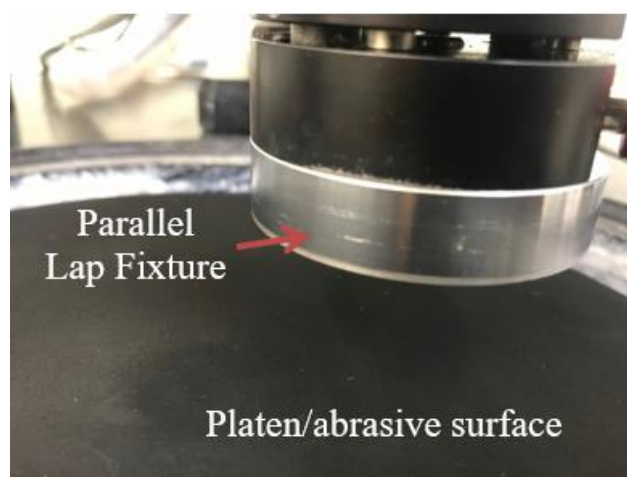


Figure 3.14: Parallel lap polishing cloth

Therefore, before the final cloth is adhered to platen, bottom surface of the polishing fixture is positioned relative to the platen based on sample thickness. It is challenging to

know when contact between the sample and the cloth is made when positioning the sample onto the platen. If lower into the cloth too much, the edges of the die are rounded, and the flatness is affected. Meanwhile, if it does not make adequate contact, it can take long time to remove a layer. Thus, a quantitative method based on die thickness is used to position the sample to ensure sufficient contact with the final polishing cloth to maintain planarity of the entire die while material is removed at a reasonable rate (Liechty et al., 2005). The distance to polishing cloth is shown in Figure 3.15 below.

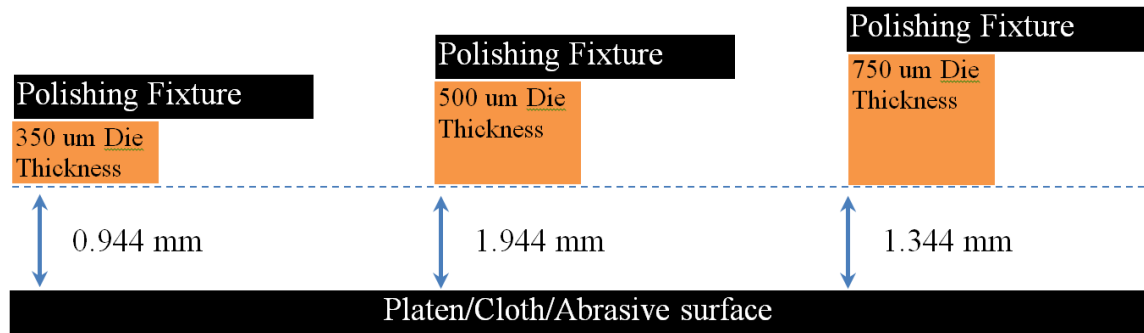


Figure 3.15: A quantitative method for sample positioning distance to final polishing cloth (Liechty et al., 2005)

To set the distance from polishing cloth to bottom of polishing fixture, the formula is

$$(T_s - T_c) - T_d + 0.116 \text{ mm} \quad \text{Equation 3.5}$$

Where:

T_s = Spacer thickness

T_c = Cloth thickness

T_d = Die Thickness

The parallel lap polishing fixture thickness is 12.65mm. The optimize distance between bottom of parallel polishing fixture is 116 μ m.

With the sample load set to full, the spindle riser is lowered, and the front dial indicator is set to zero. Another polishing fixture is used to set the Spacer thickness. For an example,

$$T_d = 0.5 \text{ mm}$$

$$T_s = 12.65 \text{ mm}$$

$$T_c = 1.094 \text{ mm}$$

Therefore,

12.65mm (Spacer thickness) – 1.094 mm (Cloth thickness) = 11.556mm is the dial indicator setting. The distance from platen is shown in Figure 3.16 below:

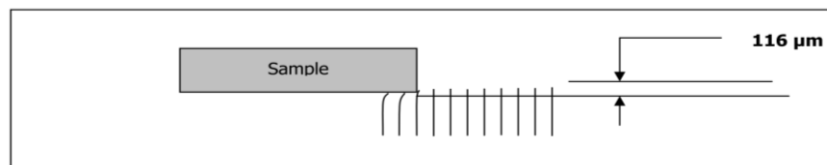


Figure 3.16: Distance between bottom of parallel polishing fixture and the platen

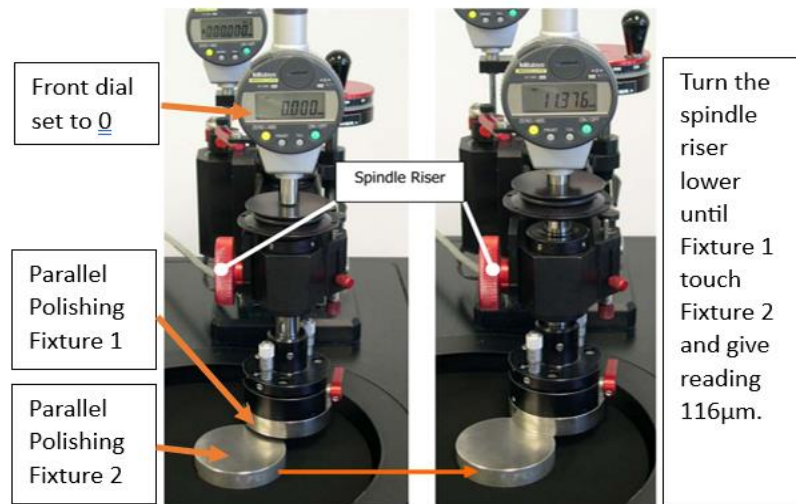


Figure 3.17: Distance between bottom of parallel polishing fixture and the platen

As shown in Figure 3.17, another parallel polishing fixture has been used for the spacing. The spindle riser is lowered until the polishing fixture contacts the spacer and the dial indicates the predetermined value (from zero). Once this step is completed, the spindle is lifted using a spindle riser and the vertical position of the sample relative to the platen is left un-changed.

The system settings for the parallel polishing are shown in Figure 3.18 below.

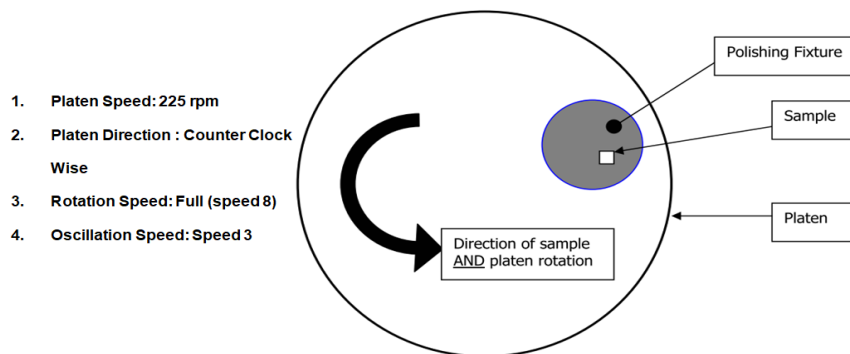


Figure 3.18: Parallel lap polishing current settings (Liechty et al., 2005)

The slurry used is 0.05 μm Colloidal Silica Blue Diamond Suspension shown in Figure 3.19 below. This slurry is poured onto the parallel lap final polishing cloth.



Figure 3.19: Parallel lap polishing slurry

One or two drop of slurry in every second is recommended to produce a consistent, constant supply of abrasive. Increased flow will increase the polishing rate (Chen et al., 2012). During polishing, coolant is activated so that the stream touches the outer edge of the cloth and gently splash water into the bowl, thus cleaning the sides and keeping the colloidal silica from drying.

To start the polishing, platen is activated at 225 rpm counterclockwise rotation together with sample oscillation and polishing cloth is saturated with water. The spindle riser

is lowered, and slurry is applied. Figure 3.20 shows the applying slurry and activate coolant during parallel lap polishing.



Figure 3.20: Applying slurry and activate coolant during parallel lap polishing

To check the parallel polishing result, the sample is raised from polishing cloth using the spindle riser and the parallel lap polishing fixture is unmounted and the sample is rinsed using De-ionized (DI) water for 5 to 10 seconds. Then, sample is dried using compressed CDA in one direction flow to eliminate water spots. Once the sample is cleaned, the ROI observation can be made under an optical microscope as shown in Figure 3.21.

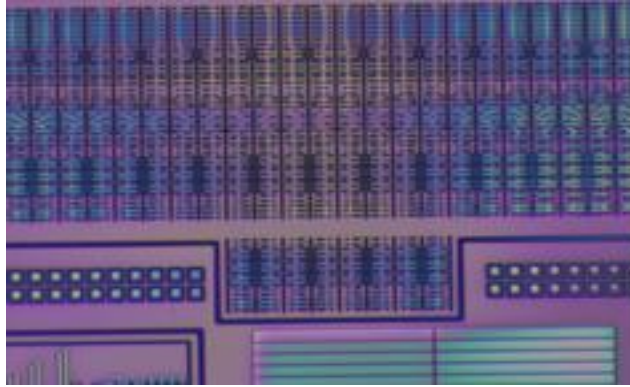


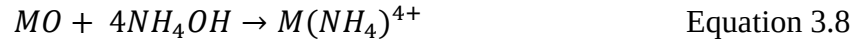
Figure 3.21: Optical image of SOI gate poly (cell) after parallel lap polishing until polysilicon layer

Parallel lapping solves uneven surface and improves material etching very well as compared to using chemical etching alone. The even surface is vital for an accurate isotropic wet etch delayering when applying Poly-etchant solution.

3.3.5 Poly-etchant Wet Etching

The use of Poly-etchant solution is to remove the remaining polysilicon and reveal the gate oxide layer. A clean exposed silicon substrate is vital to allow wet etchant solution to be carried out successfully to reveal silicon defects. This is an important capability to check gate oxide for any defects. Such as pinhole gate oxide defect (C. K. Oh et al., 2004).

After parallel lap polishing reached polysilicon layer, the sample was immersed in a Poly-etchant solution ($1\text{NH}_4\text{OH}:1\text{H}_2\text{O}_2:5\text{H}_2\text{O}$) for 2 minutes to remove organic compound and metallic particle (C. K. Oh, 2004). The cleansing reaction can be shown in Solution 1. This solution further etches the remaining polysilicon layer which cannot be removed by parallel lapping alone due to small, thin, and dense structure. The chemical reaction is in removal of polysilicon and is derived in Solution 2. The color changes from pinkish to greenish indicate polysilicon layer was removed in Figure 3.22.



Equation 3.8 (Removes organic compound and metallic particle)



Equation 3.9 (Removes polysilicon)

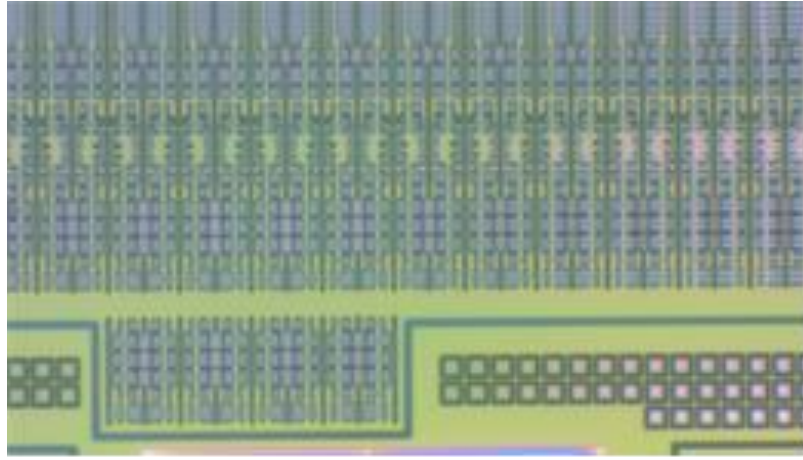


Figure 3.22: Optical image of SOI gate poly (cell) after removing polysilicon layer using poly-etchant solution

The efficiency of parallel lap polishing followed by Poly-etchant solution to remove small, thin, and dense gate polys was verified using SEM in Figure 3.23.

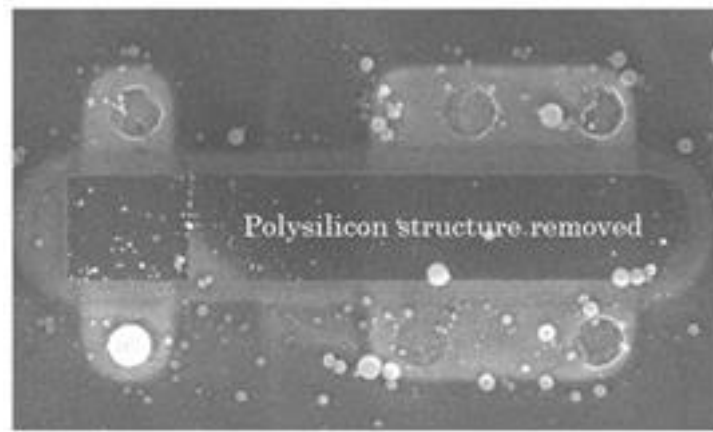


Figure 3.23: SEM top view image shows small, thin, and dense gate polysilicon's on active, and oxide were removed

3.3.6 Design of Experiment (DOE) of Diluted and Time Controlled Hydrofluoric Acid Etching

Once gate poly is removed in Figure 3.23, the next delayering step is to carefully etch the ILD oxide using hydrofluoric acid etching and revealing active layer underneath. The purpose of this step is to investigate any abnormality at active structures.

Formula of HF dilution is below:

$$C1V1 = C2V2 \quad \text{Equation 3.10}$$

Where “1” represents the concentrated conditions and “2” represents the diluted condition. Volume $V1$ of the solution with concentration $C1$ is measured. Then, enough DI water is added to make a total volume $V2$. This new solution will have your desired concentration.

Therefore, the new HF volume requires:

$$V2 = \frac{C1V1}{C2} \quad \text{Equation 3.11}$$

To get the ideal HF concentration percentage (%) and effective etching rate to etch the ILD oxide and preserve structures on Top of Silicon, a DOE was conducted. A Mini Cell structure which has a very thin, dense cell type, surrounded with DTI is selected. This structure was purposely selected as it contains dense polysilicon which is hardest to clean as compared to blanket or big wide gate poly like capacitor design (C. K. Oh et al., 2004). Furthermore, the structure located near DTI line makes it so brittle and prone to mechanical damage during supersonic debris cleaning. Therefore, if the experiment able to get rid of the thin and dense polysilicon on Mini Cell structure, then it should be easier to clean at other area such as big and wider gate poly in SOI wafer. The Mini Cell structure consists of 8 columns and 6 rows of bit cells as an input parameter result in DOE as shown in Figure 3.25 below.

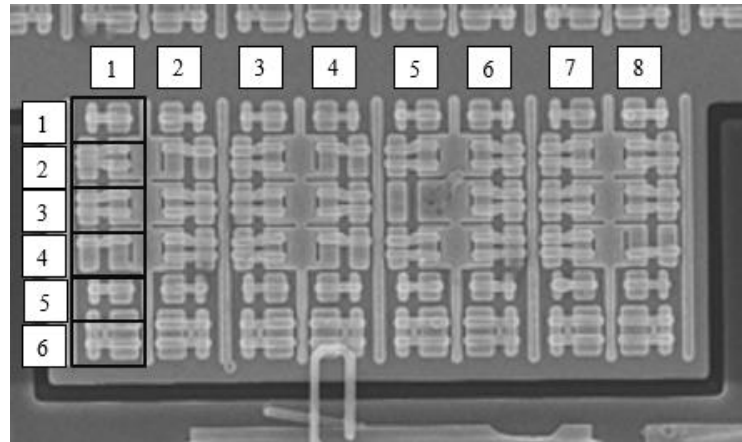


Figure 3.24: SEM top view image shows mini cell structure nearby DTI

3.3.7 Design of Experiment with MiniTab 17

MiniTab 17 is a powerful statistical software which used in this experiment to generate DOE results. Target of the DOE results are to get clean bit cell amount on the active surface with no damage at top silicon level. The more amount of a clean bit cell which no gate poly or oxide remains on active, the better the scoring.

DOE using Minitab 17 software.

1. 7 sample input to generate 7 sample output.
2. HF dilution methodology after knowing from Minitab DOE
3. Cross-section checks for clean and undamaged bit cell.

3.4 Design and Fabricate RAPH (Rapid Alignment Polisher Hand) Prototype

Once we reach the stage of ability to delayer SOI sample into polysilicon layer then to substrate layer to reveal DTI pattern, it is crucial to have a polisher hand that able to obtain a super straight polishing line for an advance cross-section analysis. A perfect alignment is also vital to do polishing more than one target in a wide area of observation for apple-to-apple profile comparison of polishing targets.

Thus, RAPH's Prototype A then Prototype B were invented for this purpose.

3.4.1 RAPH's Prototype A

This is the initial prototype that made from aluminium material. The fabrication was using CNC machining for precision build. Before beginning to fabricate prototype A, a model using 3D printer was drawn and build is shown in Figure 3.25.

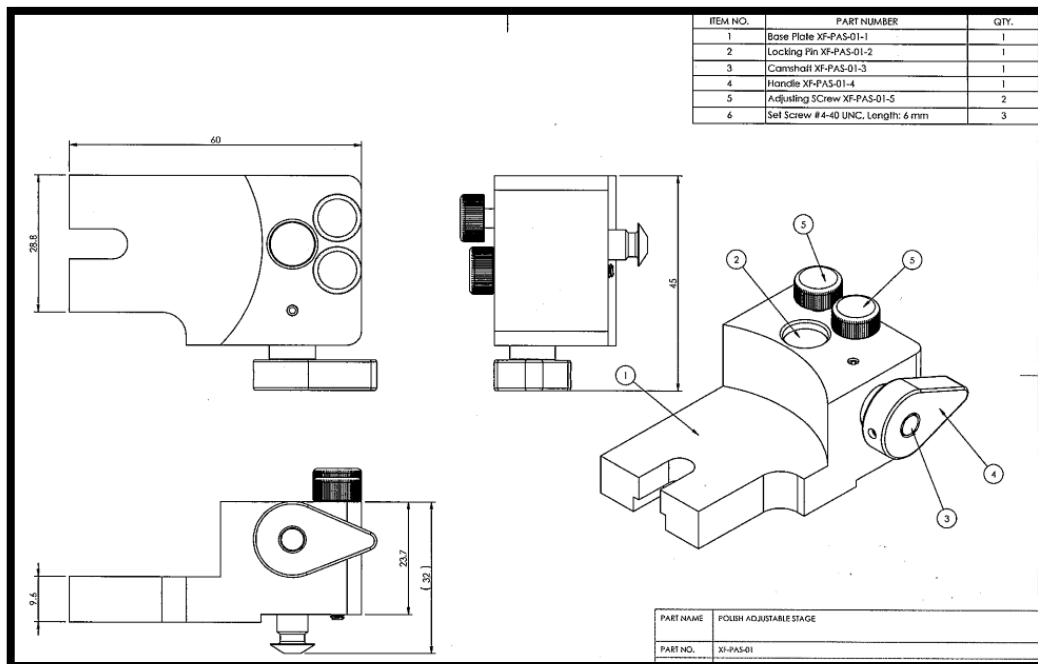


Figure 3.25: Prototype A

3.4.2 RAPH's Prototype 'A' Weakness

Few issues were immersed while testing RAPH's Prototype A which are:

- Item Clamp Piston Head bigger than specification as shown in Figure 3.37 was fixed. Diameter specification should $9.5 \pm 0.5\text{mm}$. However, the actual diameter of the clamp piston head is 12mm.

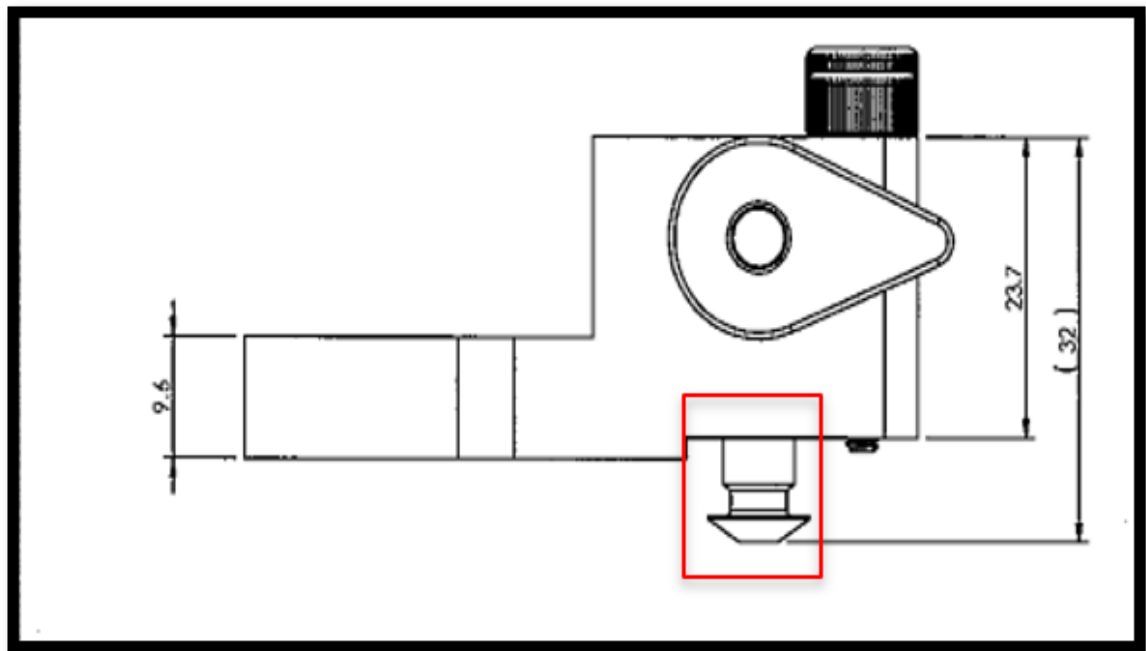


Figure 3.26: Clam piston head out of spec

- b. Item 2 - Locking Pin smaller than specification as shown in red arrow Figure 3.27. The correct Diameter for Locking Pin is $23.25 \pm 0.5\text{mm}$.

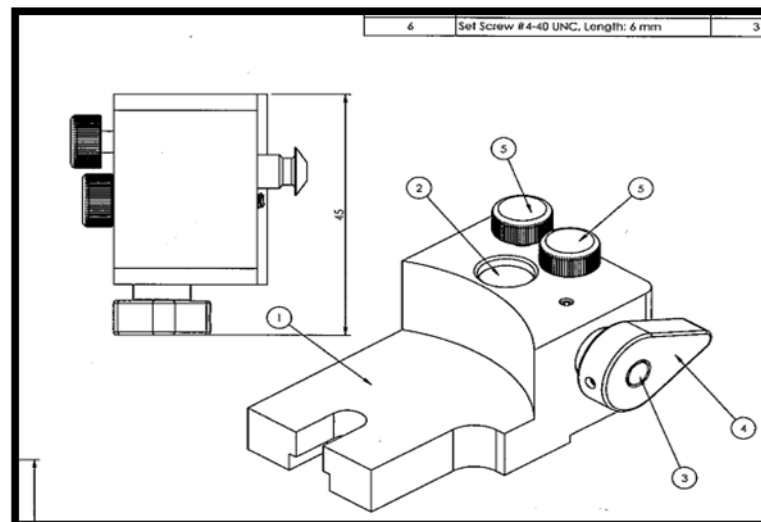


Figure 3.27: Locking Pin – Item 2

- c. Item 5 - Adjustment Screw when turn, it pushes the stage X.Y and Z axis together which is not wanted.

Although the out of specification issues are fixed for Prototype A, the Z axis movement is inevitable. Prototype A also failed during spinning platen test.

3.4.3 RAPH's Prototype B

Same material and fabrication method like Prototype A were used to fabricate RAPH's prototype B. The difference for Prototype B was the introduction of Z Groove. The Z Groove design will lock Z-axis while allowing X and Y Axis to move. Z Groove, Based Plate and Bottom Plate design shown in Figure 3.28 below. Figure 3.29 shows the RAPH's prototype B based plate design and Figure 3.30 shows the RAPH's prototype B bottom plate design.

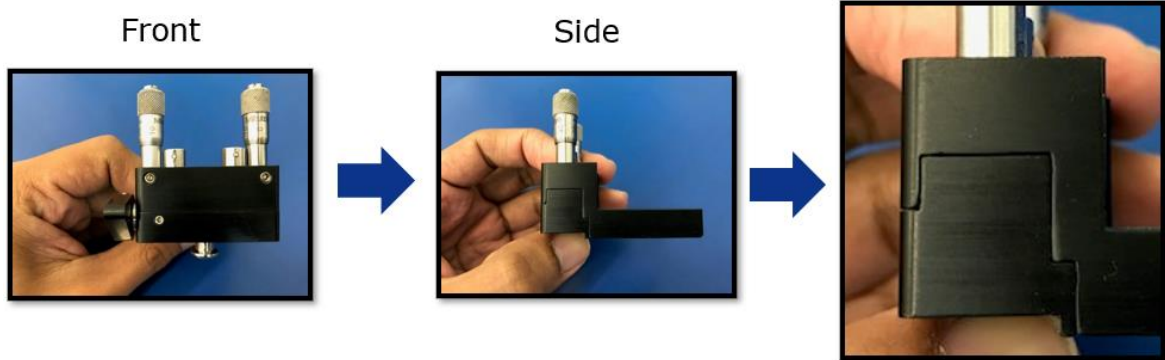
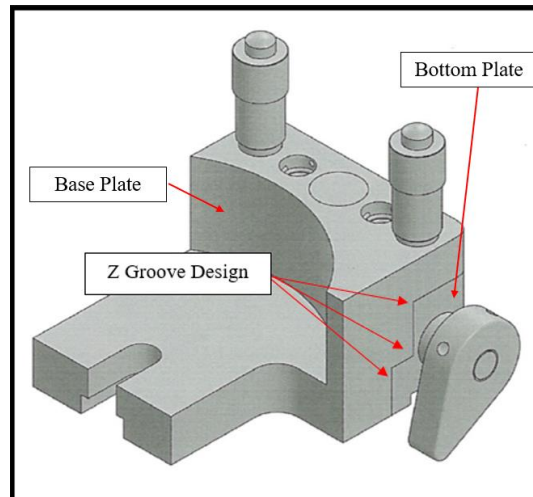


Figure 3.28: Design of Z groove to lock Z-axis while allowing X and Y-axis to move freely

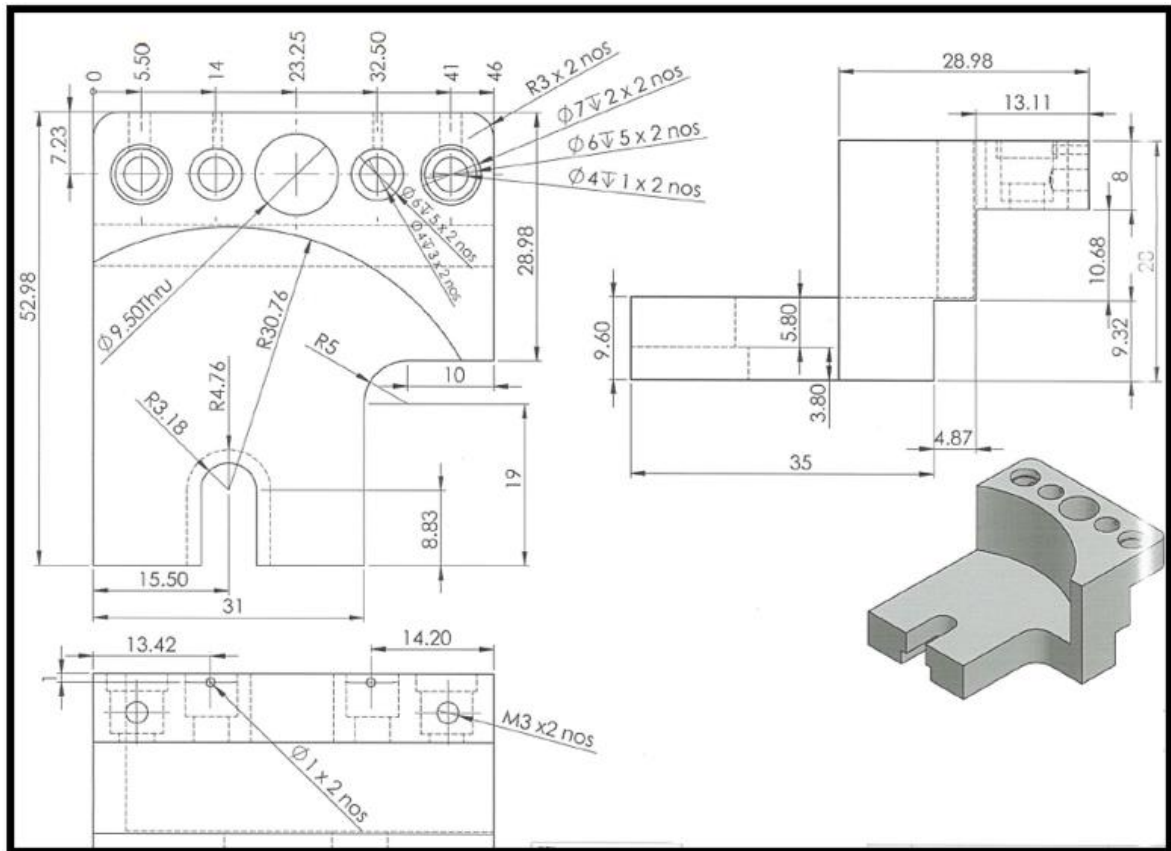


Figure 3.29: RAPH's prototype B based plate design

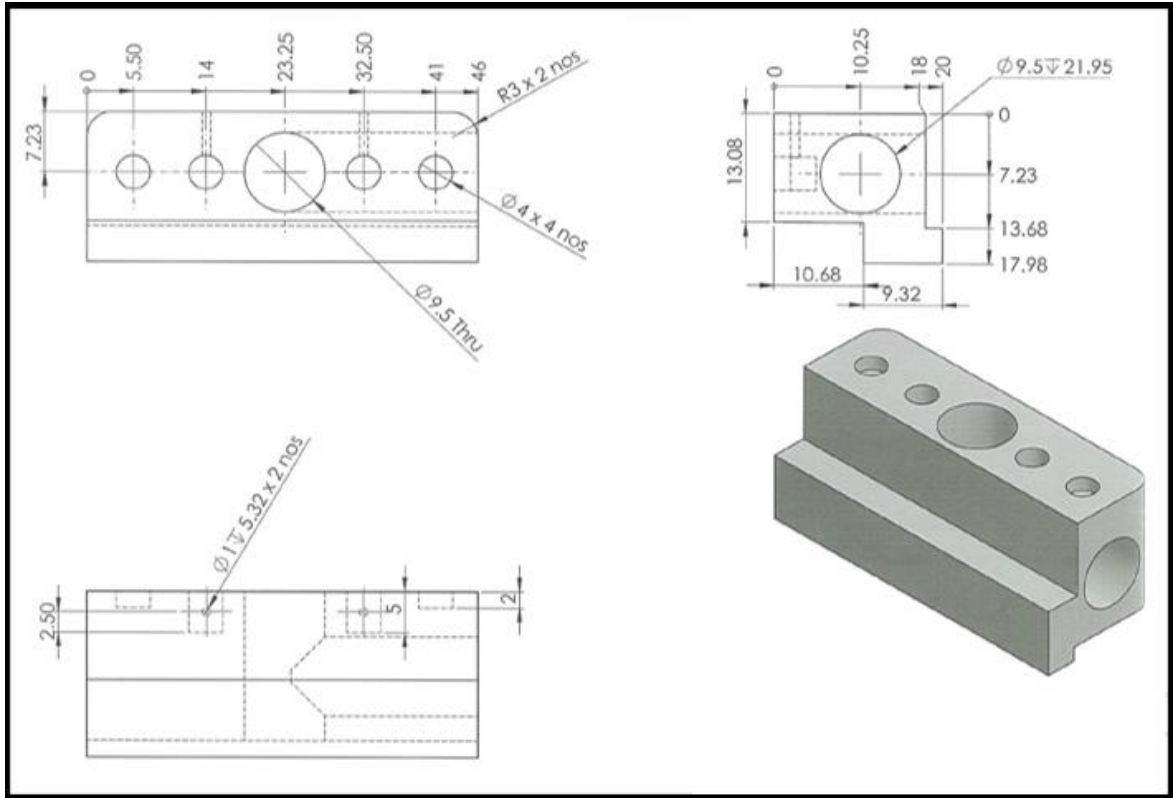


Figure 3.30: RAPH's prototype B bottom plate design

3.4.4 RAPH Performance Evaluation

Performance evaluation is to prove that RAPH is capable to polish in a straight angle which traditional Polisher Hand is not capable to perform. The performance evaluation includes:

- RAPH adjustment Straightness test
- RAPH Unadjusted versus Adjusted angle variance
- Mount-unmount Consistency Test
- Image Quality Test as compared with traditional Polisher Hand
- RAPH Behaviour during High-Speed Platen Spinning Test

3.4.5 RAPH Straightness Test

Straightness test conducted to compare Conventional Polisher Manual Alignment method and RAPH Method perpendicular to straight line pattern in a die.

With respect to the performance characteristics of the RAPH apparatus, an adjustment straightness test was performed with the RAPH, which is a measure of how close to a 90 degree angle a polished wafer edge is after the micrometre screws on the RAPH has been adjusted. Given that the distance between the left and right micrometer screws on the RAPH is 34.5 mm as shown in Figure 3.31 and that the angle between the wafer edge and the vertical top-down features on the wafer sample has been measured using a computer connected to an optical microscopy system.

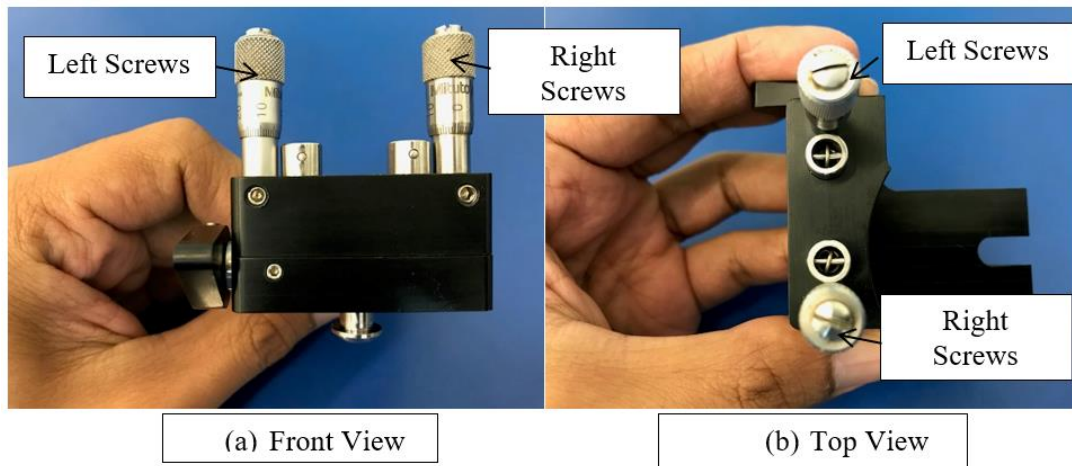


Figure 3.31: Micrometre's left and right screws front and top view

The equation to be used for adjusting the RAPH screws to achieve a right angle is then as follows:

$$Dh = 34.5 \tan (\theta - 90) \quad \text{Equation 3.12}$$

Where θ is the angle as measured by the optical microscopy system. The derivation of the equation is illustrated by Figure 3.32 below.

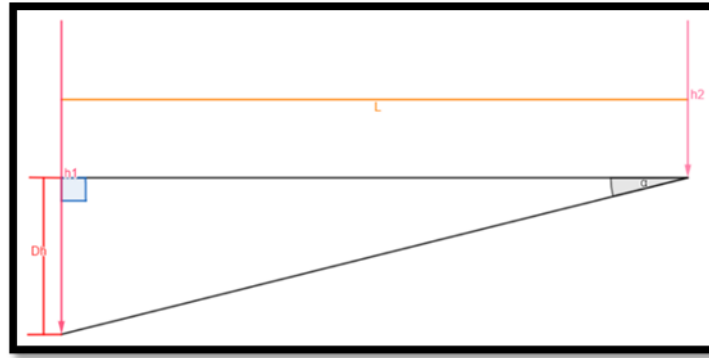


Figure 3.32: Derivation of the equation where θ angle measured by optical microscopy

If the angle θ is greater than 90 degrees (DBC), the sample is skewed counterclockwise and Dh is positive, so that the left screw on the RAPH needs to be turned and lowered, by the amount specified by Dh .

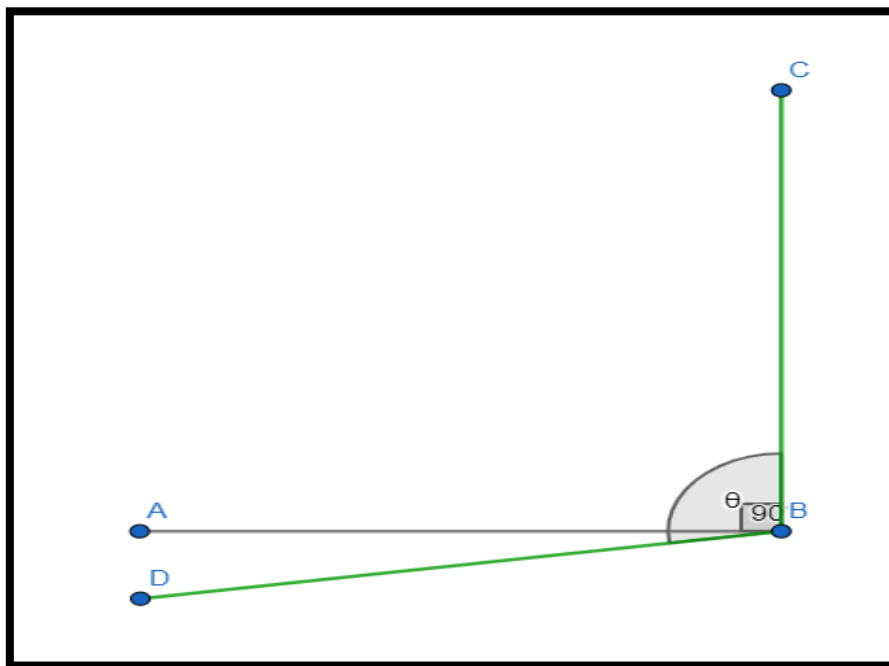


Figure 3.33: The case when the measured angle (measured counterclockwise) is greater than 90 degrees

Figure 3.33 shows the case when the measured angle (measured counterclockwise) is greater than 90 degrees. The left screw on the RAPH needs to be adjusted downwards to bring the wafer edge angle to 90 degrees. On the other hand, if θ is less than 90 degrees, the sample is skewed clockwise and D_h is negative, so that the right screw needs to be adjusted.

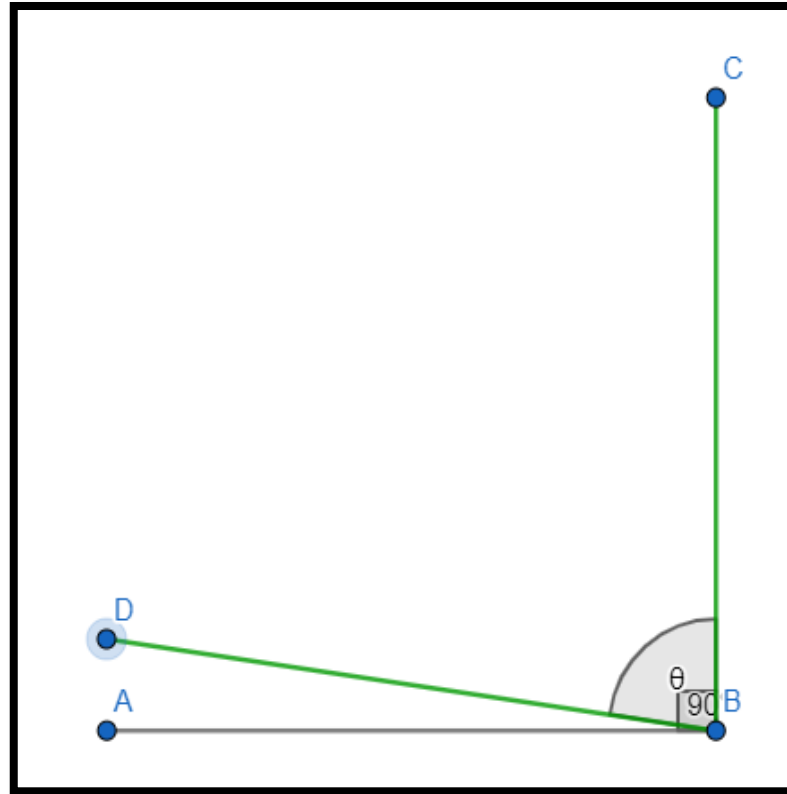


Figure 3.34: The angle is less than 90 degrees, measured counterclockwise

Figure 3.34 shows angle is less than 90 degrees, measured counterclockwise. So the right screw needs to be adjusted downwards to get a 90-degree angle. On the other hand, if θ is less than 90 degrees, the sample is skewed clockwise and D_h is negative, so that the right screw needs to be adjusted.

In practice, a deviation of 0.15 degrees from the right angle is tolerated for the straightness test. To conduct the straightness test, the wafer sample is cross-section polished

with the polisher hand initially unadjusted, down to 0.5 micrometre grit level, so that the wafer edge is clearly defined when put under the microscope later. Then the angle of the wafer edge is measured using a computer connected to an optical microscope to obtain the necessary adjustment height. The wafer sample is then cross-section polished again, with the polisher hand screws adjusted according to the Equation 3.12. After that, the wafer sample is brought under the microscope again and the angle measured on the same computer.

3.4.6 RAPH Unadjusted versus Adjusted Angle Variance

This experiment aims to find out if the variances and subsequently the standard deviations in the wafer edge angles between zero adjustment and non-zero adjustments of the RAPH are equal, in other words if the wafer edge angles are consistent whether the micrometre screws are adjusted. Ideally there should not be much variation.

To perform this experiment, one wafer sample is attached to the RAPH and polished while the difference between the micrometre screw readings is 0 mm, effectively making zero adjustment. A second wafer sample is then also attached to the RAPH and initially polished without making any adjustments to the micrometre screw, in order to measure the skew angle of this sample. Then after the angle is known, the micrometre screw is adjusted accordingly, using the equation of: $Dh = 34.5 \tan (\theta - 90)$.

3.4.7 Mount-Unmount Consistency Test

This test determines how consistent the polished wafer edge angles are when the polisher stage is mounted and unmounted on the RAPH repeatedly. This mounting and unmounting action is repeated as one changes polisher pad films, hence the purpose of this test. Ideally there should be no variance in the polished wafer edge angles when the polisher stage the wafer samples are attached to are repeatedly mounted and unmounted from the

RAPH. In practice, due to irregularities with the polisher machine as well as the pads and films, there will be slight variations in edge angles when the same sample is mounted and unmounted repeatedly. This test evaluates how big these variations are. Mount-unmount polisher stage shown in Figure 3.35.

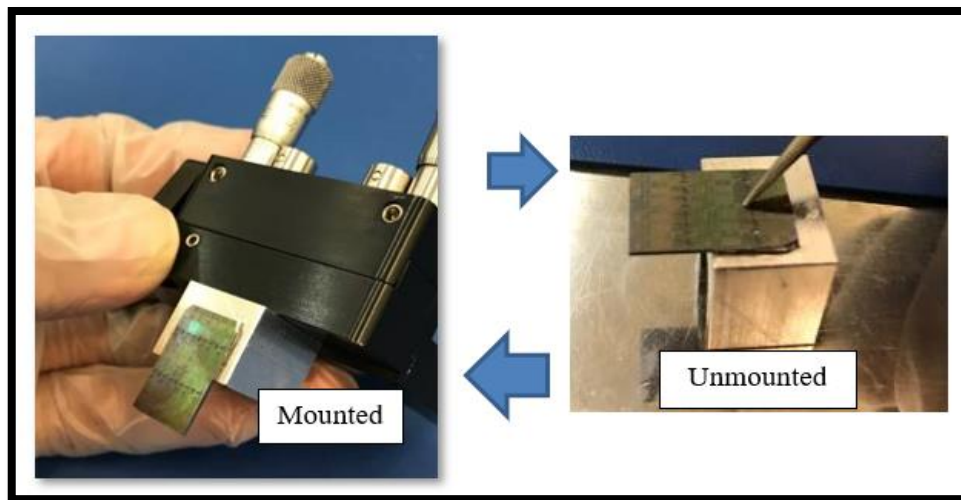


Figure 3.35: Mount and unmount polisher stage to RAPH fixture

3.4.8 Image Quality Test as Compared with Traditional Polisher Hand

SEM was employed to check the surface profile quality after using RAPH and compare with the traditional Polisher stage. This test basically proves that using RAPH's image quality is comparable or better than the traditional Polisher Hand.

3.4.9 RAPH Behaviour during High-speed Platen Spinning Test

This test is to check RAPH stability during spinning operation where RAPH with sample stage mounted on polisher arm. The sample then grinds onto polisher diamond film pad as shown in Figure 3.35. The spindle speed test was set from 100 – 600 rpm. The manual operation is 100 – 250 rpm. The maximum 600 rpm in normal operation period will prove

that RAPH stability is comparable with traditional Polisher Hand. Figure 3.36 shows the chemical and mechanical cross-section polishing in operation using RAPH.

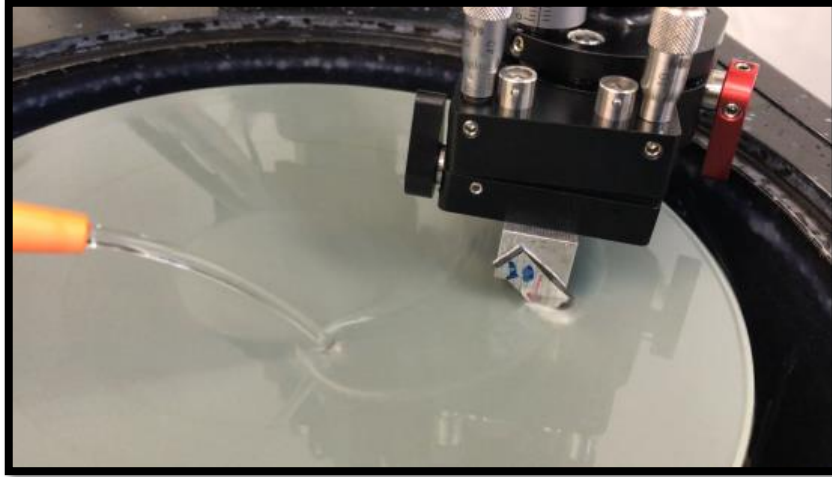


Figure 3.36: Chemical and mechanical cross-section polishing in operation using RAPH

All the results from the 5 tests above will be explain in next Chapter Result and Discussion.

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Overview

This chapter is divided into three main parts. The first part focuses on pre-processing of delayering result and discussed the suitable technique for delayering SOI wafers. The second part presents the result of improvement in a cross-sectioning method by inventing RAPH to enable polishing in straight line for Long and Narrow DTI Line in SOI wafer. Finally, the result of RAPH's performance evaluation on cross-section polishing, RAPH's method application, capability, accuracy, and productivity are then demonstrated.

4.2 The Use of CMOS Delayering Recipe into SOI Wafer Type

The etching is using 49%HF → SC1 Solution → Poly-Etchant Etching → Oxide Removal. This polysilicon etching method works for wide poly such as P-bulk capacitors. This method was employed to test its removal efficiency for thin, small, and dense poly at SRAM cell area in SOI wafer as shown in Figure 4.1.

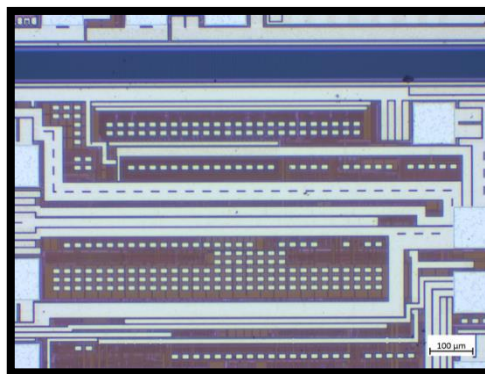


Figure 4.1: Optical images of full process die sample (top metal line with passivation)

After dipping in 49% HF for 2 ~ 3 minutes, optical microscope inspection found uneven layer surface as lens defocus occurred. Microscope's lens defocus occurred due to some area is higher than another or basically the surface not flattened. Some areas were found with exposed polysilicon and some still covered by previous layer or etching debris. Acetone was used to remove the debris of previous layers but failed as shown in Figure 4.2 below.

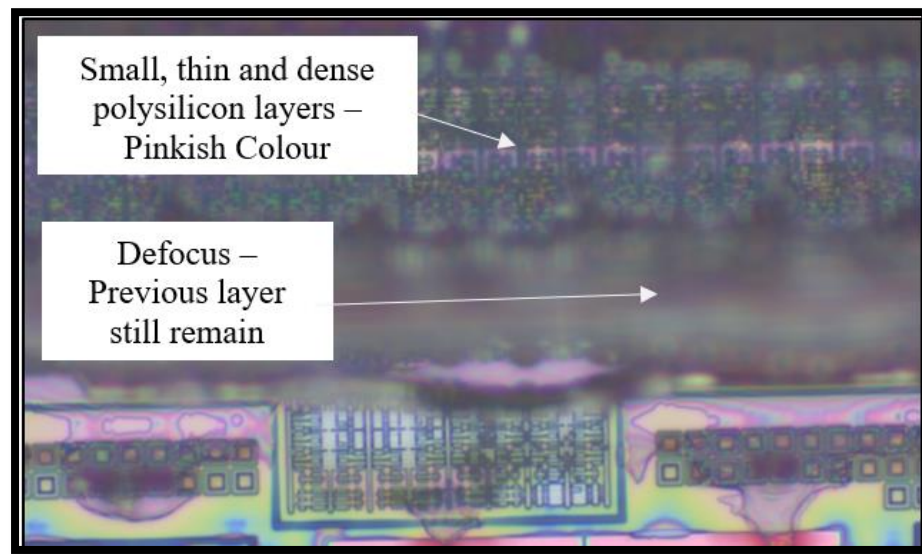
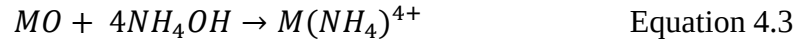


Figure 4.2: Optical images of gate poly (cell) after applied 49% HF for 2 minutes and cleaned with acetone

Next, the sample was immersed into SC1 solution (1NH₄OH:1H₂O₂:5H₂O) for 3 minutes at temperature of 50⁰ C. The reason of using SC1 solution is to remove organic compound and metallic particle (C. K. oh et al., 2004) derived in Equation 3.3.





The SC1 solution and acetone cleaning, the remaining layers persist but the etching debris or dirt was gone as shown in Figure 4.3 below.

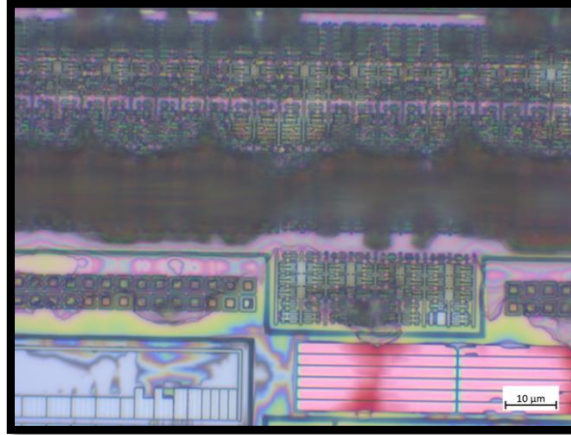


Figure 4.3: Optical images of gate poly (cell) after applied SC1 solution for 3 minutes and cleaned by acetone

Next, Poly-Etchant solution was employed to etch polysilicon layer. The polysilicon etch solution was 20NHO₃:8CH₃COOH:1HF. The result after this etchant is shown in Figure 4.4 below.

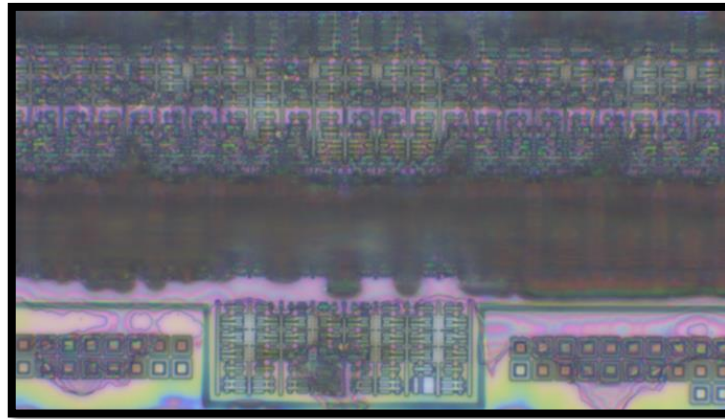


Figure 4.4: Optical images of gate poly (cell) poly-etchant solution

The Poly-etchant solution was not removing all the poly gates on the SRAM area. The surface found still uneven with previous layer stacking up. The remnant materials were possibly metal, nitride and oxide as shown in Figure 4.4. As for the reason, it was not possible to continue with HF removal followed with Wright Etchant solution to reveal substrate defects. The remaining layer mixed with oxide will behave as a barrier and block the Wright Etchant etching process. The CMOS delayering technique or recipe obviously cannot be used for SOI Wafer type.

4.3 The Reasons for CMOS Delayering Method is Not Suitable for SOI Wafer Type

The recipe of 49%HF → SC1 Solution → Poly-Etchant Etching → Oxide Removal only works for wide polysilicon such as capacitors but not dense gate poly. Thus, it only works for Bulk CMOS wafer (Misra et al., 2002) and not suitable for SOI wafer (Ahmataku et al., 2018). The 49% HF concentration will easily etch away the BOX layer. Hence, the top silicon will peel off and die during supersonic cleaning as depicted in Figure 4.5 below.

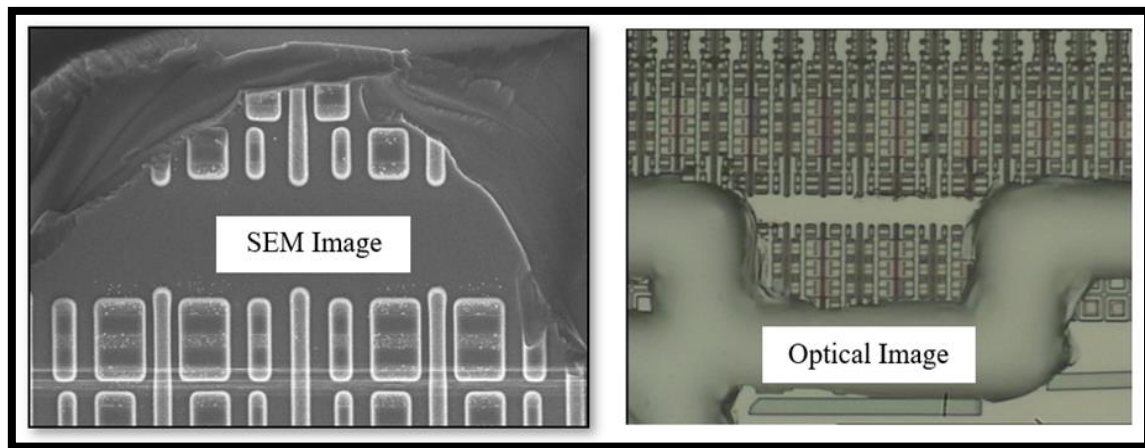


Figure 4.5: Top silicon die peeled off and damaged during supersonic cleaning

The CMOS Delayering technique is only suitable for Bulk CMOS wafer where there will be no concern of etching away BOX layer as illustrated in Figure 4.6 below.

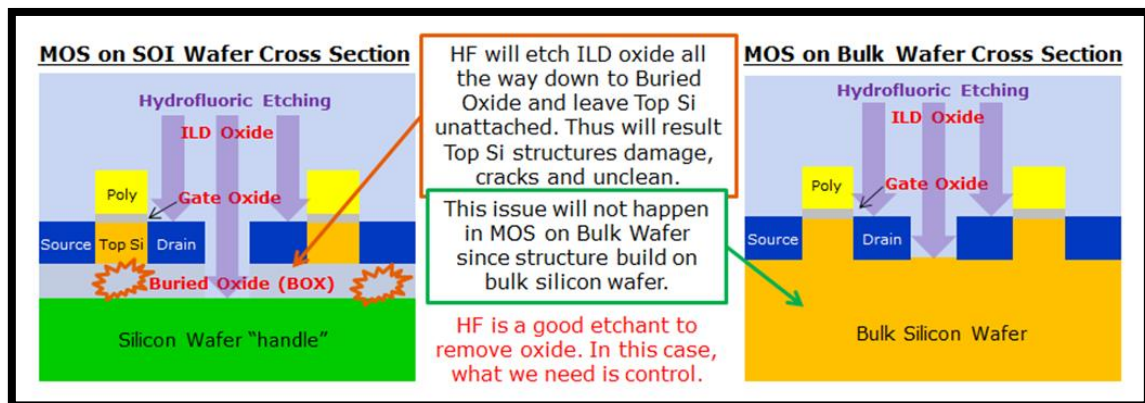


Figure 4.6: Challenges of delayering SOI technology wafer compared to bulk CMOS wafer

The phenomenon of peeling off Top Silicon Die is due to harsh etching of HF acid with concentration of 49% and long exposure time. HF acid will etch ILD Oxide all the way down from ILD Oxide then Gate Oxide to Buried Oxid (BOX) and leave Top Silicon unattached. Hence resulting Top Silicon structure damaged, cracks and unclean. These

problems were not observed in Bulk CMOS Wafer Type as the structure is built on bulk silicon wafer. However, HF acid is efficient to remove oxide layer as it is very selective to oxide.

Therefore, a proposed method which utilizes Parallel Lapping + Diluted and Time Controlled Hydrofluoric Acid Etching was developed. The idea is to avoid Top Silicon peel off or damage during cleaning (supersonic) while controlling the DTI etching. The HF etching must halt before reaching DTI's bottom. This method will remove remaining ILD oxide, and GOX underneath gate poly meanwhile preserve top silicon structure from damage or peel off in SOI wafer. Since the thin, small, and dense gate poly hold by thin GOX and remaining ILD oxide, removing these oxides layer will together remove the gate poly (Ahmataku et al., 2018).

4.4 Proposed Method to Delayer SOI by using a Combination of Parallel Lap Polishing and Diluted and Time Controlled Hydrofluoric Acid Etching

The method of using 49% concentration of hydrofluoric (HF) acid for 5~10 minutes, then SCI solution to remove poly revealing active layers only works for bulk CMOS wafer (Misra et al., 2002). This method cannot be used for SOI wafers since HF will etch ILD oxide all the way down to BOX and leave the top silicon unattached (Ahmataku et al., 2018). Consequently, this results in the top silicon structures being damaged, cracked, and unclean as shown in Figure 4.7.

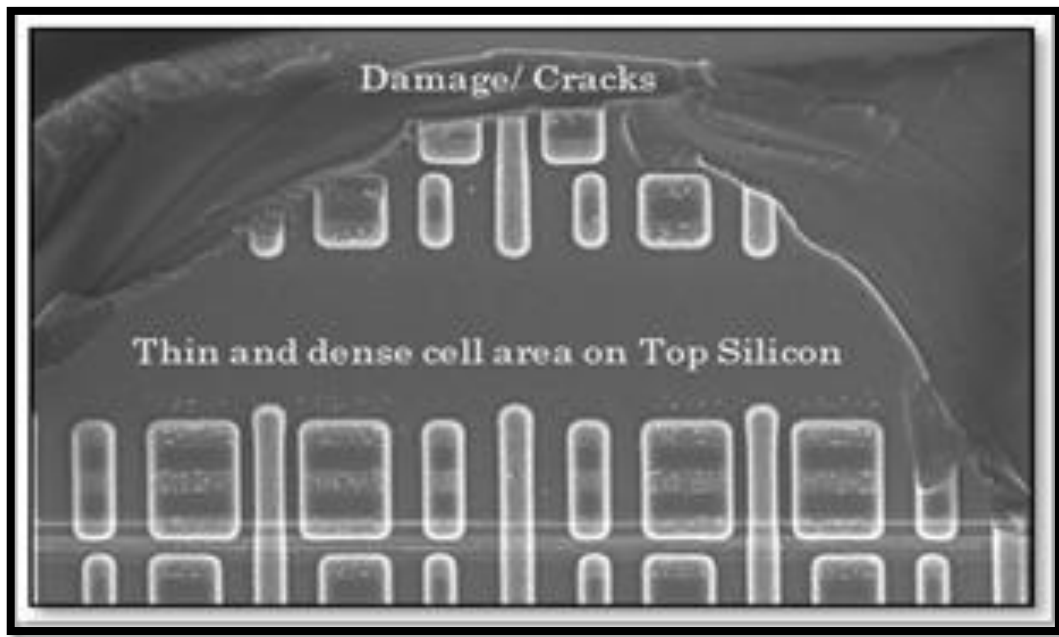


Figure 4.7: SEM top view image shows crack and damage of small, thin, and dense gate cell area on top silicon.

The Parallel Lapping method solves uneven surface and improves material etching very well as compared to chemical etch alone. The even surface is vital for an accurate isotropic wet etch delayering.

4.4.1 Delayer using Parallel Lap Polishing from Passivation Layer to Polysilicon Layer

Parallel Lapping was performed by using Allied Multi-Prep Polishing System – 8” to top-down polish until polysilicon. The pinkish colour indication that lapping reached polysilicon layer as depicted in Figure 4.8 below.

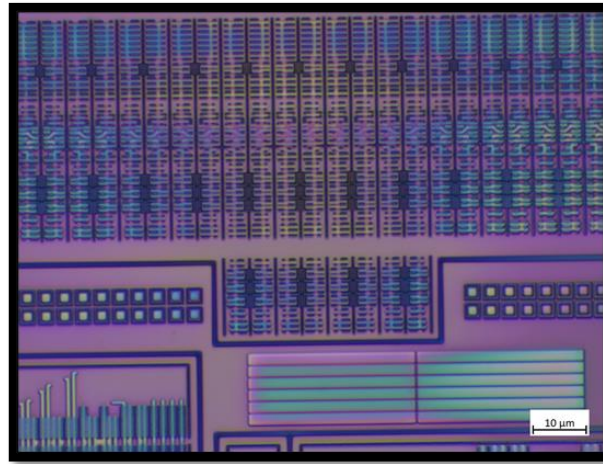


Figure 4.8: Optical images of gate poly (cell) after parallel lapping polysilicon layer

Parallel Lapping to poly silicon was carried out successfully. Optical inspection found sample layer's surface was even and flat. Flatness is the key for a stable wet etching performance that will be carried out in a later step.

The sample was immersed in a Poly-Etchant Solution ($20\text{NHO}_3:8\text{CH}_3\text{COOH}:1\text{HF}$) to remove small, thin, and dense gate polys as depicted in Figure 4.9.

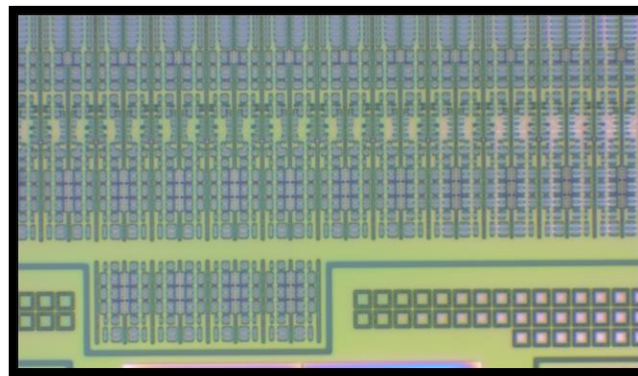


Figure 4.9: Optical images of gate poly (cell) after removing polysilicon layer using poly-etchant solution ($20\text{NHO}_3:8\text{CH}_3\text{COOH}:1\text{HF}$)

The green and see through active structure under optical microscope indicating Poly-Etchant was successfully remove thin and dense poly silicon structure. Now it has reached ILD Oxide. A Flat surface also observed under microscope after applied Poly-Etchant Solution onto the sample. The sample surface was also observed as clean and no debris because the surface layer was flattened after the parallel lap polishing.

High magnification of SEM image shown in Figure 4.10 depicted that gate poly was successfully removed by Poly-Etchant Solution ($20\text{NH}_4\text{OH}:8\text{CH}_3\text{COOH}:1\text{HF}$). The remaining materials after this step were sidewall oxide and ILD oxide. Also observed in SEM image shown in Figure 4.10 some debris visible. This debris was a remnant of oxide particles and can be easily cleaned HF solution. As told, HF is very selective to oxide layer.

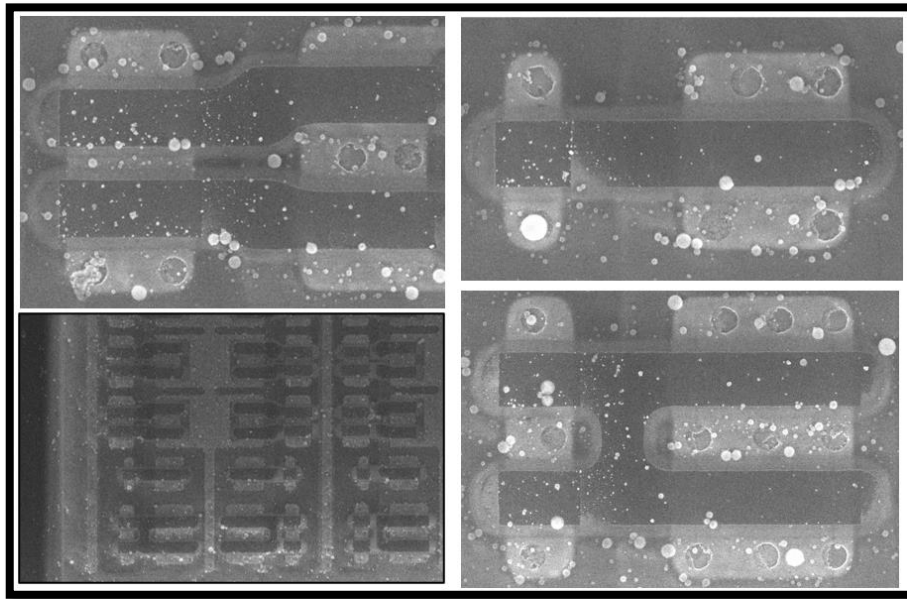


Figure 4.10: SEM images of gate poly (cell) after removing polysilicon layer using poly-etchant Solution ($20\text{NH}_4\text{OH}:8\text{CH}_3\text{COOH}:1\text{HF}$)

4.4.2 Diluted and Time Controlled Hydrofluoric Acid Etching

To get an optimum point between HF concentration, HF immersion time and Supersonic Cleaning time, a DOE using MiniTab17 was carried out.

The factors that need to be studied are HF% concentration (HF%) and HF Immersion Time (HFT). The supersonic vibration was to remove all dirt and debris on top of surface. In this experiment, the Supersonic Cleaning Time (SST) was constant 5 minutes.

A small, thin, and dense poly gate pattern at SRAM area had been selected for this experiment. The outcome of DOE was counts of clean bit in SRAM cell where the total bits were 24 as shown in Figure 4.11 below. If all bits are clean, then this is a good combination of HF% and HFT where Top Silicon Die remain and at the same time thin and dense poly silicon layer can be removed successfully.

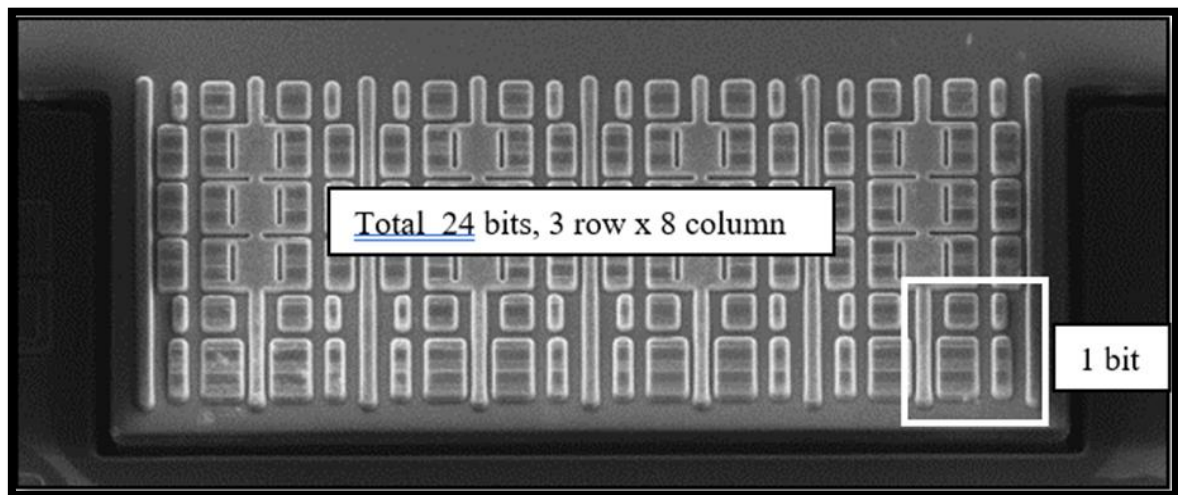


Figure 4.11: Structure of interest: small cell below SRAM which contain 24 bits.

The DOE outcomes will be the count of the clean bits.

Table 4.1: DOE result of 7 suggested samples

Sample ID	HF%	HFT	SST(Constant, 5 Minutes)	Result of Observation	Count of Cleaned Bit
1	15%	10 Minutes	5 Minutes	Not enough HF etching. Poly silicon still remain.	0
2	20%	10 Minutes	5 Minutes	Best Result where all bits were cleaned	24
3	25%	5 Minutes	5 Minutes	Top Silicon Die delamination found	20
4	30%	5 Minutes	5 Minutes	Dirty with debris	15
5	35%	5 Minutes	5 Minutes	Dirty with debris	10
6	40%	5 Minutes	5 Minutes	Not stable etching. Some parts clean and some part not.	10
7	45%	5 Minutes	5 Minutes	Top Silicon Peeled Off and cracks observed.	21

The best response was sample 2 (20%HF → 10 minutes HFT → 5 minutes) where all 24 bits were clean as shown in Figure 4.12. The over-etched was Sample 7 (45%HF → 5 minutes HFT → 5 minutes SST) where the top silicon cracks shown in Figure 4.13. This Top Silicon cracks and peel off were due to over-etched DTI trench oxide. Meanwhile, Sample 1 was under-etched where polysilicon and oxide layer were still remaining as shown in Figure 4.14.

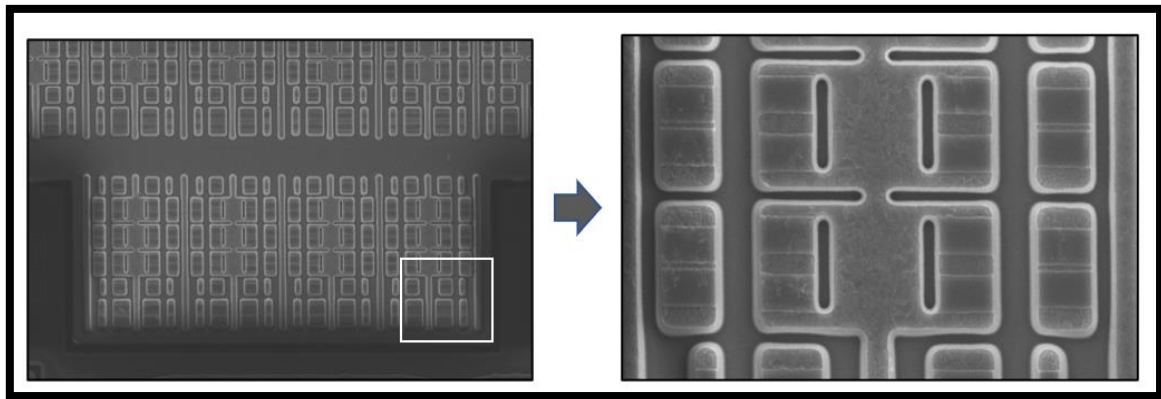


Figure 4.12: SEM images of gate poly (cell) after immersing in 20% HF for 10 minutes resulted with all 24 bits cleaned (Sample 2)

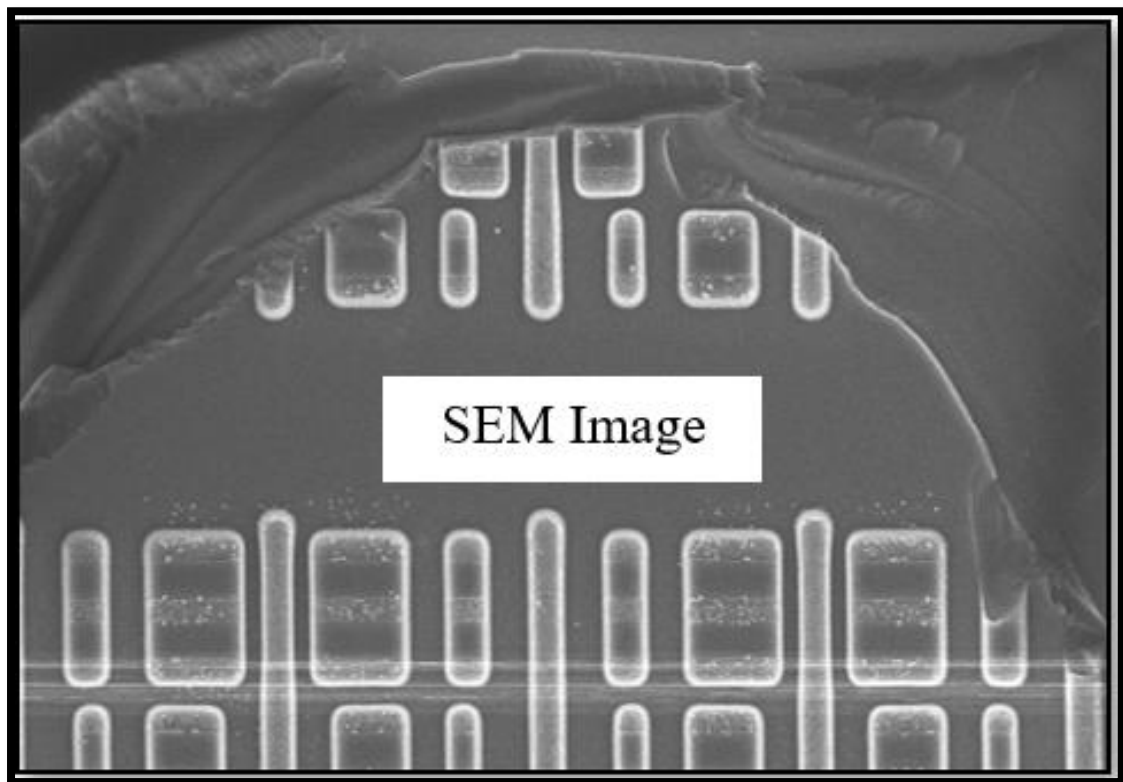


Figure 4.13: SEM image of top silicon cracks due to over-etched DTI trench (Sample 7)

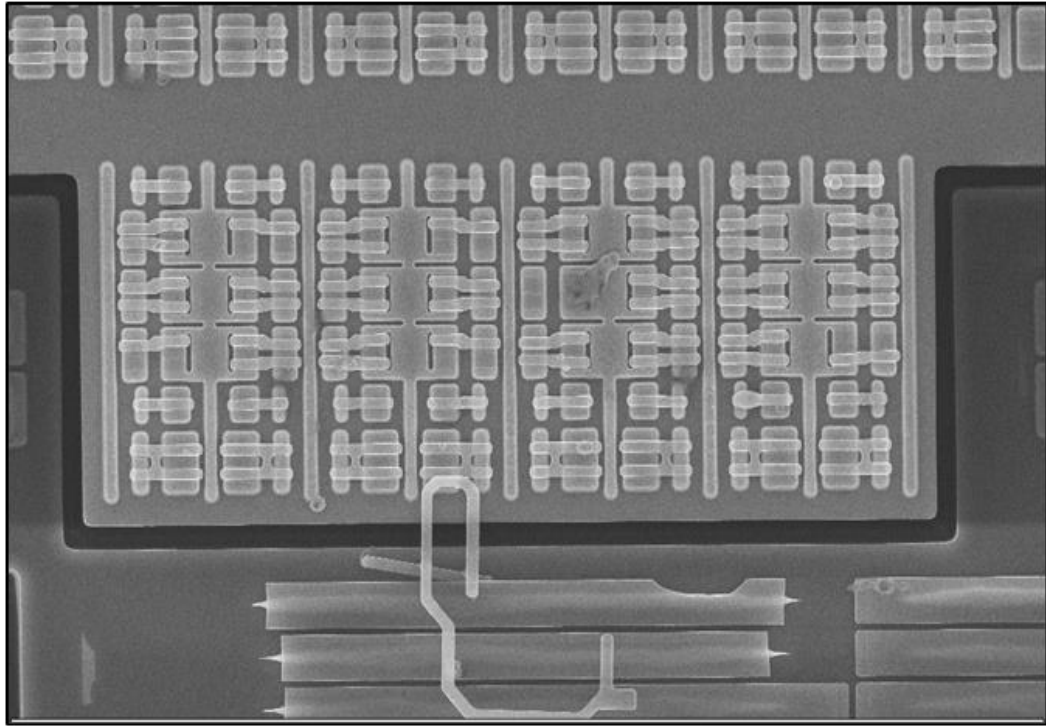


Figure 4.14: Polysilicon and oxides remain on top of silicon surface due to HF under-etch for Sample 1

The DOE findings stated that the best treatment to remove all oxide on active structures whereas preserve Top Silicon was 20% HF, 10 minutes HFT and 5 minutes SST. Since the immersion time is manual, and oxide layer thickness is varying based after parallel lapping manual settings, it is good to observe the sample on optical microscope every 5 minutes.

SEM images in Figure 4.15 shows a cross-section result of Sample 2 whereby HF etching stopped exactly before reaching bottom DTI trench. This profile is vital to hold the Top Silicon from peeling off during supersonic cleaning meanwhile oxides on Top Silicon surface is completely etched.

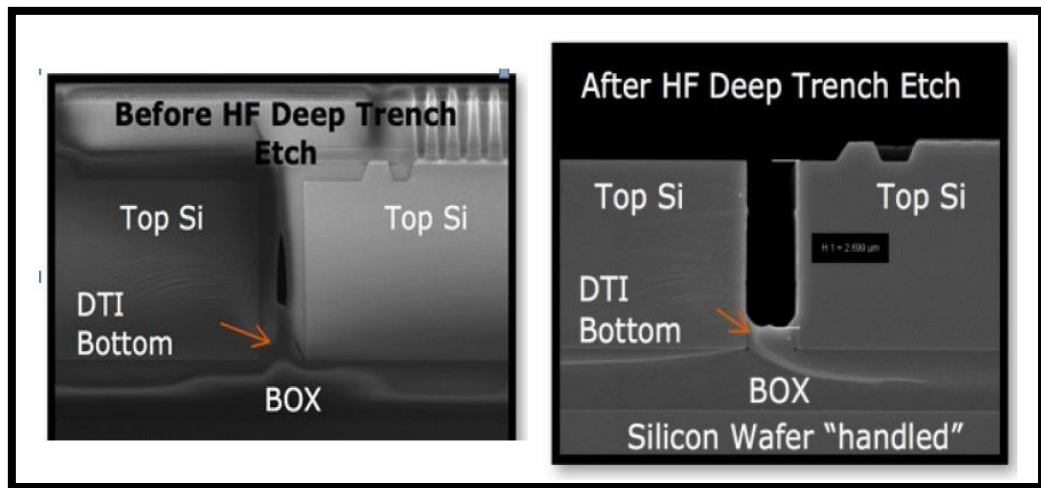


Figure 4.15: Sample 2, remaining BOX holds top silicon from peeled off/cracks

The proposed method to Delayer SOI by using a Combination of Parallel Lap Polishing and Diluted and Time Controlled Hydrofluoric Acid Etching proven to be a good, stable, repeatable delayering process for SOI wafer type. The most important contributions are the undamaged of SOI active structures, allowing a wide visibility observation of ROI. The clean active structure is crucial before being able to conduct investigation of substrate defect using Wright Etchant Solution. The result of sample immersion into Wright Etchant solution for 5 ~ 10 secs shown in Figure 4.16.

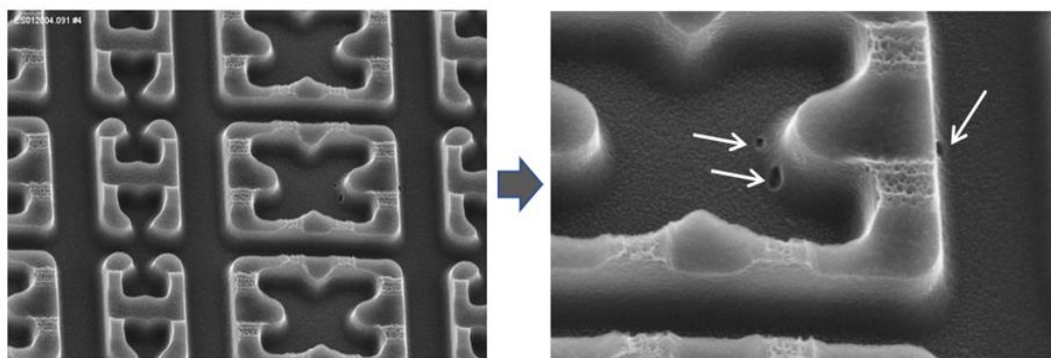


Figure 4.16: SEM titled images of an active pattern at cell area after immerse wright etchant solution for 5 seconds. The silicon defect appeared as holes (show by arrows)

As seen, the silicon defect appeared as holes. This shows that the active surface was clean and further analysis to check for substrate layer for COP, dislocation and HF defect using Wright Etchant can be done. Remaining other layers on top of active layer such as a thin nitride, oxide and metal prevent Wright Etchant to reveal defects in silicon wafer (Lim et al., 1998).

Besides enable to examining substrate defect, the proposed method to Delayer SOI by using a Combination of Parallel Lap Polishing and Diluted and Time Controlled Hydrofluoric Acid Etching also capable to uncover every layer in SOI die sample from after Passivation to Active DTI Layer. DTI layer is visible under optical microscope opens possibility to polish long and narrow structure using RAPH.

4.5 RAPH Prototypes Performance Evaluation Result and Discussion

Performance evaluation is to prove that RAPH is capable to polish in a straight angle which traditional Polisher Hand is not capable to perform.

4.6 RAPH's Prototype 'A' Weakness

Few issues were immersed while testing RAPH's Prototype A which are:

- a. Item Clamp Piston Head bigger than specification as shown in Figure 4.17

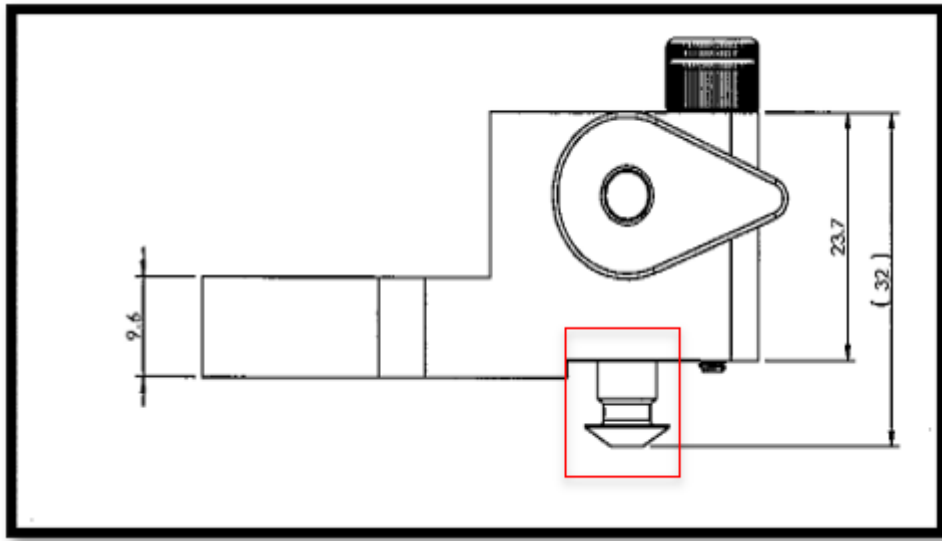


Figure 4.17: Clam piston head out of spec

- b. Item 2 - Locking Pin smaller than spec as shown in Figure 4.18

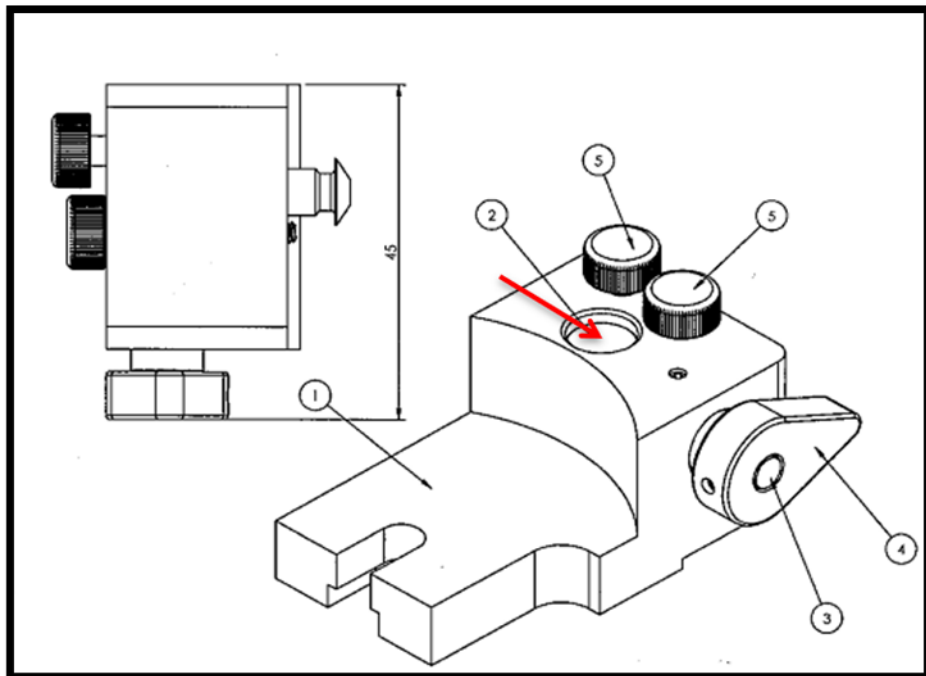


Figure 4.18: Locking pin – Item 2

c. Item 5 - Adjustment Screw when turn, it pushes the stage X, Y, and Z axis together which is not wanted.

Even if all out of specification item above were fixed and corrected, the polisher stage should only move X or Y. Z should remain still. Unfortunately for Prototype A, the Z axis movement is inevitable. Prototype A also failed during spinning platen test of 100 rpm, where polisher stage pulled out from Prototype A polisher hand.

The unfirmed polisher stage during mounting also caused issue. The major issue of Prototype A was it not able to lock Z-Axis while adjustment been made for X or Y Axis. With those weaknesses addressed, Prototype B had been invented and been tested.

4.7 RAPH's Prototype B Used for Evaluation

The RAPH is a tool to be attached to the rotary polishers in the FA lab. It is meant to solve a long-standing problem using polishing stages in the lab, namely polishing wafer samples without the sample polished edge being skewed away from the normal. Conventionally, polisher stages are waxed, heated up, then the samples are placed on the stage and the wax is left to cool. If the polished edge is misaligned, operators must reheat the stage, realign the sample, then polish again and check that the polished edge is aligned. The RAPH was designed to reduce such tedium. Z groove is designed to lock Z-Axis and allow X and Y axis to move so that control focused on straightness X and Y-Axis. There's no slanting Z-Axis which means no sample Z-Axis tapering happens during polishing in X and Y-Axis. Z groove design shows in Figure 4.19.

It uses a system of two micrometer screws to adjust the tilt of the polishing sample and thereby the wafer sample to be polished, with the goal of achieving a straight and normal

polish edge. RAPH's Prototype B photos in Figure 4.19, Figure 4.20, Figure 4.21, Figure 4.22 and Figure 4.23.

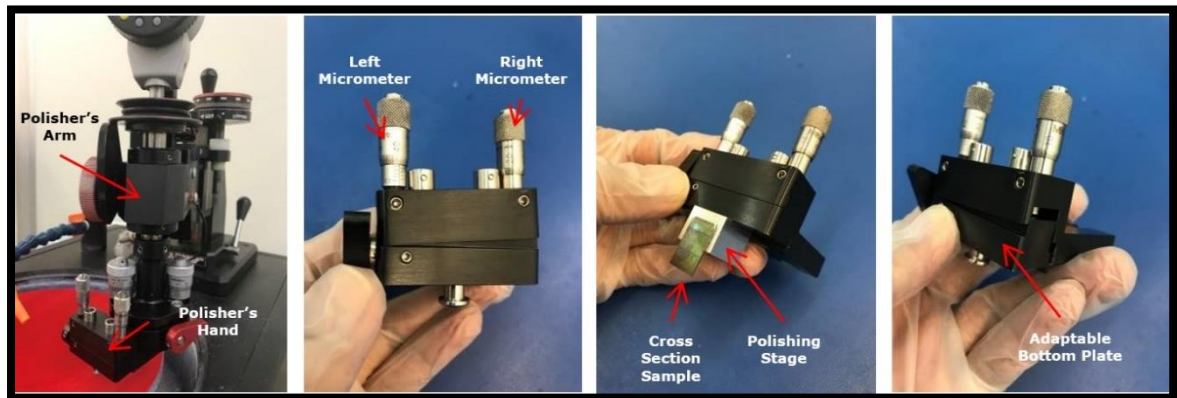


Figure 4.19: RAPH's prototype B



Figure 4.20: RAPH's prototype B 3D view

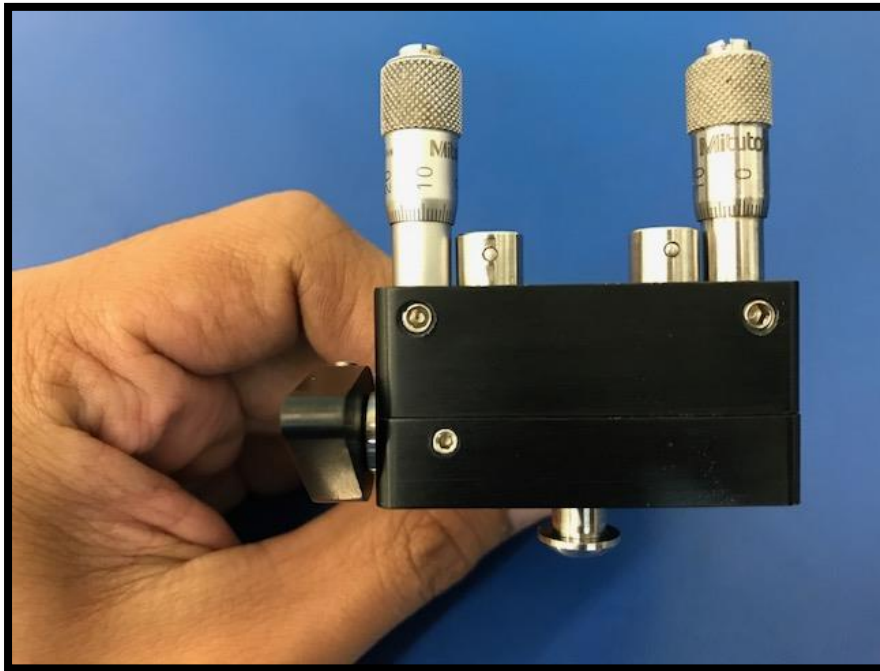


Figure 4.21: RAPH's prototype B front view



Figure 4.22: RAPH's prototype B side view



Figure 4.23: RAPH's prototype B top view

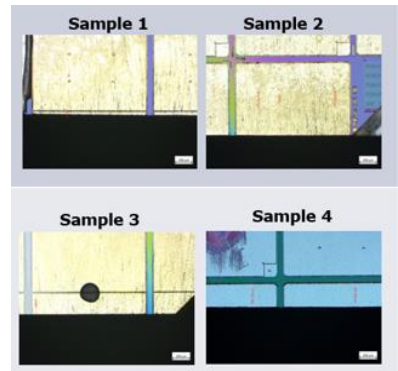
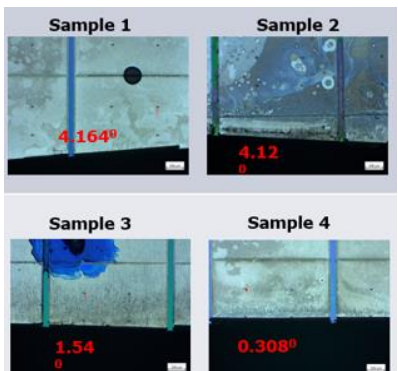
The performance evaluation for RAPH's Prototype B includes:

- a. RAPH Adjustment Straightness test
- b. RAPH Unadjusted versus Adjusted angle variance
- c. Polisher Stage Mount-unmount on RAPH Consistency test
- d. Image Quality test as compared with traditional Polisher Hand
- e. RAPH behaviour during high-speed platen spinning test

4.8 RAPH Adjustment Straightness Test Results

Straightness Test was conducted to compare traditional manual alignment method and RAPS Method straightness towards target. Result from optical microscope angle measurement shows straight polishing angle of RAPH as compared to manual alignment where very straight (00) can be achieved using RAPH Fixture.

Table 4.2: Straightness test conducted to compare traditional manual alignment method and RAPH method straightness.

Alignment with RAPH	Average Angle Variance	Manual Alignment	Average Angle Variance
	0° 0°		4.14° 1°

This test measures how straight a polished wafer edge is after the RAPH screws have been adjusted. The value can be measured by the optical microscope software. In practice, after RAPH adjustment, a polished wafer edge should be skewed at least no more than 0.15 degrees from a right angle. It is highly recommended to polish wafer edges up to at least the 0.5 μm grade polishing disc film before measuring wafer edge angles, to ensure a sharp angle in the microscope view for more precise angle measurements.

4.8.1 Tabulated Straightness Test Results and Graphical Summaries

Table 4.3: The wafer sample edge angles measured before and after the RAPH has been adjusted.

Sample	Angle 1	Skew 1	Height Adjustment (adj)	Angle 2	Skew 2
1	88.105	-1.895	-1.14	90.107	0.0107
2	89.715	-0.285	-0.17	89.747	-0.253
3	89.899	-0.101	-0.06	90.093	0.093
4	91.106	1.106	0.67	90.100	0.100
5	88.888	-1.112	-0.67	90.098	0.098
6	88.762	-1.238	-0.75	90.040	0.040
7	89.693	-0.307	-0.18	90.125	0.125
8	88.041	-1.959	-1.18	90.093	0.093
9	87.000	-3.000	-1.81	90.465	0.465
10	88.007	-1.993	-1.20	89.994	-0.006
Average	88.922	-1.078	-0.65	90.086	0.086
Standard Deviation	1.200	1.200	0.75	0.174	0.174

Skew 2 shows how much the wafer angle deviates from perfect right angle, and it should be as close to 0 as possible.

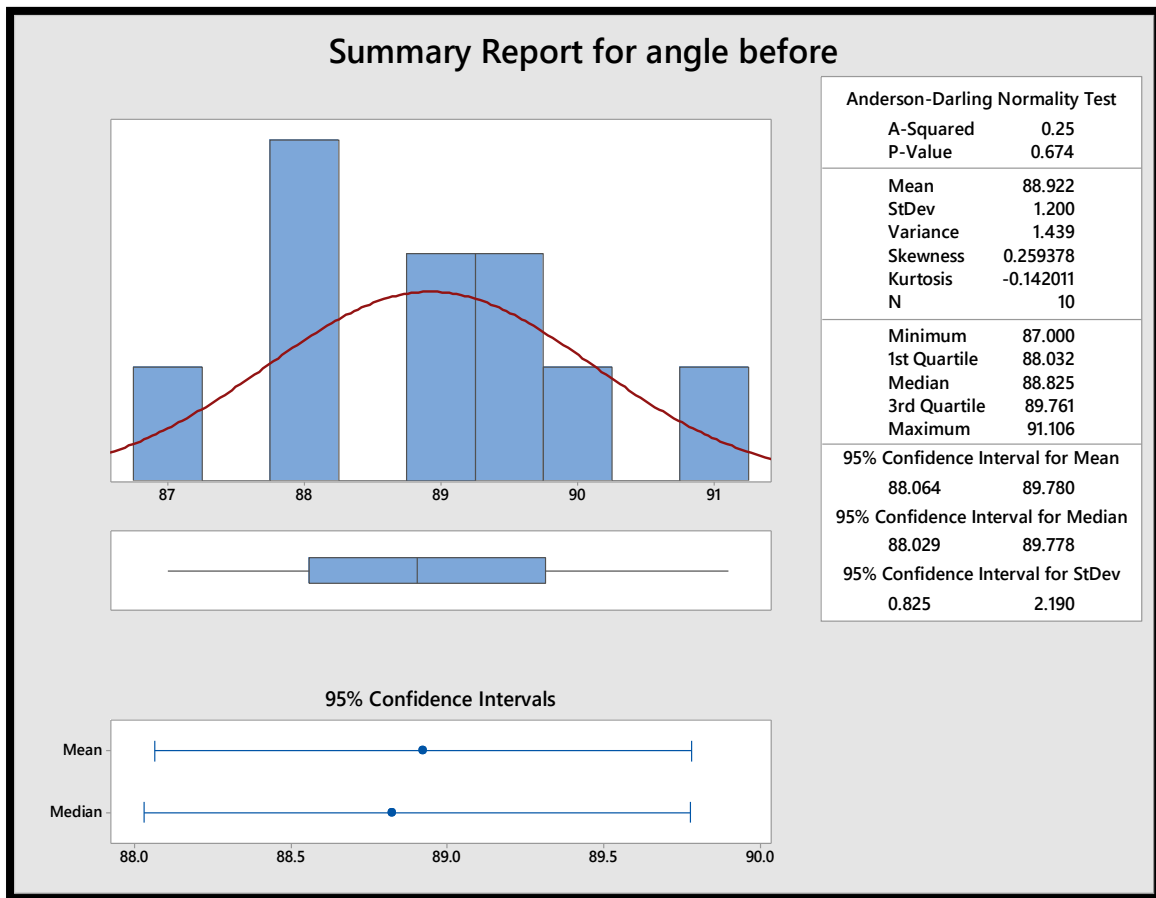


Figure 4.24: Graphical summary of wafer edge angles before RAPH adjustment.

Figure 4.24 shows the graphical summary of wafer edge angles before RAPH adjustment. The mean angle is 88.922 degrees, with a standard deviation of 1.2.

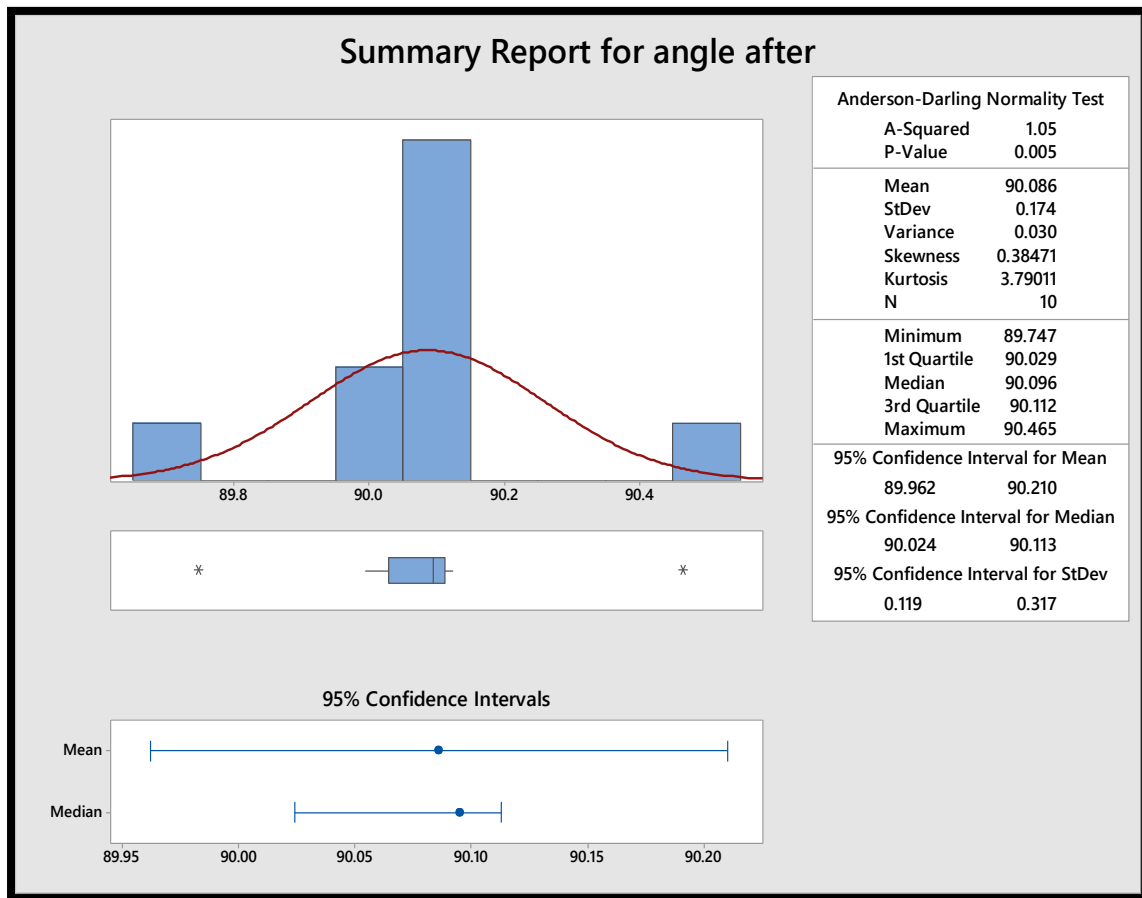


Figure 4.25: Graphical statistical summary of wafer edge angles after RAPH adjustment.

Figure 4.24 shows the graphical statistical summary of wafer edge angles after RAPH adjustment. This time the mean is 90.086 degrees, and the standard deviation is 0.174. The values are closer to the target of 90 degrees, and they are more tightly clustered.

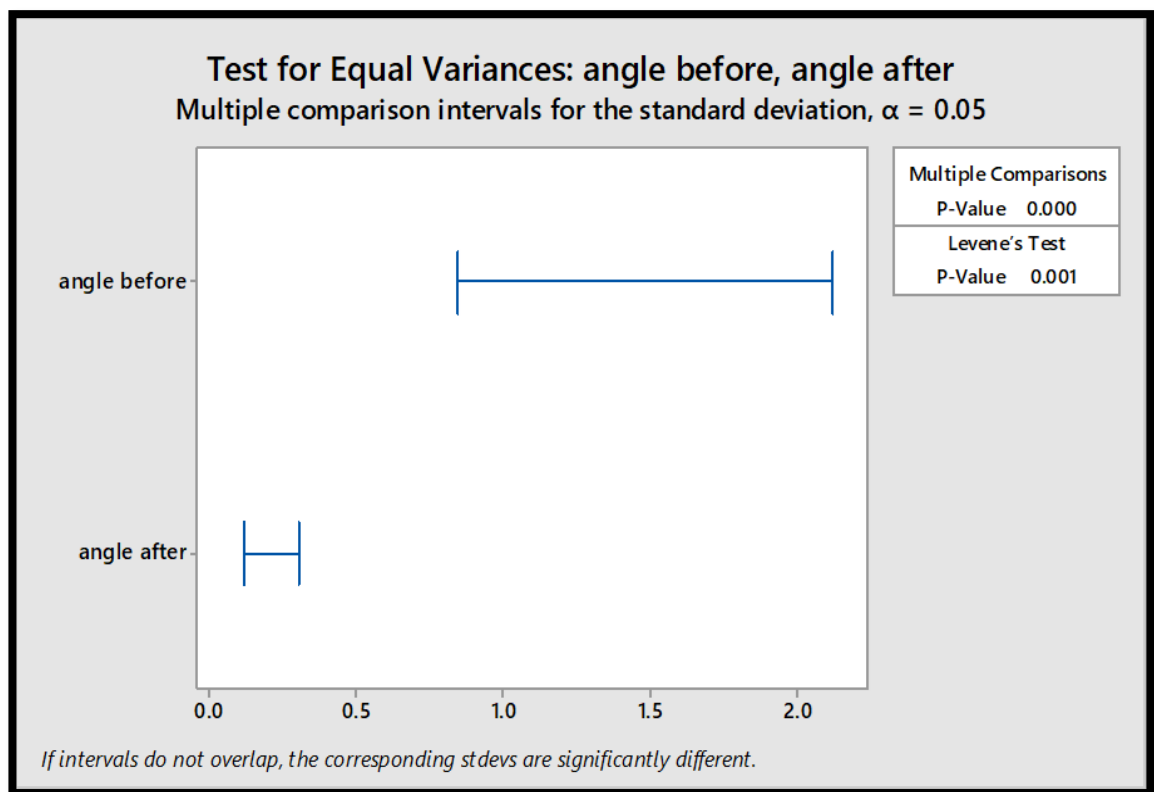


Figure 4.26: Equal variances test for wafer edge angles before and after RAPH adjustment.

Figure 4.26 shows the qual variances test for wafer edge angles before and after RAPH adjustment. The variance intervals do not overlap; therefore, the variances are significantly different.

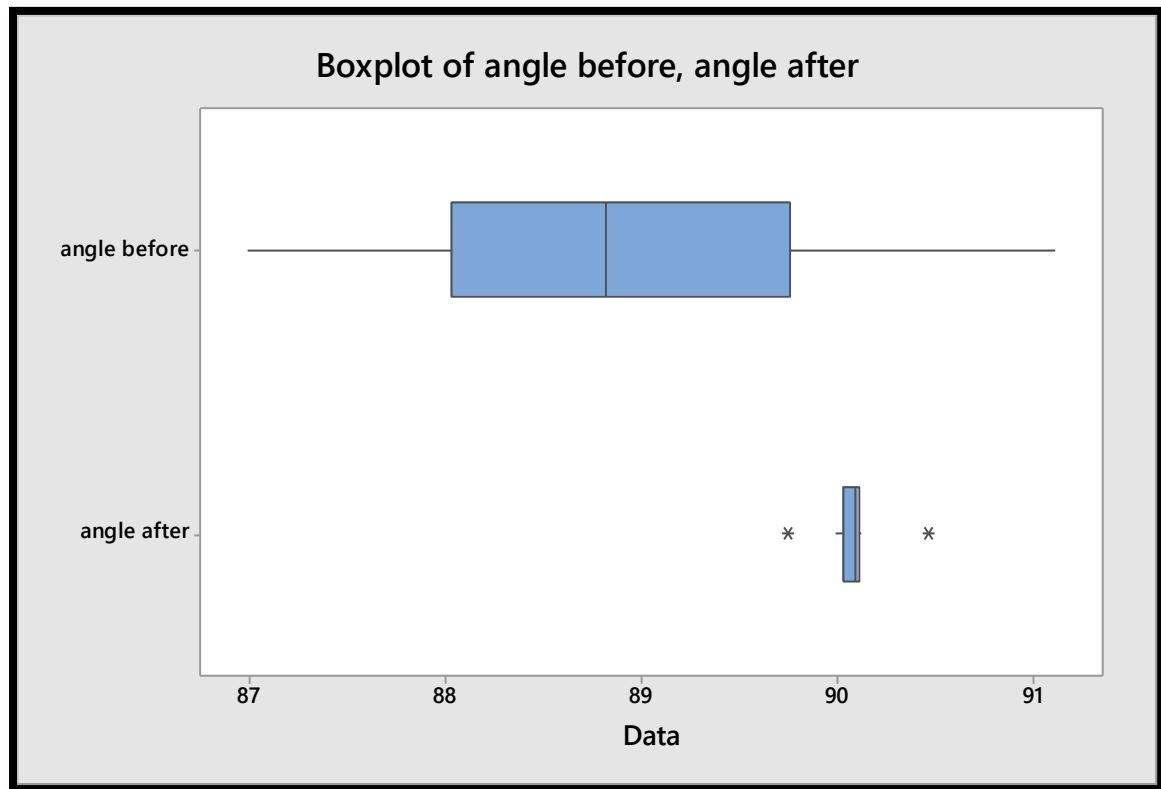


Figure 4.27: Boxplot of angles before and after RAPH adjustment.

Figure 4.27 shows the boxplot of angles before and after RAPH adjustment. The angles after RAPH adjustment are much more tightly distributed than before RAPH adjustment, though there exist two outlier values.

4.8.2 Discussions on Adjustment Straightness Test Results

This experiment focuses on the mean straightness of wafer edge polishing, expressed in terms of the angle between the polished wafer edge and the vertically oriented features on the wafer sample. From the statistical summaries in the previous section, wafer edge angles before RAPH adjustment have relatively large spread (variance), which is indicative of the highly varying wafer edge angles obtained from pasting the wafer sample on the polisher stage manually. On the other hand, the wafer edge angles after RAPH adjustment are more

tightly clustered, which is indicative of the RAPH's capability to adjust wafer edge angles to close to right angle. The after-adjustment angles are tightly distributed around the mean of 90.089 degrees, which is close to 90 degrees, though there are also two outliers, indicating again that the RAPH adjustment successfully straightens wafer edge angles.

4.9 RAPH Unadjusted versus Adjusted Angle Variance Result

The wafer edge angles obtained after repeatedly polishing one wafer sample without adjusting the RAPH and polishing another sample with the RAPH adjusted such that the end result is a polish angle close to 90 degrees. In this test, the important parameter is the variance in the angles obtained, here expressed in terms of the standard deviation. The tabulated result shows in Table 4.4 in next page.

Table 4.4: Tabulated result of RAPH unadjusted versus adjusted angle variance

Run	Unadjusted RAPH edge angle	Adjusted RAPH edge angle
1	89.733	89.957
2	89.891	89.825
3	89.787	89.922
4	89.700	89.932
5	89.775	89.828
6	89.813	90.083
7	89.895	90.062
8	89.931	90.003
9	89.915	89.855
10	89.896	90.045
11	89.874	90.064
12	89.859	90.150
13	89.679	90.098
14	89.863	90.099
15	89.969	90.087
Average	89.825	90.001
Standard Deviation	0.096	0.107

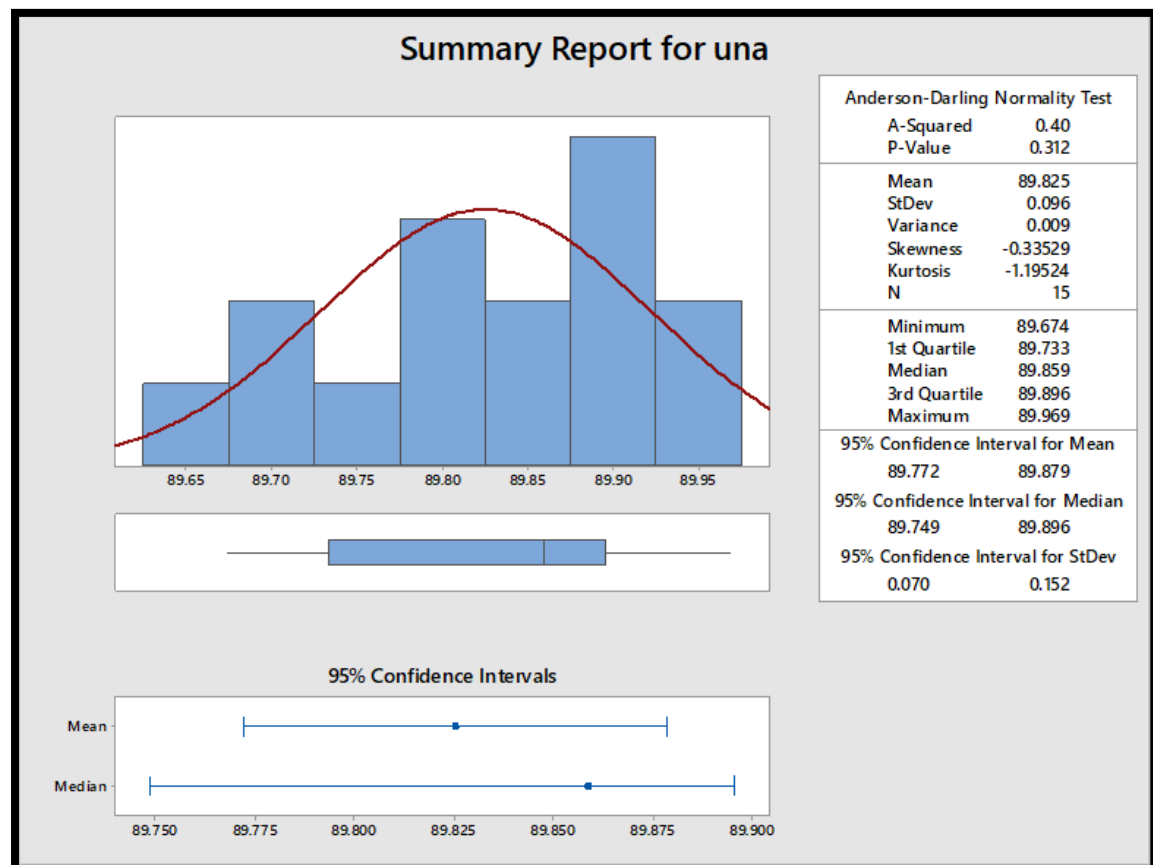


Figure 4.28: Graphical statistical summary of wafer edge angles after repeated polishing of a single wafer sample, without RAPH adjustment.

Figure 4.28 shows the graphical statistical summary of wafer edge angles after repeated polishing of a single wafer sample, without RAPH adjustment.

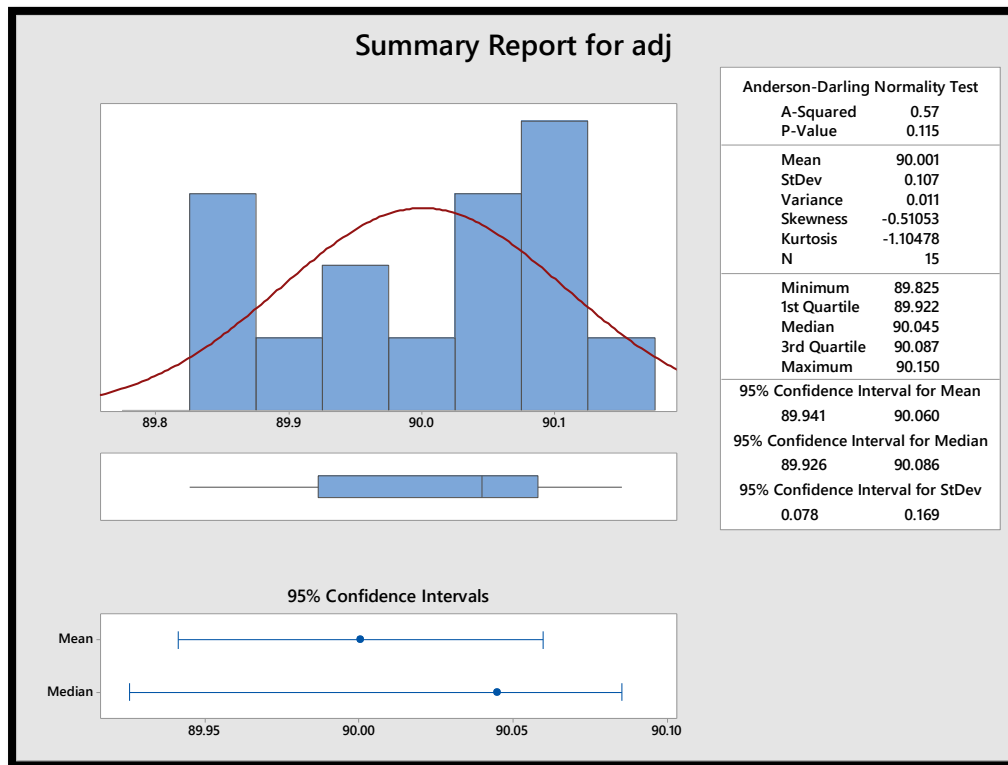


Figure 4.29: Graphical statistical summary of wafer edge angles after repeated polishing of another single wafer sample, this time with RAPH adjustment.

Figure 4.29 shows the graphical statistical summary of wafer edge angles after repeated polishing of another single wafer sample, this time with RAPH adjustment. Note that the standard deviation here is close to the unadjusted sample in Figure 2.8.

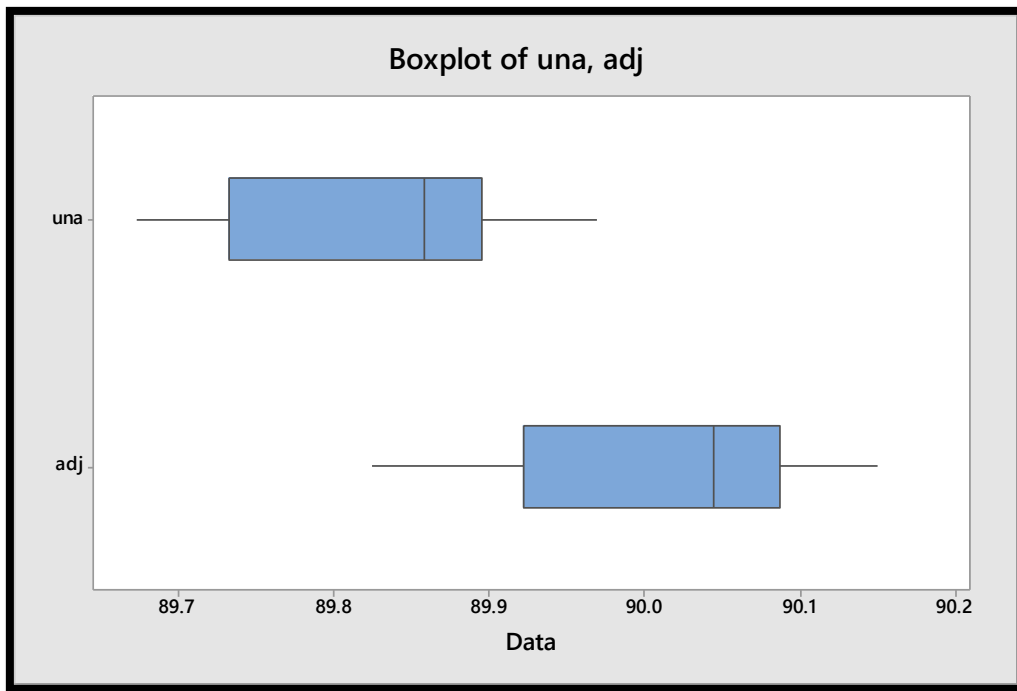


Figure 4.30: Boxplot comparing wafer edge angles without RAPH adjustment (una) with angles after RAPH adjustment (adj).

Figure 4.30 shows the boxplot comparing wafer edge angles without RAPH adjustment (una) with angles after RAPH adjustment (adj). Note that the boxes have similar width, which indicates similar variance.

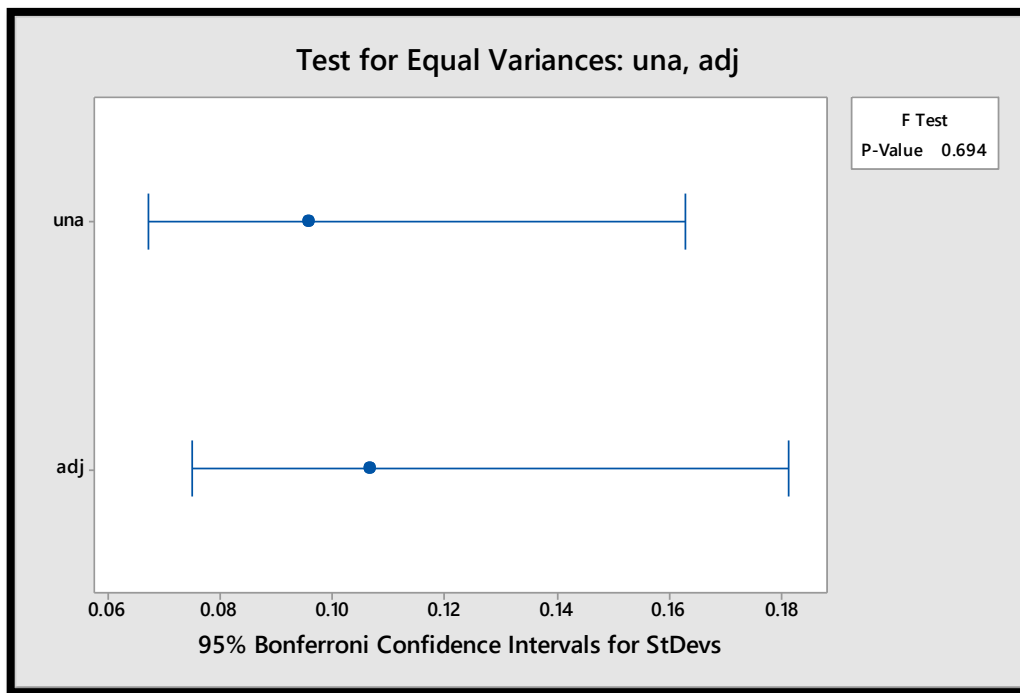


Figure 4.31: The test for equal variances.

Figure 4.31 shows the test for equal variances that the confidence intervals for standard deviations between unadjusted and adjusted wafer edge angles overlap significantly with a P-value greater than 0.05, such that their standard deviations are significantly similar.

4.9.1 Discussions on RAPH Unadjusted versus Adjusted Angle Variance Test Result

This experiment was analysed using analysis of variance ANOVA, since the comparison of standard deviances and hence wafer edge consistency is the key point here. From the box plots, while the means of both samples differ significantly, as expected when the RAPH is adjusted vs not adjusted, the boxes themselves are nearly the same length, from which it can be inferred that the standard deviations are similar. This is further confirmed by the ANOVA test of equal variances plot, where the interval heavily overlaps and the P-value of 0.694 is exceedingly higher than alpha of 0.05.

It can be inferred here then that the wafer edge angles are consistent when the RAPH is at 0 adjustment and also when it is adjusted. Thus, the RAPH is stable at any micrometre screw adjustment setting. The most likely sources of variation here are 1. slight variations from repeatedly adjusting the micrometre screws and 2. measurement errors when manually measuring the angles.

4.10 Mount-unmount Consistency Test Result

This test determines how consistent the polished wafer edge angles are when the polisher stage is mounted and unmounted on the RAPH repeatedly. The result of mount-unmount polisher stage on RAPH and Regular Polisher Hand (Regular) depicted in Table 4.5.

Table 4.5: Wafer edge angles after the samples are repeatedly unmounted and then mounted again repeatedly on to the polisher spindle, both with and without RAPH adjustment.

Run	RAPH Angle	Regular Angle
1	88.925	89.729
2	88.939	89.733
3	88.906	89.717
4	88.948	89.739
5	88.992	89.641
6	88.952	89.784
7	88.904	89.723
8	88.952	89.703
Average	88.940	89.721
Standard Deviation	0.029	0.040

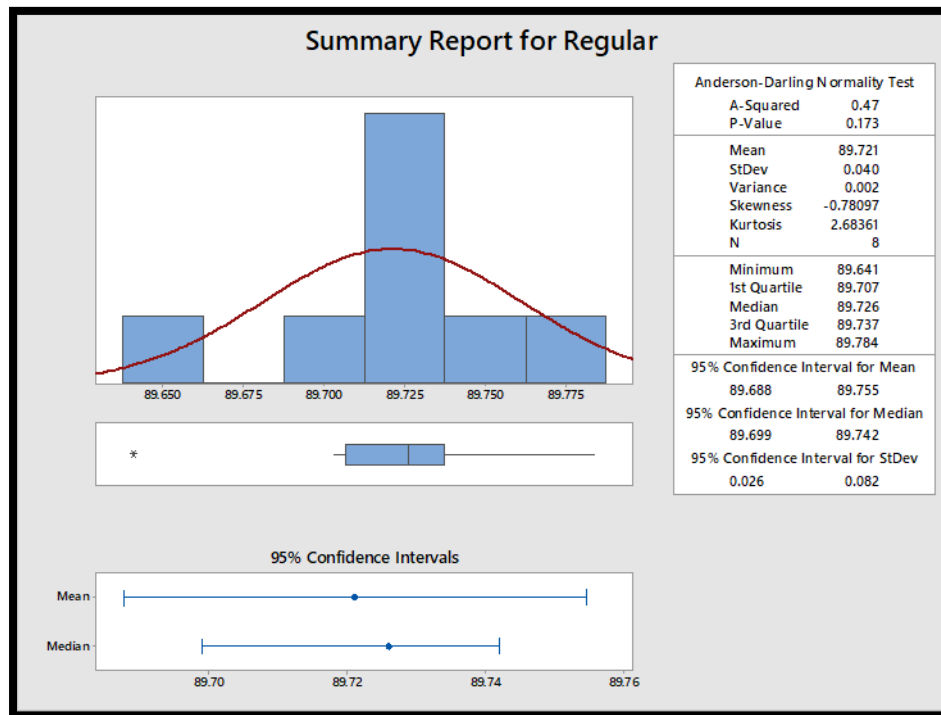


Figure 4.32: Statistic graphical summary of wafer edge angles after the sample is repeatedly unmounted and mounted on the polisher spindle, without RAPH adjustment.

Figure 4.32 shows the statistic graphical summary of wafer edge angles after the sample is repeatedly unmounted and mounted on the polisher spindle, without RAPH adjustment. The important statistical parameter in this test, the standard deviation, is 0.04.

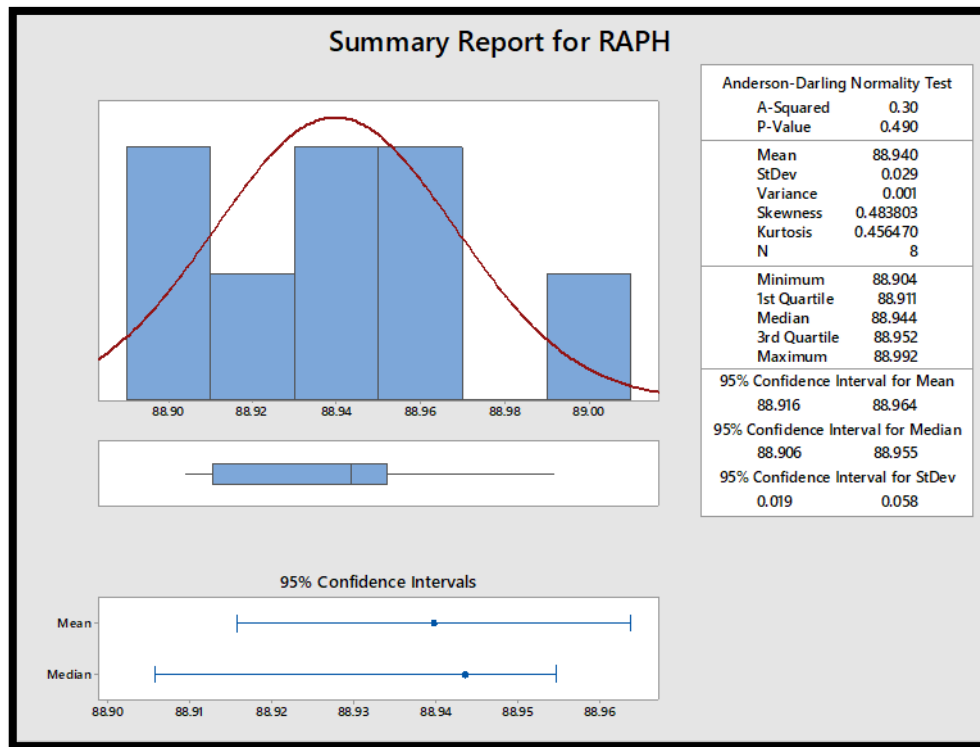


Figure 4.33: Statistic graphical summary of wafer edge angles after the sample is repeatedly unmounted and mounted on the polisher spindle, with RAPH adjustment.

Figure 4.33 shows the statistic graphical summary of wafer edge angles after the sample is repeatedly unmounted and mounted on the polisher spindle, with RAPH adjustment. The standard deviation is 0.029.

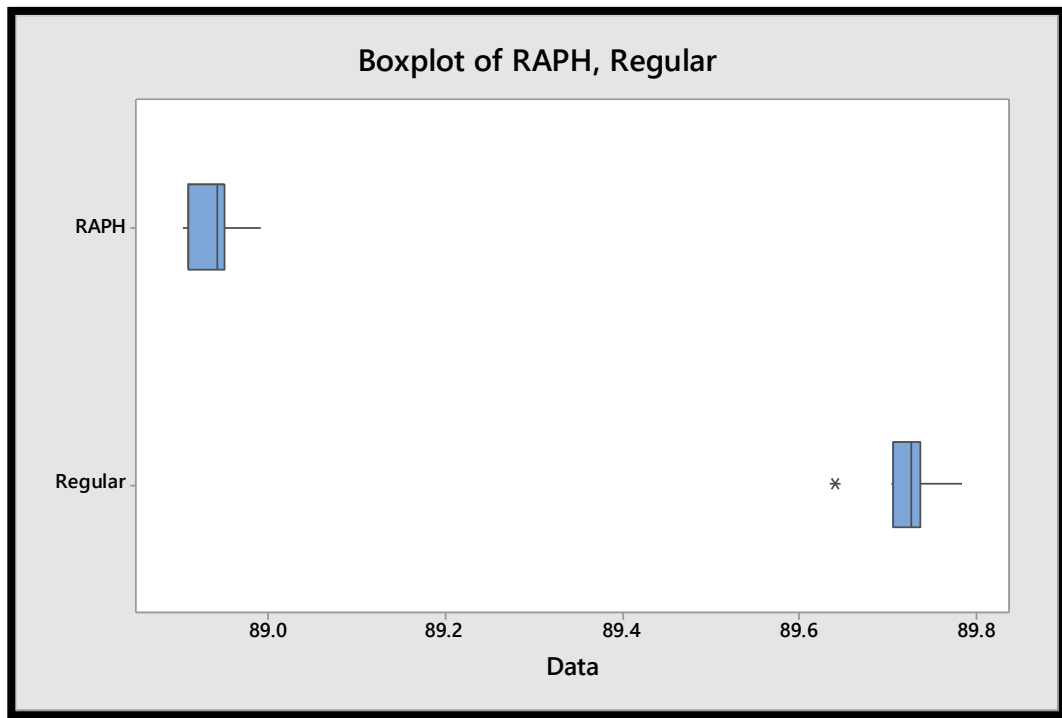


Figure 4.34: The boxplot of unmount-mount test wafer edge angles, RAPH versus Regular Polisher Hand (Regular).

Figure 4.34 shows the boxplot of unmount-mount test wafer edge angles, RAPH versus Regular Polisher Hand (Regular). Regular shows an outlier value.

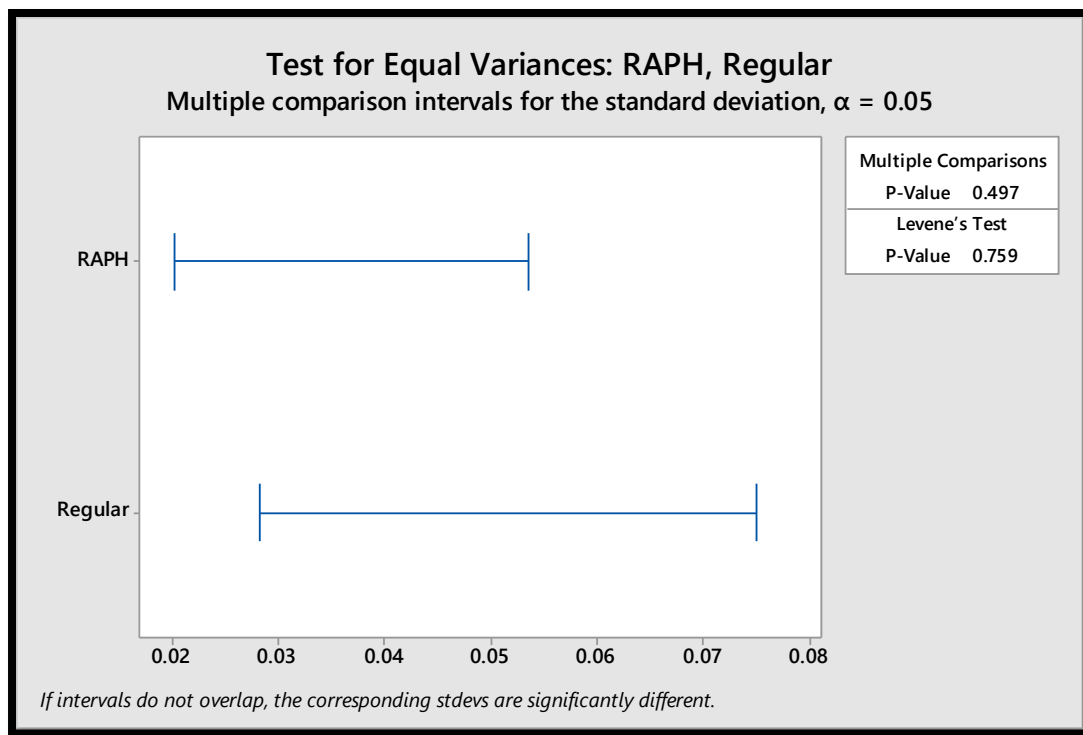


Figure 4.35: The equal variances test shows significant overlap between the confidence intervals for the standard deviation of wafer edge angles.

Figure 4.35: The equal variances test shows significant overlap between the confidence intervals for the standard deviation of wafer edge angles. Given that the P-values exceed 0.05, it can be inferred that the standard deviations are not significantly different.

4.10.1 Discussions on Mount-unmount Consistency Test

Using the multiple-comparisons P-value, the obtained P-value for the test of equal variances between RAPH angles and regular hand angles is 0.497, about 10 times the significance level $\alpha=0.05$. This means that the possibility of the variances of RAPH vs Regular Polisher Hand angles being significantly different can be rejected.

In other words, both types of polisher hands deliver consistent edge polish angles when the wafer/die samples are repeatedly mounted and unmounted on the polisher hands.

The angle does not deviate too far. This also implies that the RAPH is equal to the regular hand when it comes to consistent edge polish angles, with the added advantage of being able to be adjusted to a perpendicular angle. Given the additional capabilities of the RAPH, it is a significant upgrade over a regular polisher hand.

4.11 Image Quality Test

SEM was employed to check the surface profile quality after using RAPH and compare with the traditional Polisher stage. This test basically to check whether RAPH's image quality is comparable or not compared to Traditional Polisher Hand. 8 polished samples were used. 4 samples polished using RAPH fixture and the other 4 samples polished used Traditional Polisher Hand Fixture. These samples then undergo chemical treatment using Buffered Oxide Etch (BHF) 10:1 for 8 secs. Once dried, these samples been sputtered with Platinum coating to enhanced conductivity before putting into Scanning Electron Microscopy (SEM) for test analysis. Figure 4.36 shows a comparable result of RAPH versus Traditional Polisher Hand in term of image quality obtain form the polishing surface profile.

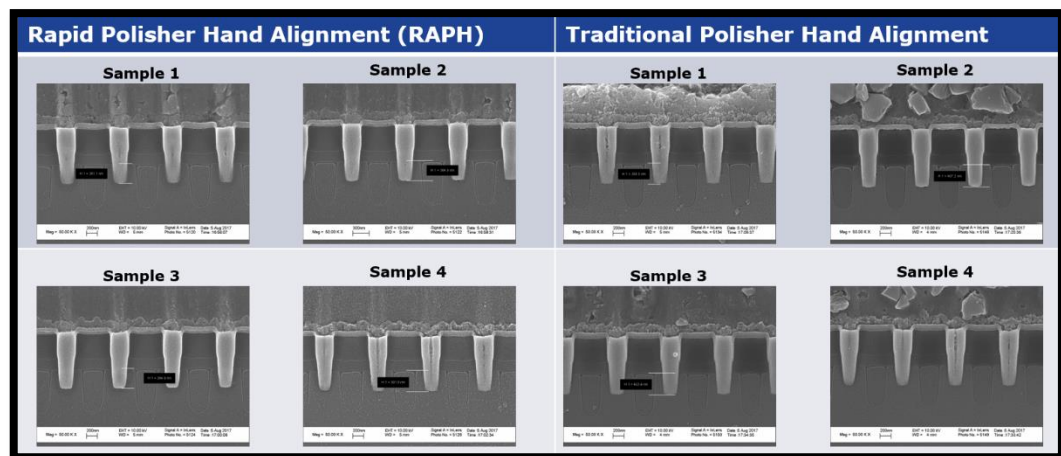


Figure 4.36: SEM result shows a comparable polishing quality of RAPH method as compared to traditional manual alignment

4.12 RAPH Behaviour during High-Speed Platen Spinning Test Result

Table 4.6: RAPH Prototype B is very stable during speed test at 600 rpm polishing.

Normal operation speed is 200~250 rpm.

Pad Rotary Speed (RPM)	Base Plate Vibration	Locking Slip	Sample is Polished	Stage Vibration Observation	Bottom Plate Observation
100	Normal	Firmed	Yes	Normal	Firm
200	Normal	Firmed	Yes	Normal	Firm
300	Normal	Firmed	Yes	Normal	Firm
400	Normal	Firmed	Yes	Normal	Firm
500	Normal	Firmed	Yes	Normal	Firm
600	Normal	Firmed	Yes	Normal	Firm

Vibration analysis: Observation at RAPH base (Part 1), Locking Slip and bottom plate and other parts of the machine were recorded. The test operation ran for about 8 hours where the spindle speed was set to 6 speeds. Speeds 1=100, speeds 2=200, speeds 3=300, speeds 4=400, speeds 5=500rpm and speeds 6=600rpm.

The result from the observations on the test operation found no abnormal vibration or RAPH's parts loose found (Firm Condition). All parts observed to be working properly and the cross-section sample polishing process was succeeded.

The maximum of 600 rpm in normal operation period proved that RAPH's stability is comparable with Regular Polisher Hand.

4.13 Method Application and Result

The RAPH precision alignment method is applicable to all structures inside integrated circuit which has very long and at the same time the width is very narrow. This time a very long and narrow Deep Trench Isolation (DTI) selected as target.

The only possible method in market to cross-section this very long and narrow structure is by using Plasma Focus Ion Beam (PFIB). However, the PFIB is too expensive. The cost to own PFIB is around USD 2 Million. Now the challenge is to use RAPH to polish in the middle of seam line inside DTI line.

4.13.1 Polishing Very Long and Narrow DTI Line

The RAPH capability and accuracy test was conducted using selected long and narrow DTI line in which length (from Start Point to End Point) = 835 μm and very narrow width = 0.942 μm as shown in Figure 4.37 and 4.38. The test target was to polish in the middle of DTI seam as shown in Figure 4.39.

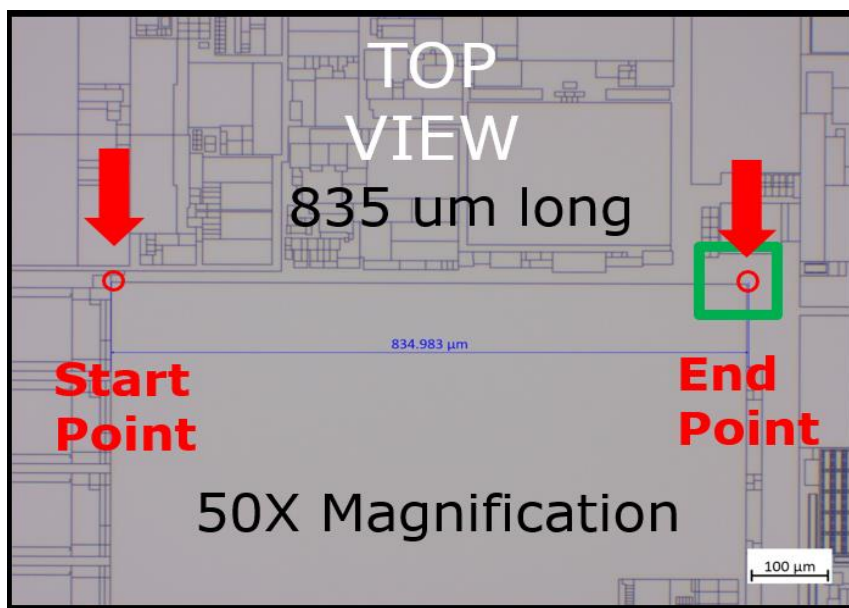


Figure 4.37: Top view optical microscope of 835 μm long DTI line with 0.942 μm width

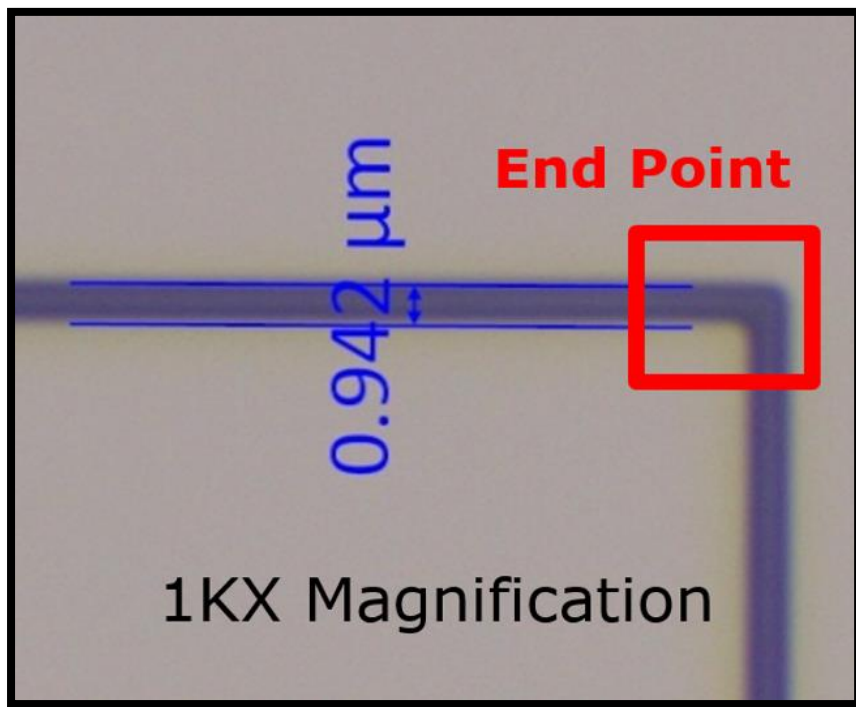


Figure 4.38: Top view optical microscope with 1000x. Measurement of DTI Width = 0.942μm

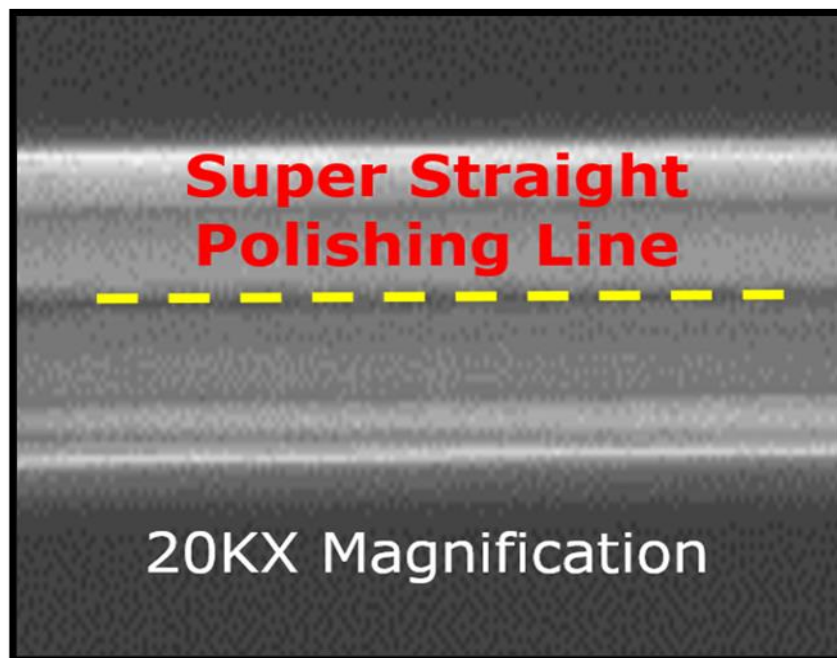


Figure 4.39: Middle seam of DTI line which RAPH is tested to polish from start to end point (polishing line is indicated with yellow dash line)

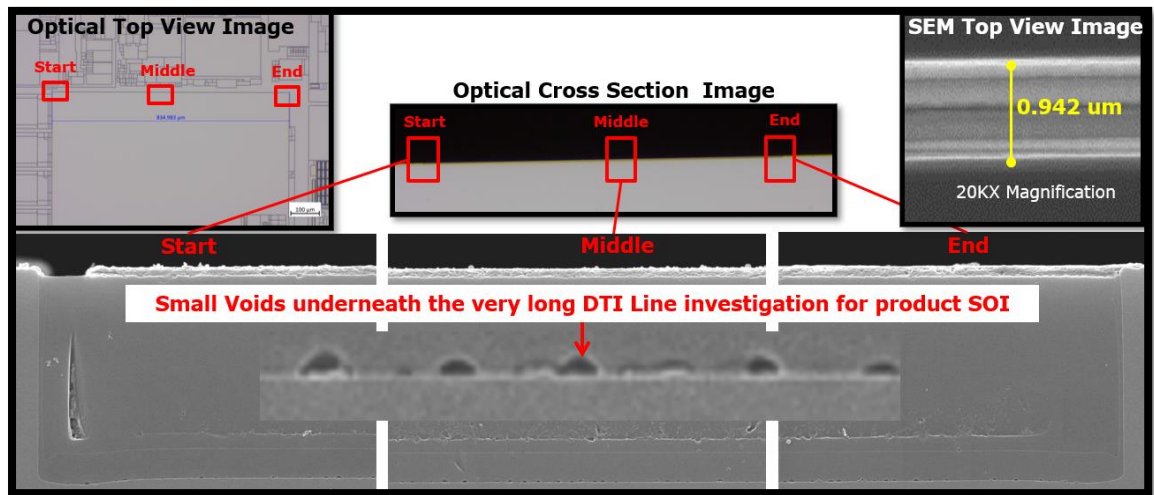


Figure 4.40: DTI voids defect was able to be observed below trench. Method used: RAPH advanced polishing

Result: From the Optical and Scanning Electron Microscope Images (SEM), it was observed that RAPH is capable to polish in the middle of very long ISO DTI Line (835um long and 0.942 um width) from start to end in Figure 4.40. Observation in SEM Cross-sectioning methodology to check small voids underneath DTI trench for very long Isolated DTI line is now possible with the help of Rapid Alignment Polisher Hand (RAPH) fixture. The Conventional Polisher Alignment method unable to reach this precision. Thanks to RAPH precise multimeter left and right tuning and Z Groove design.

4.14 RAPH Capability

The Rapid Adjust Polisher Hand, RAPH, extends the utility of the Allied Multi-Prep Polisher apparatus beyond its limitation by allowing very long structures with very narrow width to be polished, for example the long DTI lines on wafer samples. One just must measure the wafer edge angle when the wafer sample is polished without RAPH adjustment, then adjust the RAPH according to the equation $D_h = 34.5 \tan (\theta - 90)$, where θ is the measured wafer edge angle.

4.14.1 Comparison of Conventional Polisher Sample Alignment versus RAPH Sample Alignment Capability

Table 4.7: Capability of rapid alignment polisher' hand (RAPH) method alignment to cut a very long DTI line with a very narrow width.

Method	Duration to get Acceptable Straight Polish/Cleave /Mill (Time)	Cut a Very Long DTI Line (0.8mm) with a Very Narrow Width (0.9µm)	Polish/Cleave/Mill DTI Area Coverage (in %)	Super Straight Polish/Cleave /Mill (00)
Rapid Alignment Polisher Hand (RAPH)	Average 5 minutes	Possible	100% (Smooth surface)	Capable
Conventional/Regular Polisher Alignment method	Average = 1 hour	Not Possible	30%(Some area over polished)	Not Capable
SELA Micro-cleaving	NA	Not Possible	20%(Some area with surface crack observed)	Not Capable
Gallium Focus Ion Beam (FIB) Milling	Less than 1 minutes	Not Efficient and very costly	0.1% (Gallium FIB not efficient for milling area larger than 10µm)	Capable

Duration to get a Straight Polish/Mill/Cleave in Table 4.7 is a time to obtain an acceptable straightness for normal cross-section analysis. The Super Straight (0⁰) polishing is a capability that require to polish long and narrow structure such as a Very Long DTI Line with a Very Narrow Width. The Polish/Mill/Cleave DTI Area Percentage (%) Coverage was

based on 835 μ m long DTI Line from start point to end point. 100% means all structure's surface area is polished.

As seen in Table 4.7, the Rapid Alignment Polisher Hand (RAPH) method alignment fulfilled 4 out of 4 capabilities requirement. RAPH able to perform faster polishing as compared to Traditional Polisher Hand. RAPH also capable to cut or polish very long and narrow structure as RAPH capable to be tunned until achieved Super Straight (0^0) line polishing. In addition, RAPH also capable to polish and covered a 100% target surface area during the alignment capability test.

4.15 RAPH Accuracy

The RAPH makes it possible to relatively quickly adjust wafer edge cross-sectioning angle to achieve a 90-degree polish angle with the Allied Multi-Prep Polisher machine, in a way that Conventional Polisher Hand cannot.

According to the adjustment straightness test, the RAPH can achieve a 90-degree cross-sectioning angle, with a standard deviation of 0.174 degrees, compared to the standard deviation of 1.2 degrees while using the conventional polisher hand. Further variance tests also lend evidence to the RAPH's capability for consistent 90-degree polishes, even when the wafer sample is repeatedly mounted to and unmounted from the polisher machine, for example when one wants to change the polisher pad films to achieve finer cross-section polishes.

In summary, the RAPH is capable of accurate and precise cross-section polishing of wafer samples. Rapid Alignment Polisher's Hand (RAPH) made a Super Straight (0^0) polishing possible for Allied Multi-Prep Polisher machine. This can be proven during

investigation of small voids underneath very long with very narrow DTI line in Figure 4.40 (previous page) as the Conventional Polisher Hand unable to achieve this level of accuracy.

4.16 RAPH Productivity

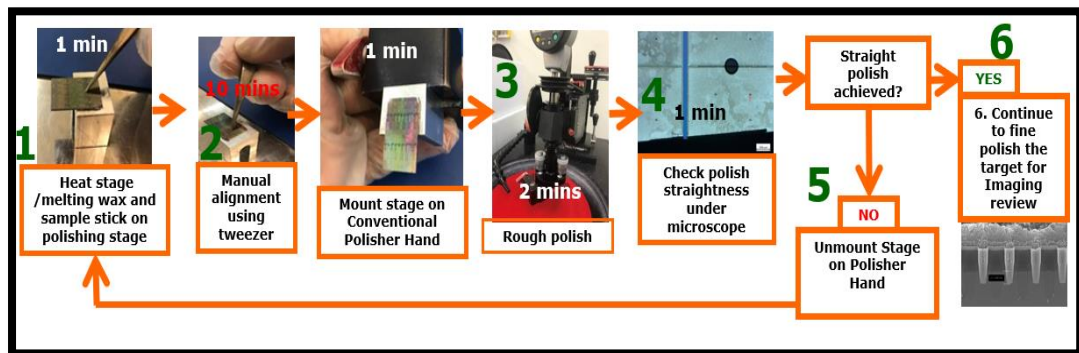


Figure 4.41: Conventional/regular polisher hand cross-sectioning step flow

Figure 4.41 shows the conventional/regular polisher hand cross-sectioning step flow. A Conventional Polisher Hand Requires to repeat Step 1-2-3-4 for at least 5 Cycles to get acceptable straight polishing. Thus, it took an average 1 hour to achieve acceptable straight polishing line alignment. Super straight polishing (0^0) is not possible using manual alignment.

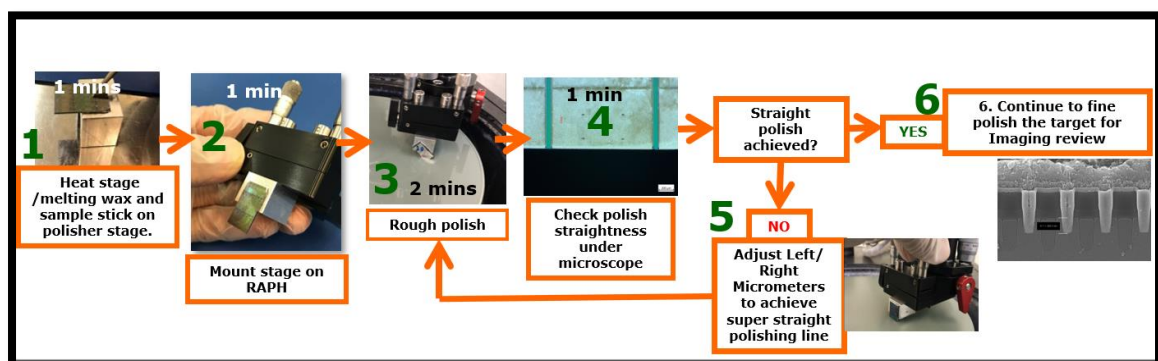


Figure 4.42: Rapid alignment polisher hand cross-sectioning step flow

Figure 4.42 shows the rapid alignment polisher hand cross-sectioning step flow. Took average 5 minutes to achieve acceptable straight polishing line and 10 minutes for a Super Straight Polishing Line (0^0). In average, only need to repeat Step 3-4 at least 2 Cycles to get acceptable straight polishing line. By using the RAPH, it takes on average a 12 times faster rate to perform sample alignment for cross-section analysis compared to Conventional Polisher Hands to achieve acceptable straight polishing line.

The RAPH can thus potentially save 55 minutes on the Failure Analysis of a cross-sectional wafer sample analysis, allowing the failure analysis job to progress and be finished at a faster rate, such that either a new job can be commenced faster, or give the failure analysis engineer time for a break to improve their productivity. In addition to that, only with the used of RAPH, Super Straight Polishing Line (0^0) can possibly be achieved, which important capability for an advanced manual polishing method such as analysis of Long and Narrow DTI trench as explained in section 4.12.1 in this chapter.

4.16.1 Cost

From a cost standpoint, the RAPH material cost is only around the range RM 3000, when compared to the alternative for cross-sectioning long narrow structures, the Plasma Dual Beam FIB (PFIB) which costs an expensive USD 2 million, which is 3 orders of magnitudes more expensive than the RAPH, which may pose a problem for budget proposals for the failure analysis laboratory to the fab administration.

One motivation for developing the RAPH is the ability to do local failure analysis, especially on long narrow structures, for cheaper. The status quo is that analysis of these long and narrow structures must be outsourced to foreign firms. these firms tend to charge USD 500 per hour for Plasma Focus Ion Beam (PFIB) milling.

PFIB sample requires approximately 3 hours to complete, for a total cost of USD 1500 per sample. In 2017, at least 10 requests from RD were submitted to cut along the DTI line for void and profile investigation. Total avoidance cost in 2017 is approximately USD 15 000. With the use of a RAPH, the failure analysis laboratory can save USD 15 000 in analysis costs, not to mention the additional costs of outsource shipping the PFIB sample to foreign firms in the first place.

CHAPTER 5

CONCLUSION AND RECOMMENDATIONS

5.1 Conclusion

Chemical and mechanical polishing (CMP) is a technique for planarizing or flattening wafers used in the fabrication side of the semiconductor industry. In Failure Analysis Lab, CMP has been a standard de-processing for sample preparation in FA laboratory which employed polisher machine like Allied Multi-pre polishing machine. The techniques employed need to adapt to current technologies. One current technology in the semiconductor industry includes silicon-on-insulator, SOI.

Comparing SOI technology to traditional bulk silicon substrates, there are a number of benefits. The first is making space for smaller devices. The lateral isolation of devices on an SOI substrate enables more compact designs and technologies than is conceivable with traditional bulk silicon. Secondly, SOI lowers the capacitance at source and drain junctions by preventing the depletion areas from penetrating into the substrate as a result of being suppressed by the insulator layer, which lowers RC delay caused by parasitic capacitance. Because of this, SOI CMOS devices function faster than bulk devices, especially at low power supply voltages. Third, SOI has high resistivity values, which is a benefit. SOI substrates have resistivity values higher than 1 k-cm, making them desirable for usage in mixed signal, radio frequency integrated circuits (RFIC), and systems-on-chip (SOC) technologies. Because high resistivity silicon will cause undesirable latch-up in bulk silicon MOSFETs, SOI substrates are required to create high performance radio-frequency circuits. The SOI substrate's BOX layer separates the top silicon layer from the bottom silicon substrate, enabling the top layer to be altered to enhance resistivity without affecting the IC

performance. Energy efficiency comes at fourth. The CMOS devices constructed on SOI substrates have power consumption decreased to one-fifth of bulk silicon CMOS while having speed performance that is typically one generation faster. SOI MOSFETs can function at a lower supply voltage than bulk silicon CMOS operating at the same speed because of the reduced back bias effect and the potential to lower threshold voltage (V_{th}) due to the abrupt subthreshold feature. Thus, low-voltage, low-power, high-performance devices are best suited for SOI technology.

The conventional CMOS delayering techniques based on solely using wet etchants has proven to be ineffective to delayer SOI technology as ILD Oxide, Gate Oxide, and Buried Oxid (BOX) will all be completely etched by HF acid, leaving Top Silicon free. As a result, the Top Silicon structure is broken, cracked, and dirty.

In this research, investigation on suitable technique for delayering of SOI wafer by using combination of parallel lapping and wet etchant was performed. The findings proved that the parallel lapping and wet etching combination is most effective for SOI delayering. The parallel lapping of the SOI wafer sample provides an even surface on which the wet poly-etchant can act to remove small, thin, and dense gate polysilicon structures, leaving a clean delayered SOI wafer sample. For a deeper analysis on active layer, Diluted and Time Controlled Hydrofluoric Acid Etching method was developed to ensure a clean active surface without damaging SOI Top Silicon structure. The wet etching stopped precisely before reaching the bottom of the DTI trench, which is the main concept of the Diluted and Time Controlled Hydrofluoric Acid Etching technique. This is vital to hold the Top Silicon from peeling off during supersonic cleaning and to etch remaining oxide on Top Silicon's surface.

There isn't yet a tool in the Failure Analysis Laboratory that can perform cross-section analysis for a very long, narrow structure like a Deep Trench Isolation (DTI) line in SOI wafer. The only possible method in the market to cross-section this structure is by using an expensive USD 2 million Plasma Focus Ion Beam (PFIB). The nearest possibility to cross-section this very long DTI line with a very narrow width is by using current polisher machine, Allied Multi-Prep, with its hand being reinvented. The purpose of the invention is to obtain a super straight cross-section polishing line. Only then, it is possible to cross-section the very long DTI line with a very narrow width. Thus, a new prototype named the Rapid Alignment Polisher Hand, RAPH was designed and fabricated for cross-sectioning of SOI wafers which incorporate a very long and narrow Deep Trench Isolation line. The key feature of RAPH is the Z groove design which lock Z-Axis while allowing X and Y axis to be adjusted. Mitutoyo precision horizontal micrometre which located on the left and right of RAPH's body help the X and Y axis adjustment. As a result, a controllable polishing angle can be achieved to obtain 0° straight cross-section polishing line. This gives RAPH ability to polish in the middle (contact seam) of a very long ISO DTI Line (835 µm long and 0.942 µm wide) from beginning to end of line. For example, revealing small voids defect underneath the very long DTI Line investigation on SOI product.

In terms of productivity, as compared to traditional or regular Polisher's Hand, sample alignment for cross-section analysis can be completed 12 times faster. Traditional or regular polishing required an average of an hour, but RAPH only needed five minutes. RAPH. In terms of cost, outsource cost saving USD 500 per hour for Plasma Focus Ion Beam (PFIB) milling. Each PFIB sample requires approximately 3 hours to complete, the cost is USD 1500. In 2017, at least 10 requests from RD were submitted to cut along the DTI line

for void and profile investigation. Total avoidance cost in 2017 is approximately USD 15,000.

The evaluation performance of RAPH compared to conventional polisher hand is that the RAPH is able to adjust the incident angle of wafer edge polishing such that a right angle can be obtained with respect to the features and structures on the wafer sample, provided that an accurate measurement of the wafer edge angle is obtained prior to polishing with the RAPH. In addition, analysis of variance shows that the RAPH maintains a consistent right-angle polish when the wafer sample is repeatedly mounted and dismounted from the RAPH, thus giving some evidence for the reliability of the RAPH. In summary, the RAPH can be used to perform accurate and precise cross-section polishing of wafer samples, especially long and narrow structure design in SOI wafers.

5.2 Recommendations

RAPH can be used for any cross-section application which require to polish long and narrow structure, not just long and narrow DTI line. For instance, a long and narrow poly line, metal line, active line, contact line, oxide line and via line. RAPH's controllable polishing angle enable to precisely polish adjacent structures in one polishing line. This application will save a lot of polishing time.

The future development of RAPH is to add 3rd precise micrometer on RAPH in the middle between left and right micrometer. The 3rd micrometer positioned slightly backward to produce ability to tune Z-Axis. By using current polisher stage, and added with Z-Axis tuning capability, a multi-view cross-section polishing can be achieved. Multi-view cross-

section simply means in a single cross-section surface, we can obtain more profile structure of target. This only possible if Z-Axis can also be control by using 3rd micrometer.

Third recommendation is to fabricate special lapping stage for RAPH. With the special parallel lap stage attached to RAPH, tuning 3rd micrometre will give a slight slanting angle for parallel polishing. By doing this, multi-layer parallel lapping can be obtained. A multi-layer parallel lapping capability means on a single polishing surface, we can observe multiple layers of target structure.

Although there will be more advanced method coming in the future for delayering, such as Plasma FIB, Ion Miller, and Laser etching, only parallel lapping and cross-sectioning by CMP polisher machine can perform global planarization on large wafer surface. This means CMP polisher machine will always be relevant in the future. The future application and work of RAPH will open more windows of opportunity in advanced parallel and cross-section polishing technique in semiconductor Physical Failure Analysis laboratory with high accuracy in a cheaper cost.

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APPENDICES

Appendix A: Journal Publications

1. **Ahmataku, H.**, Mohamaddan, S., Warren, E., Yusuf, M., Azli, A., Hasmaliana, N., Manas, A., & Kipli, K. (2018). Analysis of Gate Poly Delayering in SOI Wafer. *Journal of Telecommunication, Electronic and Computer Engineering (JTEC)*, 10(1-12), 85-87.

Appendix B: Symposium Publications

1. **Ahmataku, H.**, Mohamaddan, S., Yusuf, M., Alias, A. A., & Kipli, K. (2018). Improved Delayering Method for SOI Wafer Processing. *2018 IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)*, (pp. 1-4).