



Faculty of Engineering

**Formulation and Mitigation of Soft Error in CMOS Memory System by
using Transmission Gate**

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Formulation and Mitigation of Soft Error in CMOS Memory System by using Transmission Gate

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DECLARATION

I declare that the work in this thesis was carried out in accordance with the regulations of Universiti Malaysia Sarawak. Except where due acknowledgements have been made, the work is that of the author alone. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.



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ABSTRACT

The downscaling of technology has resulted in increased packing density in CMOS technology and thus, a worrying uptick in single event upset susceptibility in contemporary technology. SRAMs in particular, which now occupy up to 70% of all chip size, are vulnerable to errors from single event upsets, leaving the reliability of its memory storage potentially compromised. The application of submicron electronics in areas of high particle activity in fields such as aerospace calls for the need for technology that is resistant against the occurrence of soft errors, with an increased capacity of mitigating the phenomenon of single event upsets. The current literature has proposed methods such as radiation hardening through methods such as transistor sizing and triple modular redundancy which are unable to keep pace with technology downscaling. This study aims to characterize and model the transient pulse formed from a single event upset, formulate the probability of a state flip in various SRAMs, and produce a transient filter based on transmission gate. The transient pulse, modelled by the double exponential model is injected into the vulnerable memory nodes of the interlocked inverters, Q and QB in the 4T, 6T and 9T SRAMs to observe the amplitude of transient pulse required to incite a state change. The critical charge is then calculated from the readings, and its subsequent probability is calculated further based on the memory node area, technology node of 180nm and the atmospheric cross section per unit area constant. The transmission gate transient filter SRAM achieves an 88% improvement in error probability reduction.

Keywords: Soft error, single event upset, single event transient, SRAM, CMOS

Formulasi Dan Mitigasi Gangguan Ralat Lembut dalam Teknologi CMOS dengan Penggunaan Suis Pemancar

ABSTRAK

Penskalaan semula teknologi telah menyebabkan peningkatan ketumpatan pembungkusan dalam teknologi CMOS dan seterusnya, peningkatan yang membimbangkan dalam kerentanan terhadap gangguan peristiwa tunggal (single event upset, SEU) dalam teknologi kontemporari. SRAM khususnya, yang kini merangkumi sehingga 70% daripada saiz cip keseluruhan, adalah terdedah kepada ralat akibat SEU, sekali gus menjejaskan kebolehpercayaan penyimpanan memorinya. Penggunaan elektronik submikron dalam kawasan yang mempunyai aktiviti zarah tinggi seperti dalam bidang aeroangkasa memerlukan teknologi yang tahan terhadap berlakunya ralat lembut (soft errors), dengan keupayaan untuk mengurangkan fenomena SEU. Literatur semasa telah mencadangkan kaedah seperti pengerasan terhadap sinaran (radiation hardening) melalui teknik seperti penyesuaian saiz transistor dan redundansi modul (triple modular redundancy), namun kaedah-kaedah ini tidak mampu menyaingi kadar penskalaan teknologi yang semakin pesat. Kajian ini bertujuan untuk mencirikan dan memodelkan denyutan sementara (transient pulse) yang terhasil akibat SEU, merumuskan kebarangkalian perubahan keadaan (state flip) dalam pelbagai jenis SRAM, dan menghasilkan penapis denyutan sementara berasaskan gerbang penghantaran (transmission gate). Denyutan sementara yang dimodelkan melalui “double exponential model” akan disuntik ke dalam nod memori yang terdedah pada penyongsang terkunci (interlocked inverters), iaitu Q dan QB dalam SRAM 4T, 6T dan 9T untuk memerhati amplitud denyutan sementara yang diperlukan bagi mencetuskan perubahan keadaan. Cas kritikal (critical charge) kemudiannya dikira daripada bacaan tersebut, dan kebarangkalian berikutnya dikira berdasarkan luas nod

memori, nod teknologi 180nm dan pemalar keratan rentas atmosfera per unit luas. Penambahbaikan kebarangkalian sebanyak 88% telah dicapai oleh kaedah yang dicadangkan.

Kata kunci: *“Soft error”, “single event transient”, “single event upset”, SRAM, CMOS*

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LIST OF ABBREVIATIONS

SER	Soft error rate
CMOS	Complementary metal oxide semiconductor
UNIMAS	Universiti Malaysia Sarawak
BPSG	Borophosphosilicate glass
SRAM	Static random access memory
SNM	Static noise margin
SEU	Single event upset
Q_{col}	Collection charge
Q_{crit}	Critical charge
4T	Four transistor
6T	Six transistor
9T	Nine transistor
C_{node}	Node capacitance
LET	Linear energy transfer
V_{DD}	Supply voltage
MOSFET	Metal oxide semiconductor field effect transistor
NMOS	N-channel MOSFET
PMOS	P-channel MOSFET
WL	Word line
BL	Bit line
BLB	Bit line bar
FF	Flip flop

VTC	Voltage transfer characteristics
I_{read}	Read current
V_{BL}	Bit line voltage
C_{BL}	Bit line capacitance
MCU	Multiple cell upset
MBU	Multiple bit upset
FPGA	Field programmable gate array
LUT	Look up table
V_{th}	Threshold voltage
PR	Pull up ratio
CR	Cell ratio
CNT	Carbon nanotubes
SEE	Single event effects
BEOL	Back end of line
L_f	Length of funnel
TCAD	Technology computer aided
TID	Total ionisation dose
FET	Field effect transistor
TMR	Triple modular redundancy
TPDICE	Triple path dual interlocked storage cell
SOI	Silicon on insulator
HVPDH	Horizontal vertical parity and diagonal Hamming
PIM	Processing in memory
LRS	Low resistive state
HRS	High resistive state

TTF

Transient transmission filter

LIST OF SYMBOLS

τ_{α}	Collection time constant
τ_{β}	Ion track establishment time constant
k	Boltzmann constant
ε_o	Permittivity of vacuum
ε_r	Relative permittivity of silicon
q	Electron charge
N_D	Donor density
μ	Electron mobility
τ_r	Rise time
τ_f	Fall time

CHAPTER 1

INTRODUCTION

1.1 Study Background

The downscaling of electronics into the submicron range has presented an old challenge with a new problem, mitigating circuitry against errors with the added issue of single event upsets. If complementary metal oxide semiconductor (CMOS) technology is to obey Moore's law, new design approaches must be taken to continue its trend. The downscaling of technology leads to higher circuit density on a smaller area, leading to higher sensitivity to soft errors occurring.

The study of soft errors has been as a phenomenon has been undertaken since the 1970s when it was first observed to occur in space equipment. Since then, the attention of the scientific community on soft errors has only grown as recent technology trends towards higher sensitivity, especially in SRAMs where downscaling was done by implementing smaller capacitance with smaller dimensions. Now that the trend involves the reduction of transistor dimensions, supply voltage reductions along with a plethora of other parameters, single event transients, once an abstract concept, now present a concrete threat to the continued reliability of CMOS technology. Bolstering CMOS technology against soft errors while simultaneously maintaining the trend of downscaling presents a unique challenge to designers.

Soft errors may be produced when a radiation-sourced particle collides with a gate. While single event transients are temporary in nature and can be overwritten by the next

clock cycle, if the transient signal is latched into a memory element, it will lead to the occurrence of a soft error. Soft errors can threaten the reliability of high-performance chips despite their transient nature, exacerbated by the recent prominence of single event multiple transients caused by the upward trend of circuit density (Evans et al., 2016).

The mechanisms of single event upsets and an overview of techniques used for mitigation against them are explored in chapter two. Chapter three covers the methodology used to investigate the soft error sensitivity of the 4-transistor, 6-transistor and 9-transistor static random-access memory (SRAM). In chapter 4, the results of the simulation obtained are discussed and elaborated upon.

1.2 Problem Statement

The field of soft errors is lacking in a method to formulate probability of known vulnerable nodes being affected by soft errors. This study proposes not only a mathematical algorithm to formulate probability, but also a dataset for the SRAM memory response to parameter variations in temperature and voltage supply. SRAMs can experience an increase in the rate of soft errors due to the influence of atmospheric neutrons (Burnett et al., 1993). These soft errors can affect the interlocked inverters holding the data of the SRAM and cause a bit flip to occur (Bota et al., 2009). Not only does the threat to this region need to be analysed, but the SRAM must also have a system in place to protect it against further single event transients that can be scalable with voltage as voltage scaling is one of the first parameters altered in order to reduce the power consumption of a design. This is disastrous in circumstances of where reliability is especially required such as aerospace or in the medical field (Toghuj, 2020; Zhao et al., 2022)

The issue of soft errors has been brought to the forefront of many design considerations as the downscaling of technology in accordance with Moore's law begins to tread the territory of submicron levels (Arden, 2002; Schaller, 1997). With this issue, it becomes imperative that to design qualitative measures to evaluate the robustness or weakness of circuitry to the effects of single event upsets. High density memory devices are especially prone to radiation induced errors, but the severity of soft errors has become has worsened with downscaling and an understanding of soft error probability must be achieved to ensure the reliability of a system against single event upsets. Therefore, theoretical modelling and soft error analysis is crucial to further the understanding of system mitigation and improving the system reliability. Thus, alternative methods for the evaluation of failure probability due to single effect upsets are required to provide a larger selection of tools toward the effort of improving robustness against soft errors.

Though there are existing methods in the field of microelectronics that address these issues mainly in the form of error correction code, radiation hardening by design and the use of triple modular redundancy, further research must be conducted to directly target these erroneous data flips. In the case of this study, the modelling of the transient error using the double exponential model and the subsequent formulation of failure probability based on the 180nm technology node serves to present a novel and realistic mathematical model to represent the robustness of a given system against single event upsets. Furthermore, the study seeks to present a novel method to filter the transient currents from the data nodes of a static random access memory cell, thus avoiding the occurrence of an unintended data flip, a method that provides additional robustness in exchange for minimal area overhead.

1.3 Hypothesis

The critical charge of the SRAM memory node can be increased and therefore hardened against single event upsets through the use of transmission gate transient filters, the results of which can then be validated through a novel method of probability formulation.

1.4 Objectives

The research aims to formulate the probability of the occurrence of a soft error and design a mitigation method against it. This can be achieved through the following set of objectives:

- i. To assess the reliability of the circuit and the system due to the SEU
- ii. To formulate the probability of soft error when transient current is injected into the system
- iii. To mitigate the system with the use of a transmission gate transient filter
- iv. To evaluate the performance of the transmission gate transient filter using the probability formulation

1.5 Project Scope

The scope of this project is to investigate a new method with which to evaluate the robustness of a system against data corruption, specifically from the production of a transient current from the single event upset phenomenon, which is produced as a result of an ionised particle impacting the sensitive nodes of an SRAM cell.

The research will be conducted under simulations performed in Cadence Virtuoso version IC5141USR3 wherein the 4T, 6T and 9T SRAMs will be modelled within the analog environment tool using 180nm PDK. The transient current model employed will be based on the double exponential model, which will play a part in simulating the effects of single event upset on the memory nodes of the SRAM cells. The critical charge of the memory

node of each SRAM will be acquired and subsequently used to calculate the data flip probabilities for each instance. An additional mitigation measure using transmission gate transient filters will then be proposed and its performance compared against the conventional architectures of the 4T, 6T and 9T SRAM.

CHAPTER 2

LITERATURE REVIEW

2.1 Overview

Current literature on the mechanisms, sources and modelling methods of soft errors is detailed in this literature review. Also included in this chapter are common measures put into place to mitigate, detect, and correct soft errors caused by single event upsets.

2.2 Soft error in CMOS SRAM

SRAM cache is comprised of an array of bi-stable memory bitcells and other circuits. Read and write processes are facilitated by the surrounding circuitry. A conventional SRAM memory architecture is shown in Figure 2.1. An SRAM array is made up of millions of uniform bitcells. Consequently, much research has been invested in bitcell design improvement as any upgrade in reliability, performance and saving in static power has an overall effect on the entirety of the system. High performance processors prioritise operating speed and bitcell area to maintain high cache density and reliability but energy efficiency and reliability present significant issues in low energy applications. A memory bitcell can store a bit of data, either "1" or "0" (J. Singh et al., 2013).

The columns of each SRAM array share a word-line (WL) and a pair of bitlines (BL, BLB). SRAM arrays are bound by the bitline and word-line capacitances and resistances. SRAMs are used in cache memories and systems-on-chip (SOC) to take advantage of their superior speed. Device scaling, however, poses design challenges. Now designers must work around lower threshold voltages and specified manufacture conditions put in place to reduce energy leakage.

Memory arrays are structured so that their horizontal and vertical dimensions are of equal size. Ergo, substantially sized memories may be placed in blocks with a set number of columns and rows. Each memory row is to hold a number of words that can be represented by 2^k , wherein k is a selected integer. The number of rows and columns are arranged as $2^n - k$ and $2^m + k$ as represented in Figure 2.1. By selecting the proper word-line (WL) and bitline pair (BL, complement of BL), correspondingly, triggered by the row and column decoders, each bitcell may addressed by random (Kanhaiya et al., 2019b).

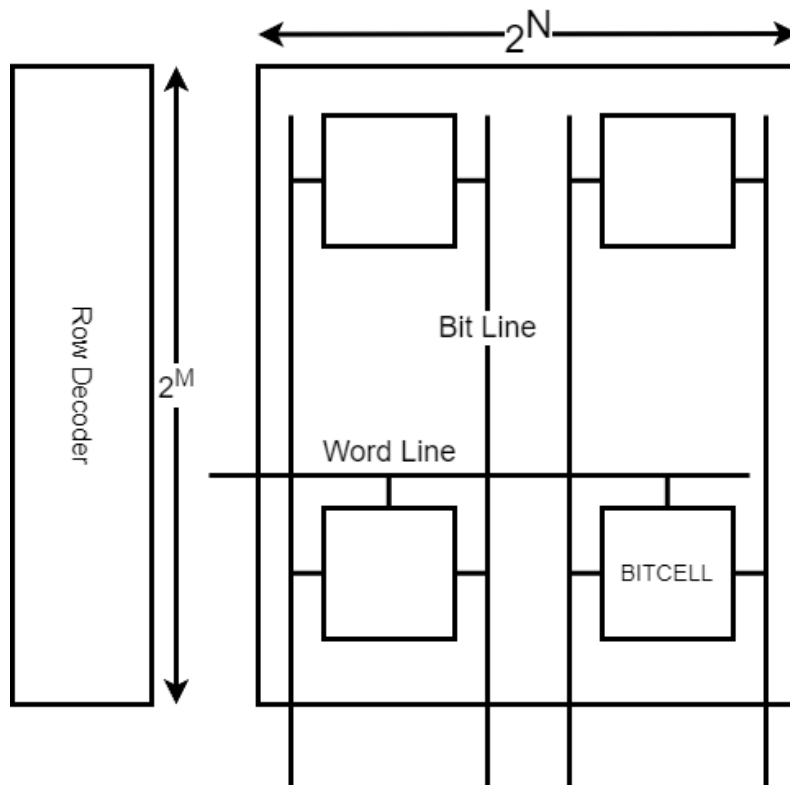


Figure 2.1: SRAM array structure.

Complementary Metal Oxide Semiconductor (CMOS) devices, such as Static Random Access Memory (SRAM) or Flip Flops (FFs), are often fabricated with a stripe structure of p and n-dual wells wherein the same stripe architecture on a chip contains all the circuit nodes. Silicon on insulator (SOI) designs use two wells instead of one, and isolation

oxides work to ensure separation between nodes. A fully depleted silicon on insulator design has a thinner depletion layer than the SOI layer, while the converse is a partially depleted (PD) SOI. Buried oxide has a covered depletion layer, reducing parasitic capacitance further than the previous designs, and presenting overall greater performance (Ibe, 2015). The static random access memory design (SRAM) has not been left out of the race for technologies pursuing lower operation voltages. This downscaling, however, also makes SRAM memories also require protection from soft (Hashimoto & Liao, 2020).

Each successive generation of technology has continued to develop transistors that are smaller, more efficient, and capable of switching faster than those produced by any prior generation. Previously, intrinsic transistor delay allowed microprocessors to operate in each new generation at higher frequencies, and as a result, computer performance steadily improved at a rapid pace. Since the introduction of Von Neumann's vision of how to accomplish computing in 1945, the fundamental computer architecture has not profoundly altered. But the power used by integrated circuits (ICs) kept going up until the beginning of this decade, when some of them finally hit their thermal limits. Then, it became evident that it had become practically impossible to sustainably increase operating frequency and the number of transistors. Since the middle of the preceding decade, frequency has stagnated in the region of a few gigahertz, having been chosen as the trade-off. During the past five to ten years, new transistor designs and architectures have been developed to address this issue (IRDS Systems and Architectures Team, 2020).

Using their advanced technology, semiconductor manufacturers try to take the lead in the fight to miniaturise chips. The area of an SRAM memory cell that represents is halved with each successive technology. Decreasing the size of the memory cell will

increase device unreliability, owing to diffusion and fluctuation of impurities required for fabricating the transistor devices that make up a memory cell, resulting in obstacles in SRAM design. SRAM memory cells have an inversely proportional relationship for performance and stability. By decreasing the threshold value of the transistors that comprise a memory cell, the memory cell's performance is enhanced, but its stability is compromised. With the growing dispersion of threshold values that accompanies the shrinking of semiconductors, the frequency of unstable memory cells will increase, incentivising cautious design to ensure results. Consequently, reducing the size of a memory cell in accordance with the progress of semiconductor technology results in a performance decline. This results in high-speed application SRAM manufacture being challenging. Between 2005 and 2018, the projected increase in transistor density between logic and embedded SRAMs is from about 5 to 6 times for every technology node. Simultaneously, the size of a 6T SRAM cell is comparable to approximately 36% of the logic gate area of a conventional four transistor design. This is predicted to scale down to 35% by 2018 (Nakadai et al., 2011).

The downscaling of SRAM cell sizes typically follows a pattern of reducing by half each generation. Memory cell scaling thus results in an expansion of the area where spot defects in the manufacturing process can lead to undesired mistakes in the topology and thus, cell damage. Embedded SRAMS are also experiencing increasing bit counts, heightening the risk of deformities. Therefore, the challenge for design and testing is compounded for each subsequent generation of technology.

Furthermore, the sensitivity of SRAMs to cosmic neutrons have been investigated especially within the context of equipment in the medical field. Cosmic neutrons, a primary contributor of single event transients, have been demonstrated to induce device malfunctions

in implanted medical equipment such as pacemakers (Plettenberg et al., 2022). While investigations of SRAMs under radiation exposure is nothing new, the detrimental effects of disruptions in device operations on human lives cannot be understated (Weide-Zaage et al., 2022).

2.2.1 Stability Metrics

It is imperative that the SRAM maintains its data at any state, but technology scaling imposes reduced supply voltage and increased leakage current and variability, resulting in lower stability. Seevinck et al. (1987) introduced the stability metric known as static noise margin, which defined as the maximum quantity of noise that an SRAM cell can resist while maintain its stored value. Voltage transfer characteristics (VTC) will graphically move in the butterfly curve as it approaches the SNM with the increase of the noise voltage (Grossar et al., 2006a). The figure of a 6 transistor SRAM is as shown in Figure 2.2.

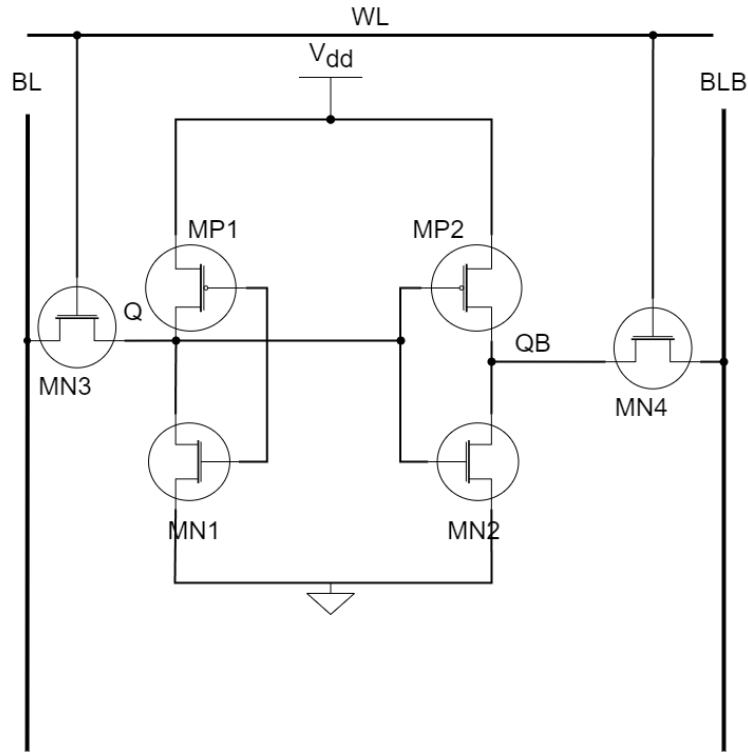


Figure 2.2: 6T SRAM cell

The pull-down transistor and the pass gate ratio will be the defining factor of the SNM. Ideally, the gain SRAM inverters would be infinite and produce a square of maximum side length in the butterfly curve. The additional steps required to obtain the SNM from the butterfly curve presents another downside to the technique (Agarwal & Nassif, 2008). Using testers to form an N-curve is another method to quantify stability for SRAMs. These are valuable metrics used to measure the stability of the read-stability and write-ability. Within the context of qualitative analysis of a system against single event upsets however, this method does not provide sufficient insight on the robustness of the system against the effects of the transient current formed as a result of a single event upset, lacking the values of critical charge and threshold current of an erroneous data flip.

The progress of electronics necessitates more efficient circuitry. As embedded SRAMs take up most of the area silicon-on-chip, the consequences of aging and process variation are exacerbated for memory elements and can reduce the period of failure free state for the device (Alorda et al., 2018). More stability metrics must be designed to present accurate results following these developments for highly secure systems. The drift of threshold voltage of a device must be approximated to observe the performance degradation of memory due to process variation and other factors. Cost effective test methods must be specially designed to for screening of defective SRAM cells.

While static noise margin is widely used to numerate the stability of SRAMs, dynamic metrics too have been proposed in order to provide a characterization of SRAM stability when it has undergone degradation from negative bias temperature instability which can cause a reduction in reliability. As opposed to static stability metrics for SRAM, dynamic metrics engage the word-line and find the critical pulse width needed to facilitate write/read operations (Chaudhari et al., 2018). Designers must balance the ratio of performance and cost by improving the size of SRAM arrays to reduce chip cost. Consequently, SRAM arrays are densely packed onto the chip design, resulting in chip regions that are vulnerable to processing errors or changes. The challenge of downscaling SRAMs stems from the fact that previously, the power for SRAMs were reduced by lowering the value of the supply voltage. This method cannot be used indefinitely as the saturation current of SRAMs remain the same as dimensions of technology is reduced (Pavlov, 2008).

The read current I_{read} of an SRAM cell is determined by the saturation current of the access transistor, while the speed is frequently determined by the small-signal slew rate:

$$t_{\Delta V_{BL}} = \frac{C_{BL} \Delta V_{BL}}{I_{read}} \quad \text{Equation 2.1}$$

If I_{read} is unchanged, Equation 1.1 demonstrates that the speed of SRAM can be increased by decreasing the bit line differential created during a read operation V_{BL} and/or the capacitance of the bit lines C_{BL} . Scaling the size of the transistors has only a small effect on the bit line capacitance C_{BL} , which is made up of the diffusion capacitance and the wire capacitance. The wire capacitance component that is responsible for at least fifty percent of the total bit line capacitance C_{BL} is not decreasing at the same pace as the speed of the logic circuits. Therefore, V_{BL} does not scale at the same pace as the logic speed.

Unfortunately, this method has reached the limit of its feasibility in sacrificing power and area. Multi-stage or complicated sense amplifiers, local amplification of the bit line differential V_{BL} , as well as rigorous clocking and pipelining approaches, are also reaching their practical limitations when tackling the non-scaling problem. Thus, the SRAM non-scaling problem represents one of the most challenging design challenges for nano-scaled SRAMs. The desired uses of SRAM arrays, with high-performance applications on one end of the spectrum and low-power applications on the other, determine the potential methods for mitigating the SRAM non-scaling problem.

A significant issue faced by SRAMS are multiple cell upsets caused a single neutron. Interleaving and error correction code are well known mitigative measures against multiple cell upsets but cannot be employed for patterns of larger numbers of upsets in a single event. Such critical MCUs are referred to as multiple bit upsets (MBU), and they hinder the implementation and operation of high-performance systems and applications that hinge on the importance of increased reliability. In addition, there are four probable MCU mechanisms:

- i. sequential strikes by a single ion
- ii. simultaneous multiple impacts by numerous ions
- iii. charge drift/diffusion (charge sharing)
- iv. parasitic bipolar action

At the nominal supply voltage, charge sharing, and parasitic bipolar activity are significant mechanisms in bulk SRAM. When charge spreads to multiple cells, charge sharing occurs which can produce MCU (Rao & Desai, 2019). Multiple cells in a well are flipped by parasitic bipolar activity induced by potential fluctuations in the well. Holes generated by a neutron-induced nuclear reaction raise the P-well voltage, which is equivalent to the base-emitter voltages of parasitic bipolar transistors. Consequently, the collector-emitter current of the parasitic bipolar transistors rises, resulting in the formation of MCUs (Hashimoto & Liao, 2020). These two mechanisms have opposing inclinations with respect to the supply voltage. As the supply voltage decreases, the critical charge, or threshold for the collected charge generating soft errors, as well as the MCU's contribution, decreases. Total reduced bipolar activity of parasites facilitates the formation of charge-sharing-induced MCUs.

Due to the reduced collector-emitter voltage, the parasitic bipolar action becomes less active, and hence, MCUs caused by the parasitic bipolar activity are less likely to occur. The relation of MCU to voltage is affected by the two aforementioned factors. Conversely, fully depleted silicon on insulator (FD-SOI) SRAM does not employ well-sharing, effectively avoiding MCUs that occur through charge sharing and parasitic bipolar action.

Therefore FD-SOI SRAMs see a reduced rate and a lower probability of large scale MCUs (Hubert et al., 2015).

2.2.2 4 Transistor (4T) SRAM

Before CMOS technology was commonplace, four transistor resistor load cells were used. They make use of inverters set at ratio, outperforming 6T SRAMs by about 30% in terms of size overhead. As NMOS have a relatively increased electron mobility (Kita et al., 2019), polysilicon resistor loads commonly employ them. Load resistors offset the leakage current of the pull-down devices in their off state. The load resistor must be high enough to suppress the rise of a “0” state, although this simultaneously increases the propagation delay for a low-to-high transition. This impacts the pre-charging of V_{DD} , which functions to decrease the read time but also threatens the cell reliability. Alternatively, in exchange for increased time and power consumption, the bit lines could instead be pre-charged to the full value of V_{DD} , eliminating the need for transition current for the low-to-high state change. The pull up current must be 100 times larger than the leakage current, which then defines the resistance limit on the resistor load (Simon, 2002).

The progress of technology into submicron sizes imposes complications on the scaling of resistor loads, which is yet another challenge that must be resolved to adhere to noise resistance and limit power consumptions. Furthermore, it was apparent that even in its infancy, the polysilicon resistor would be unable to match the submicron scale of advancing technology as easily (Lu et al., 1982). The downscaling of 4T SRAM was redirected from targeting voltage to constant-field scaling eventually uncovered an insufficient compensation for power consumption at the cost of reliability. The incorporation of polysilicon at high resistance was also not a conventional step in the process of CMOS technology, and the low static noise margin of the polysilicon resistor load poses a further

weak point against soft errors, which blocks system-on-chips using polysilicon resistor load SRAM cells and prohibits use from deep submicron technologies.

While the loadless 4T SRAM has enjoyed some success due to the omission of the PMOS load transistors, and the replacement of the NMOS access transistors with PMOS, allowing for a significantly reduced cell size, the issue of cell stability was still in question. This was due to the requirement that the off current of the access transistors be remarkably higher than the pull down NMOS transistors, a difficult feat for scaled technologies. Zhu and Ohsawa (2022) proposed a design that would be structurally identical to the existing loadless 4T SRAM but that it maintain data based on the gate leakage current of the PMOS access transistors from the word-line.

Improvements for 4T SRAMs can also be implemented with a specific use of the SRAM in mind. Niewiadomski et al. (2017) made several amendments to the conventional design of the loadless 4T SRAM as pictured in Figure 2.3 to optimise it for field programmable gate arrays (FPGA) look up tables (LUT). The modifications included a replacement of the NMOS transistor pulldown with a PMOS pull up network to hold data. For the read state, the bit-lines were connected to ground instead of being precharged to V_{dd} as is conventional. As the drivers were comprised of PMOS transistors, the change in the process step allowed for additional power saving. The auxiliary circuitry would, of course, require consequent changes to account for the adjustment. Furthermore, the design employed the use transistors with a high threshold voltage, V_{th} as a way to further reduce power consumption (Wang et al., 2020). The implementation of the high V_{th} also presented a slight improvement in performance. The design presented decreased leakage current during standby mode.

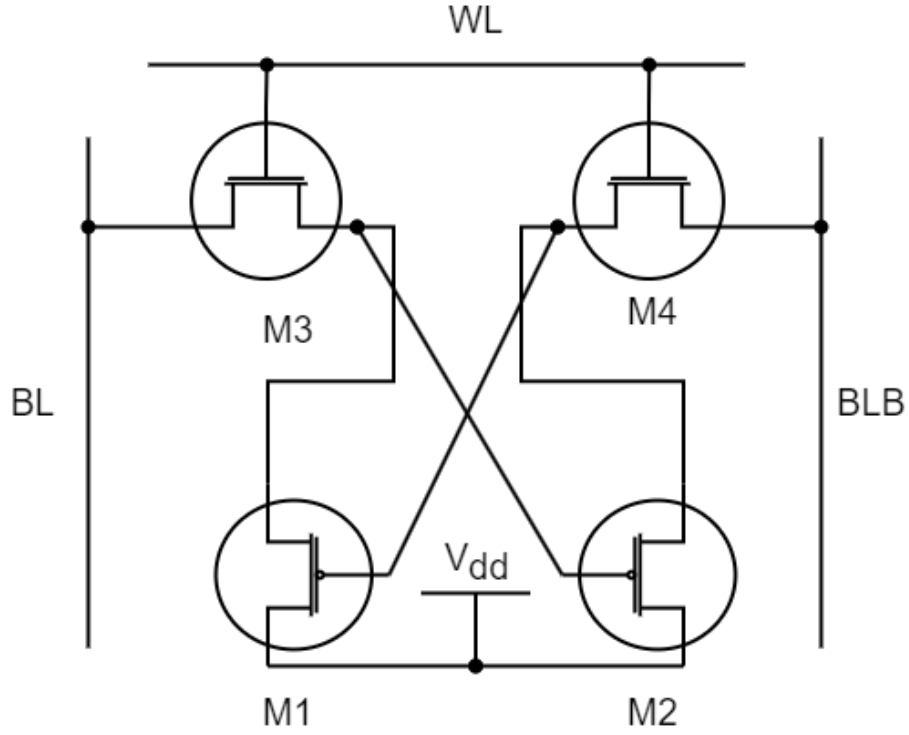


Figure 2.3: 4T loadless SRAM cell with pull up network

2.2.3 6 Transistor (6T) SRAM

The reliability of SRAMs often is dependent while in hold state, but the SRAM can be vulnerable to soft errors in read and write states as well. The vulnerability of SRAM to soft errors remains highest during the read operation (Marques et al., 2021). The performance of the various SRAM cells in their hold state were evaluated. Evaluations were also done on its robustness to radiation, with particular attention paid to the 6T SRAM in its write/read state. In the instance of particle strikes occurring in the auxiliary circuits, fault propagation through the bit lines were observed. Furthermore, the write operation displayed greater resilience against radiation than the read operation. This is due to the voltage division between the two activated access transistors (Singh et al., 2009).

6T SRAMs maintain a non-destructive read and functional write process via the appropriate transistor sizing. The sizing constraints depend on the pull up ratio (PR) and cell ratio (CR). The pull up ratio is the ratio of sizes of load to access transistor in the write process, while the cell ratio is the size of the driver transistor relative to the load transistor. The downscaling of technology has necessitated innovation in SRAM operations. One method employed is the operation of the SRAM in subthreshold region (Teman & Fish, 2010). As the bulk of leakage power on chips comes from SRAMs, minimising the leakage during operation states was prioritised as they could not be shut off during periods of inactivity. With all the advantages of being able to operate SRAMs at low voltage also come with obstacles. A major one is the consequences of process variations is raised by a drastic degree, with large current variation in minor threshold voltage fluctuations, worsened by shifts in operation temperatures which further upset NMOS/PMOS ratios (Salehuddin et al., 2011).

While the conventional 6T SRAM provides improved performance over its predecessors, design tweaks have been made to maximise optimal operational results. An example of this would be the fabrication of CMOS SRAM arrays on carbon nanotubes (CNT) (Kanhaiya et al., 2019). The findings show promising results, the density scaling is enabled by the low temperature processing, whereas silicon requires much higher temperature in its production process.

Since the scaling of technologies is mainly impeded by the challenges of reducing power consumptions, that particular factor has been the focus of many studies. One of which is that of a single ended 6T SRAM cell designed especially for significantly low voltage applications (Singh et al., 2008). Designing for low voltage applications can prove difficult,

as one must delicately balance between low power consumption and maintaining good data stability. The isolated read current path promotes higher noise robustness and read stability.

The design strategy of cell storage node isolation has been used in multiple other 6T SRAM cells. Notably in 40nm technology design, a low power version of a single ended design was used(Wang et al., 2021). The standby power is decreased when the word-line is inactive due to a decreased voltage level, which is brought back up to normal supply voltage during read/write operations. The proposed SRAM achieves a relatively robust SNM and high speed despite its low operational voltage.

The single ended 6T SRAM design has also been employed in in-memory computing(Yan et al., 2020) . The work had improved on the existing 5T SRAM which had a Q node that was vulnerable to leakage current and would ultimately be destroyed through current accumulation (Wang & Hsieh, 2016). The SRAM was designed to hold the inputs for the ripple carry adder without a destructive read.

2.2.4 9 Transistor (9T) SRAM

The 9-transistor (9T) SRAM functions to store information using cross coupled inverters and is built upon the design of the 6T SRAM (Apollos, 2019). The design of the 9T SRAM has a differential read that removes connections between the data and the bit lines (Karthika & Sivamangai, 2016). During hold operation, the leakage power consumption is reduced by a greater degree than that of 6T SRAM cells. As the read bit line is engaged during the read operation, a significant pull-down effect is produced, reducing the voltage rise of whichever node is holding a “0”. This is due to the reduced resistance between the data nodes to ground, resulting in an improved discharge. During the write operation, the read word line is disengaged, and the word line is enabled to write into the data storage nodes.

Further innovations upon the existing 9T SRAM design has been proposed to improve the read and write SNM by reinforcing the data in the inverter loop through the use of additional transistors (Hassanzadeh et al., 2013). The word lines for the bit line and bit line bar are distinct, resulting in total separation between read and write lines. Thus, the use of stack transistors reduces leakage current, as well as improves the operation time for write.

The read SNM and leakage power was also addressed in a novel 9T SRAM cell (Zhiyu & Kursun, 2008). The design was possessed of two access connections for read and write respectively. The bit lines were separated from the data during read, which provided a substantial increase in the read SNM. The data stability allowed smaller transistor sizing in the SRAM and produced less power consumption due to leakage. The enhancements maintained the new data stability when tested with variations under temperature.

Transmission gates have been used in place of NMOS or PMOS access transistors of SRAMs to strike a balance between increasing write and read stability. Pal et al. (2019) had designed a 9T SRAM cell that employed transmission gates to separate the bit lines from the memory nodes as well as the write and read lines being distinct from one another. In comparative studies of the proposed transmission gate 9T SRAM against SRAMs of similar size, the proposed SRAM displayed superior performance in comparison. The transmission gate 9T SRAM also displayed resistance against the problem of half selected cells, which can be prone to having adjacent cells changing data when one cell is written into.

2.3 Soft error modelling

Modelling single event effects (SEE) are vital for formulation of soft errors in system to design comprehensive mitigation measures against them. The application of SEE modelling to nanotechnology remains a difficulty. In the past decade, multi-physics modelling using on Monte-Carlo simulations has replaced obsolete engineering approaches for estimating SEE rates (SERs). These novel techniques are vital for analyzing the sensitivity of a device, researching evolving technology, and monitoring developing SEE phenomena. Multiphysics techniques permit the modelling of the radiation field (including complex radiation fields), the transport of primary particles in the sensitive target throughout the overall shielding, package, and back end of line (BEOL), electron-hole pair generation through ionisation processes, the charge transport and collection, and the circuit electrical feedback (Hubert et al., 2015).

Normally, SET effects are simulated by injecting a current pulse in specified circuit nodes using SPICE simulation software. According to Andjelkovic et al. (2017), modelling of SET currents typically employs the concepts of:

- i. Macro-modelling where the current source is designed as an independent module connected between the output of the intended gate and the ground.
- ii. Micro-modelling where the target transistor has the current source built in

The macro-modelling concept sees more popularity due to its ease of implementation while the micro-modelling only be employed when there are transistor models available within the simulation. Particle strikes can be modelled using the micro-modelling method in PMOS and NMOS transistors. There are four categories under which models for SET current have been proposed.

- i. Single voltage current source
- ii. Current sources reliant on voltage
- iii. Dual voltage independent current sources
- iv. Switch and resistor in series

2.3.1 Single voltage current source models

Through experimental techniques, it has been observed that a majority of charge collection was largely due to the action of drift conduction during a particle strike (Messenger, 1982). The formulation of such observations was then ceded to be expressed in a double exponential as;

$$I(t) = \frac{Q_{coll}}{\tau_\alpha - \tau_\beta} (e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}}) \quad \text{Equation 2.9}$$

Where Q_{coll} is the collected charge generated from the particle strike, while the τ_α and τ_β are the time constants for the collection and diffusion time constants for the junction respectively. This formulation will be used over the course of this study as it sufficiently models the shape of the transient current produced by the single event upset.

2.3.2 Current source reliant on voltage

This model implements a voltage dependent current source in a 90nm CMOS technology as presented by Figure 2.4 (Kauppila et al., 2009). The model is made up of an independent current source, I_{SRC} , a capacitor, C_S , and two dependent current sources G_{REC} and G_{SEE} . I_{SRC} is applied as a double exponential current while the capacitor C_S conserves the charge from induced from the single event transient. The recombination current and variation node voltage are implemented by G_{REC} and G_{SEE} respectively. The model allows

customisation of the current induced by a single event transient, especially the peak for particularly significant linear energy transfer (LET) levels.

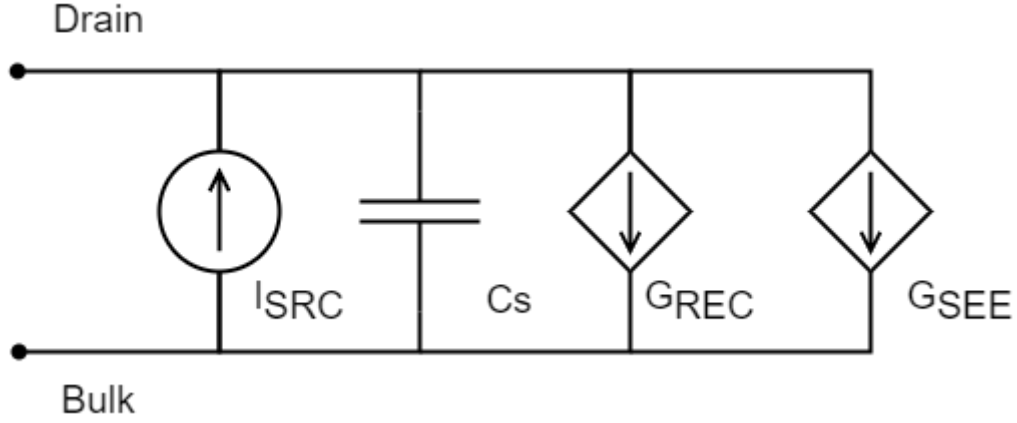


Figure 2.4: Bias dependent junction single event upset model with NMOS transistor

Clark et al. (2003) has designed a voltage dependent current model which is an independent current source derived from the double exponential current model as expressed below;

$$I_{SET}(t) = k(V_{NODE} - V_{SUB})(e^{-\frac{t}{\tau_{\alpha}}} - e^{-\frac{t}{\tau_{\beta}}}) \quad \text{Equation 2.10}$$

Where I_{SET} represents the single event transient current, with τ_{α} and τ_{β} representing the collection and diffusion time constants for the junction respectively. The target node voltage is expressed by V_{NODE} , substrate voltage is V_{SUB} , and k is technology-based value that is defined from;

$$k = q\mu N/L_f \quad \text{Equation 2.11}$$

Where electron charge is expressed by q , the average carrier mobility in silicon is defined by μ , per length number of electron-hole pairs produced is defined by N , and length

of the funnel is defined by L_f . This model was employed in the analysis of probability of a state change and the determination of the effective cross section of the processor, which plays a factor in the sensitivity of the device against soft errors.

2.3.3 Dual voltage independent current sources

In a model proposed by Black et al. (2015), two current sources are in parallel, each representing a component of the single event transient pulse, namely one with a high current peak and narrow pulse width, and the second being one with a low current peak and a long pulse width. These two current models, as illustrated in **Figure 2.5** are combined to form a model of single event transient comparable to that devised in technology computer aided (TCAD) simulations performed at device level (DasGupta et al., 2007; Kauppila et al., 2009). This model would then be able to accurately recreate the high current peak and the low current shelf that followed. The collected charge would then be obtained from the transient currents of the combined model.

The model was not without its weaknesses, however. When inserted into a simulated circuit of four inverters, the simulation showed that the calculation of the critical charge will fluctuate away from that of expected values at different points of the circuit. It was found that the model was still more precise and had simpler implementation even with these inaccuracies.

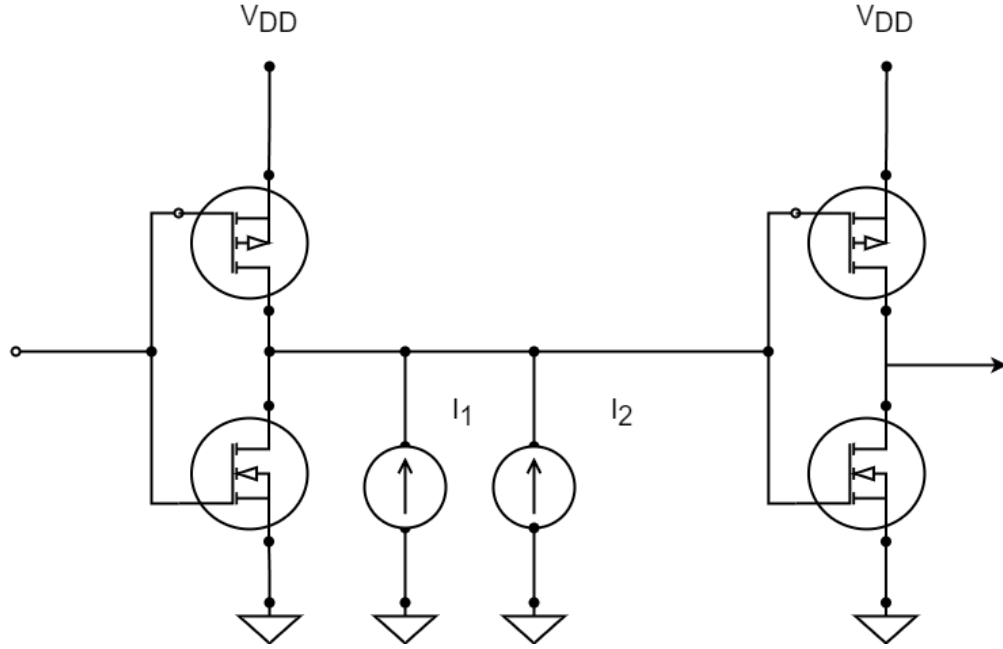


Figure 2.5: Dual voltage-independent current source

2.3.4 Switch and resistor

To obtain a waveform consistent with the plateau region demonstrated by TCAD simulations, Makihara et al. (2008) proposed that a switch and a resistor connected in series be implemented in place of a current source as illustrated in Figure 2.6. The initial peak of the waveform would be chiefly sourced from the load capacitors, with the subsequent lower shelf current coming from the transistors. The collected charge would be determined by how long the switch is closed and the peak capacitor current would be controlled by the resistor. The study compared the TCAD voltage pulse of the single event transient, and the SPICE simulations for switch and current source, with the TCAD and switch SPICE simulations being acceptably close. It was found that the voltage pulse of a transient can be increased when the current levels out. The switch SPICE implementation was able to reliably recreate voltage pulses with plateaus and otherwise, allowing for predictions of responses to single event transients with SPICE simulations given TCAD data for collected charge estimation.

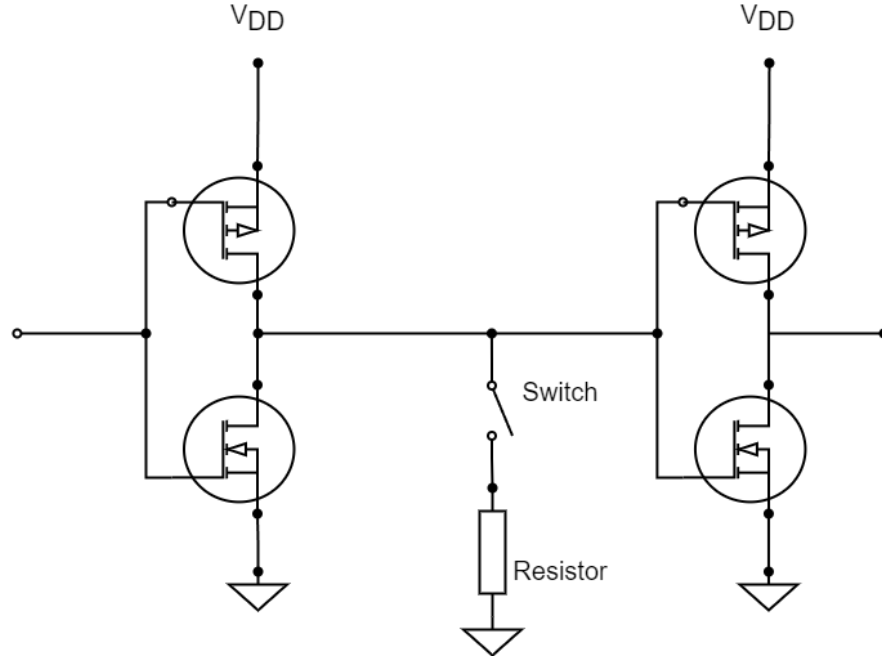


Figure 2.6: Switch and resistor model

2.4 Mitigation Techniques

This section covers the current literature on mitigation strategies employed in the interest of error rate control and soft error reduction. The strategies are categorised under radiation hardening by design, modular redundancy and transient filters. This section also compared the advantages and disadvantages of each strategy compared to one another as well as the transmission gate transient filter proposed in this study.

2.4.1 Radiation Hardening

The isolation of FET by the insulator presents a desired quality that makes the SOI CMOS a preferred technology. SOI pixel devices using fully depleted silicon on insulator are particularly sensitive to the effects of total ionisation dose (TID). Hara et al. (2019) reviews enhancements in radiation hardening. Pixel devices implemented with fully depleted silicon-on-insulator have been in development since 2005, with observations noted of the sensitivity increase to the total ionisation dose effect inflicted by the insulator. Improvements

in radiation hardness are reviewed as well. Radiation hardness assessments when presented with TID were conducted with gamma particles sourced from the Cobalt-60 isotope, as well as protons with a magnitude of 70 MeV (Kochiyama et al., 2011). The ionisation shifted the voltage threshold of various field effect transistors (FET), increasing the vulnerability of the FETs to data corruption through soft errors. This is largely due to the insulator encompassing the FET. The TID effect is exacerbated in the designs of both the gate oxide and buried oxide. For buried well designs, layers under the buried oxide are lightly doped. The back gate effect is counteracted by the buried well protecting the circuit. However, it is imperative that the potential beneath the circuitry possesses a separate control as it is dependent on the pixel node, and that the suppression for the back-gate effect diminishes with increase in proton fluence.

One such design is a 6T SRAM with dedicated ports for read and write (J. Singh et al., 2013). This would include the conventional cross coupled inverters for memory storage with the addition of the two ports. The design adds an additional transistor to isolate the memory nodes from the read bit line, which allows access to the read port. The state of QB informs the data through the write port bit line. In the instance of node QB holding the data '1', bit line is high, and the corresponding information obtained is '1' as well. The converse is true when QB is '0'. The node Q is able to maintain its state at '0', due to the use of a distinct path for the read current. The activation of the read port depends on the read word line, which also manages the read assist transistor. A pass gate device controlled by the write word-line connects node QB to the write word-line and bitline, denoted respectively as WWL and WBL. A single-port bitline executes the write operation, facilitated by the write assist transistor. The complement of the write word-line thus determines the activation of the write assist transistors. Two port 6T bit cells have the advantage of a more stable and

efficacious read operation to 8T SRAM bit-cells, due to the isolation of the read bit-line. Furthermore, the complement of the write word line facilitates the operation of the write-assist transistor. All word bit cells are contingent to the read and write assist transistors.

Furthermore, in the case of SRAMs, there have been efforts to harden circuitry against soft errors by increasing node capacitance. As the critical charge Q_{crit} is the result of node capacitance multiplied with the node voltage, it would then be natural to increase the node capacitance to increase the critical charge, subsequently producing a more robust design. This method was then employed by Liaw and Chu (2007) by adding capacitors to the feedback loop of the SRAM cell. Due to the formation of the layers in MOSFET design, parasitic capacitance can be formed due to its arrangement. Charges can collect at the overlap of the metal gate oxide and the source region. This can also occur in the drain and gate connection. With the cell now having an increased critical charge, disruptions to normal operations require higher energy particles or longer lasting charges. The discharge time of the node now being longer also reduces the soft error rate (Degalahal et al., 2006).

The usage of process variations and material changes have also been employed to improve the SER in devices. For example, the process changes investigated have included manipulating junction depth to reduce the diffusion depth and manipulating the dosing of the source and drain junctions to lower the junction leakage (Chavali, 2019).

2.4.2 Modular redundancy

A well-established technique for SEU mitigation is the triple modular redundancy (TMR). This technique uses a method that repeats a circuit in triplicate which then feeds into a voter (Vanderkulk, 1962). In the instance that one of the circuit repetitions are affected, the majority voter can derive the original signal from the remaining unaffected circuits. With the effects of SEU overwritten, the design defends the soundness of field-programmable gate

arrays (FPGAs) that are derived from SRAMs (Keller & Wirthlin, 2021). A reduction of SEU effects can be achieved with a selective implementation, though triple modular redundancy is most efficacious with the technique implemented throughout the design. A selective approach may be selected to reduce costs and area overhead of the circuit. The percentage of tripled components is the cost. The benefit-cost ratio should be maximised. On a benchmark design, 25 distinct options are tested. Some choices notably increase the cross section while others noticeably lower it.

Reliability in deep neural networks is important especially in fields of autonomous driving and aerospace. Unfortunately, FPGAs based on SRAMs can be vulnerable to the effects of soft errors. This weakness can be addressed through triple modular redundancy at the cost of area overhead and increased power. The robustness of deep neural networks against single event upsets can be increased through the usage of approximate TMR wherein the logic was applied to produce similar results to a conventional TMR model. The reliability saw a 40% increase, with 8% improvement in resource usage and 4% decrease in power consumption. The same success can be seen in the application of TMR to hardware IPs as well (Sánchez et al., 2019).

Jiang et al. (2018) proffered a cost-effective, error tolerant latch in 110nm CMOS technology which is made up of a storage cell based on clock gating for data retention and employs a Muller C-element to impede single event upsets. In comparison to the conventional triple path dual-interlocked storage cell (TPDICE), the latch presents an advantage of a reduced power usage, delay and area.

Silicon on insulator (SOI) SRAMs on thin buried oxide films were exposed to heavy ions for ground level and cosmic radiation simulation to observe soft errors. Soft error

vulnerability is at a higher degree with a back bias method. Multiple cell upsets were discovered to be the cause of the increase. The fluctuations induced by ions under the buried oxide cause multiple cell upsets due to capacitance coupling. The P well can be vulnerable as a radiation hardening method as ion strikes can result in capacitance coupling, consequently activating the top SOI transistor's error correction code.

The rectification of soft errors is commonly performed through single error correction code, correcting singular errors in each memory word, but this method loses efficiency with increasing frequency of soft errors. Multiple bit errors can be detected through horizontal-vertical parity and diagonal hamming (HVPDH) (Raha et al., 2017). The technique implements an encoder/decoder for error detection and correction that employs three-dimensional parity sets. The reliability metrics analysed for error controls are code rate, the bit overhead and reliability. The HVPDH technique can deliver a similar measure of reliability while reducing the parity bits.

Efficient contemporary computing requires a need for a distinction in operation between memory and computation. The bulk of resources, however, are spent in the ferrying of data transfer between processing and memory units, thus displaying a concept known as the von Neumann bottleneck (Zou et al., 2021). One method devised to tackle this problem is the use of processing-in-memory (PIM) technology, wherein data can be stored and computed within the same location (Hayashikoshi et al., 2020). This is done through the combination of processor and random-access memory (RAM). Other factors can increase the already latent advantages in the process, with the demand for PIM technology increasing with the progressive accessibility of capable hardware.

PIM can be implemented with the use of a resistive memory array, or the memristor, originally introduced as a circuit element that stores and displays data through its resistive states, with a low resistive state (LRS) and high resistive state (HRS). Furthermore, the resistance of the device can be manipulated by the level of voltage applied (Leon, 1971). These devices, however are not unique in their weakness to being affected by soft errors, as ion strikes can still affect their data storage (Liu et al., 2015).

2.4.3 Transient filter

As a measure of protection for circuits against the effects of soft errors, transient filters have been devised in order to halt them before they reach vulnerable nodes. An example of this is a tuneable transient filter meant to reduce the rate of soft errors when inserted into combinational logic (Choudhury et al., 2009; Zhou et al., 2008). The filter, used in tandem with gate sizing, can be modified to specify the maximum suppressible width of the single event upset. The design is a relatively cost-effective method for soft error rate reduction with positive results for 70nm process technology.

There is considerable interest in economical strategies to decrease the occurrence of soft errors in combinational circuits. This study introduces the concept of TTFs (Transient Transmission Filters) to mitigate the impact of propagated SEUs (Single Event Upsets) in such circuits. When coupled with circuit enhancements involving gate sizing and dual VDD techniques, the integration of TTFs emerges as an appealing approach for achieving a notable reduction in the soft error rate without incurring significant costs. An area warranting future exploration involves the targeted optimization of the most susceptible gates. This approach allows for a delicate balance between the overhead incurred and the level of SEU resilience achieved. One method has been the incorporation of transmission gates as a fault tolerant element in CMOS architecture (Fairooz et al., 2021).

Furthermore, investigations have been conducted into the utilization of pass transistors as filters. This entails leveraging the dampening characteristics of logic gates to weaken the effects of transient input pulses and modification of the design of a multiplier was done in order to reduce glitches that arose during operations (Marimuthu & Thangaraj, 2010). The design took advantage of the low pass filtering characteristic provided by the transmission gates. The result of the simulations displayed greater protections against variations that occur during the process and place-and-route stage. The design also provided a lower level energy consumption than the conventional Wallace architecture for multiplier purposes.

Interconnect coupling in integrated circuits pose a weak point that can be exploited by crosstalk noise and delay, which presents a design concern for submicron compositions. While driver sizing can be used to mitigate noise, this method may induce crosstalk noise with adjacent connections and increase area overhead, as well as detract the gate timing. Transmission gates have been proposed to dampen crosstalk noise, leading to reduced area overhead, with nominal adjustments to the initial design (Sayil et al., 2020). The method involved the application of varying gate bias on transmission gate pass transistors proportionally with crosstalk strength to mitigate it. The method was used alongside driving sizing to keep the delay in check, resulting in more economical area compared to driver sizing alone with little layout modification.

2.5 Performance evaluation

The following table details the mitigation strategies covered in this chapter. The radiation hardening by design strategy proposed by Sayil and Patel (2010) was implemented through the use of dynamic thresholds technique and the use of driver sizing, thus leading to the error improvement of 60% with the updated design having an additional reduction of area overhead of 30%. This strategy, however, must be used in tandem with aggressive driver sizing in order to achieve this level of improvement. Unfortunately, a known issue with the use of the dynamic threshold technique is that since the gates are tied to the bodies of the devices, the gate capacitances are much higher than those of a standard CMOS, thus placing a limit on speed with this strategy (Corsonello et al., 2012). It must also be noted the malleability of the substrate bias voltages when output switching cannot be inferred from input transitions, leading to energy wastage when the body capacitances are charged and discharged. This strategy is also not immune to the temperature dependence with regards to the threshold voltage, with severe fluctuations observed in a wider range of operating temperatures (Hidalga-W. & Deen, 2002).

A radiation hardening technique was presented that employs triple modular redundancy and RC filtering (Díez-Acereda et al., 2019). The use of RC filtering in this instance may in fact do more harm than good, as the filter has poor load capacity and small output current, thus making it unsuitable for a frequency synthesizer in the 0.18 μm technology node which would require a greater output current especially in aerospace applications (Chen et al., 2018). This also limits the use of this strategy to low frequency applications as the amplifier gain bandwidth product limits the operating frequency (Sanabria-Borbon & Sanchez-Sinencio, 2021). As the RC filter requires a large gain

bandwidth this also results in a filter that has a high-power consumption and wasted bandwidth.

Furthermore, the application of triple modular redundancy in this design in the frequency divider imposed an additional area overhead of 14% of the original design, excluding the area overhead imposed by RC filter. The use of triple modular is also still vulnerable to the occurrence of multiple bit upset, wherein the redundant circuitry is impacted by multiple particle collisions, thus providing a false positive to the majority voter, which selects for the majority output of the redundant circuits (Nowee, 2022). The triple modular redundancy mitigative strategy proposed by (Keller & Wirthlin, 2021) also poses similar disadvantages. While the strategy attempts to reduce the neutron cross section in order to reduce the output of observable errors, the application of this strategy still results in not only additional area overhead in the triplicated components, but also an increased consumption of routing resources in return for only partial error reduction coverage.

The 14T SRAM cell proposed by (Ahirwar et al., 2023) strives to reduce the number of sensitive nodes within its design and increase the write stability as well as include read upset immunity. The downside of the design is that the read access time was amongst the highest amongst other 14T SRAM designs. The design features a lower energy consumption for its read and write process, though it sacrifices speed for this improvement. As the design is intended for aerospace applications, a field in which requires higher speeds for real-time data processing, this may present a larger issue that is absent amongst existing 14T SRAM designs such as the high speed soft error aware SRAMs proposed by (Prasad et al., 2021). In short, the design compromises too much of its speed in favour of stability, to the point that existing designs have comparatively greater trade-off.

Rajendran et al. (2011) proposed sizing ratios that are capable of resulting in desirable trade-offs in terms of static noise margin, critical charge, delay and power. The approach, however fails to demonstrate feasibility of its application in advanced technology nodes as this method was only tested on the 6T SRAM architecture in the 32nm technology node. Furthermore, the data did not account for the differences in SRAM performances in read and write processes. Rahman et al. (2016) shows that the cell ratio sizing has a different effect on the static noise margins of a 6T SRAM at the technology nodes 32nm, 22nm and 16nm. This is expected as the read operation of the SRAM has the cell in its most vulnerable state, as the node being read has to charge or discharge the bit-line in order to provide a logical 1 or 0. Thus, the method presents its usefulness only in specific use cases, limiting its applicability as a strategy in soft error resistant circuit design.

Table 2.1: Comparison of mitigation strategies

Author	Year	Mitigation strategy	Purpose	Error rate improvement (%)	Area overhead improvement (%)	Summary
S. Sayil, N. Patel	2010	Radiation hardening by design	Increase robustness against soft error and soft delay	60	30	Dynamic threshold technique and driver sizing were used in tandem to significantly increase circuit robustness with minimal area increase

V. Díez-Acereda et al	2019	Radiation hardening by design	Design hardened by frequency synthesizer	50	14	The sensitive nodes of the circuit were identified and hardened using a resistor-capacitor filter and local redundancy
A. Keller, M. Wirthlin	2021	Triple modular redundancy (TMR)	Improving single event upset robustness of FPGA using partial TMR	34%	44%	Partial TMR was applied to selective portions of logic to improve protective coverage with reduced area overhead.
Ahirwar et al.	2023	Radiation hardening by design	Radiation-Hardened 14T SRAM	81.88	0	The 14T SRAM employs internal nodes between the memory nodes for additional node isolation.

Rajendran et al	2011	Radiation hardening by design	Transistor sizing ratio	58	-	Transistors were aggressively sized to increase the critical charge against soft errors.
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2.6 Summary

The chapter had covered multiple sources of soft errors and how the mechanisms of this concept was able to incite the errors in memory systems. The chapter also explains CMOS systems and how their designs can be vulnerable to soft errors. The techniques employed by contemporaries in the field to model soft errors in simulations in order to characterise and formulate the effects of single event upsets. The CMOS system of SRAMS and their various architectures, as well as modern improvements on their design are explained in further detail, as well as the mechanism of soft errors affecting the reliability of their systems. Finally, the types of mitigation techniques used in several different systems are discussed.

CHAPTER 3

THEORY AND METHODOLOGY

3.1 Overview

In this chapter, the methodology of the study will be explained in detail. An overview of the process flow of the study will be detailed here. The processes and software used, components used, circuit design, soft error simulation as well as robustness metrics will be detailed.

3.2 Project workflow

The project begins with the modelling of the circuit designs to be tested with the effects of soft errors as illustrated in Figure 3.1. As this study focuses on the effects of soft errors on CMOS memory systems, the test circuits will be CMOS SRAM cells. The cell designs tested will be the 4T, 6T and 9T SRAMs. The aforementioned cells are selected in order to test the robustness of each of the configurations and present a control case prior to the addition of the mitigation strategy in the form of the transmission gate transient filters.

These cells are first modelled in Cadence Virtuoso Silterra 18G version 1.8. Then the transient current as discussed in Equation 2.9 will be injected into the vulnerable nodes of the SRAM cells, that being the memory storage nodes Q and QB. This is done with the use of a current source with its parameters set to emulate the transient current model.

This error injection will have its amplitude varied until a change in state is observed. This step is done to determine the strength of the transient current required to overcome the stored data and flip from 0-1 or vice versa. This step will allow the determination of the critical charge of the cell configuration. This will be done under parametric variation of voltage supply and temperature to observe their effects on the soft error susceptibility of the

SRAM cell in accordance with those variables. The sensitivity of the cell to soft errors will then be calculated from the collected readings. The calculation of the probability would then be reproduced after the implementation of the soft error mitigation strategy, that being the transmission gate transient filter, to evaluate the change in critical charge and thus quantify the effectiveness of the strategy.

Once the transmission gate transient has been implemented, the steps done are then repeated to record the changes introduced and to recalculate the probability of soft error in the SRAMs. Once an observable reduction of soft error probability has been achieved the results will then be collected and elaborated upon as done in chapter 4.

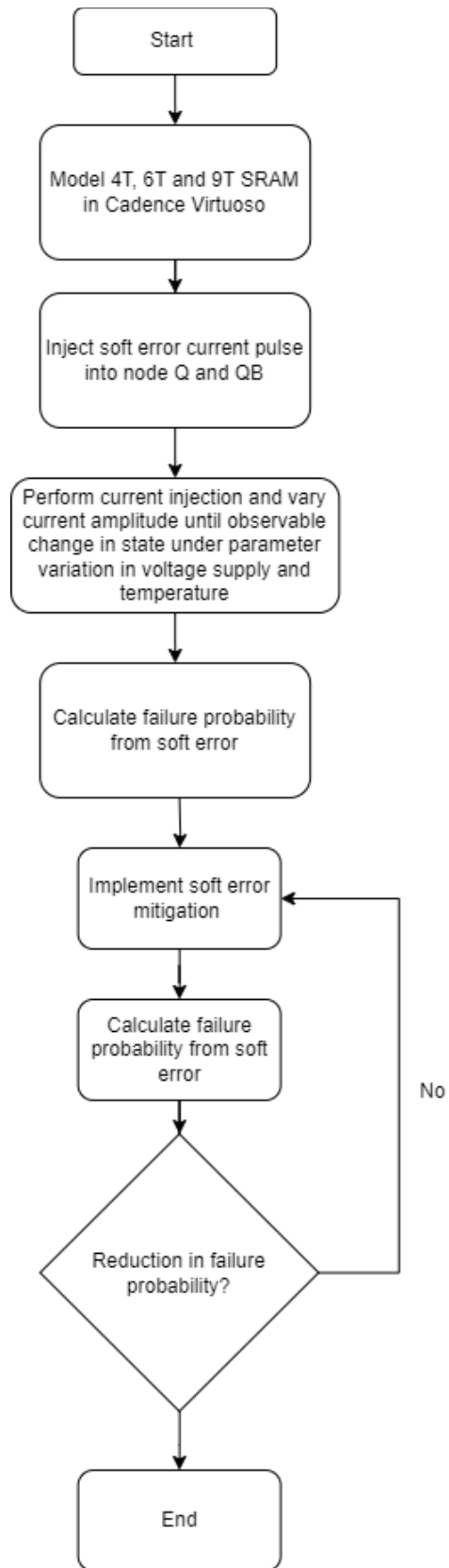


Figure 3.1: Thesis project workflow

3.3 Software

The software used is Cadence Virtuoso Silterra version IC5141USR3. The project was modelled with 180um PDK, with testing done under the Analog Environment.

3.4 Theory

3.4.1 Soft errors

The downscaling trend of development of integrated circuit has been revealed by (Petersen et al., 1982), presenting an increase in critical charge with each generation of feature size reduction. The research therefore illustrates a decades-long awareness and investigation into the phenomenon of single event upsets and its worsening effects on the reliability of circuitry in subsequent generations. Progress in CMOS technology brings increasing reductions in nodal capacitance, drive currents and supply voltages, increasing soft error rates. If gate outputs are flipped, these can result in single event transients, which can lead to soft errors if propagated into memory (Sayil & Patel, 2010).

3.4.2 Sources of Single Event Upsets

Single event upsets can occur from a number of different sources, namely those that contribute to an environment that introduce a higher concentration of particles that can potentially impact an electron within circuitry. These sources are elaborated upon within this following section as illustrated in Figure 3.2.

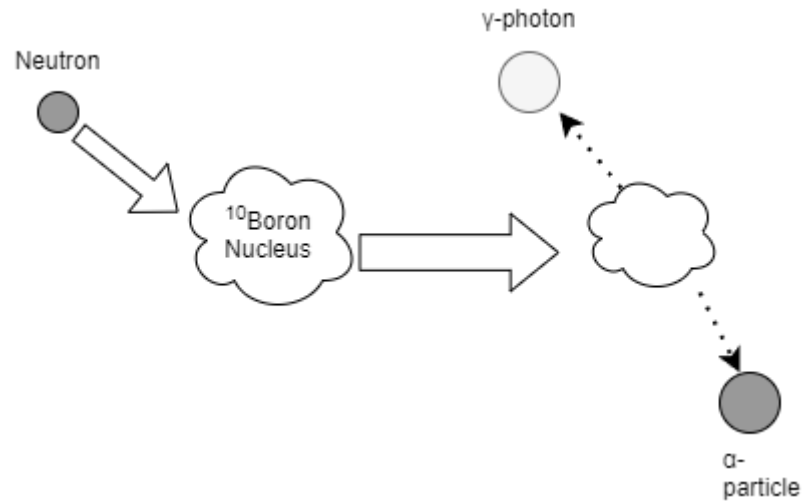


Figure 3.2: Boron fission reaction from neutron interaction

The presence of boron in many existing electronic devices makes them vulnerable to thermal neutrons as well, as evident in soft errors disrupting operations in large hadron colliders and their effect on accelerator processes (Cecchetto et al., 2020). Soft error mechanism

Free drift carriers can create a transient current pulse that will then elicit charge collecting at the affected node. Factors affecting the collection charge (Q_{col}), which is the charge generated and collected at a sensitive node during a particle strike, can include the qualities of the affecting particle and its collision trajectory, circuit dimensions, and bias conditions. If the (Q_{col}) is greater than the critical charge (Q_{crit}), which is the minimum charge required to induce a single event transient (SET), it may subsequently erroneously overwrite data if it reaches a storage element. There have been advances in the formulation of critical charge models. Roche et al. (1999) proposed that the transient current induced by ion strikes can produce a charge, modelled by:

$$Q = I_0 \cdot \tau = LET \cdot L \quad \text{Equation 3.1}$$

The linear energy transfer (LET) can be expressed as:

$$LET_{Threshold} = \frac{Q_{critical}}{L} \quad \text{Equation 3.2}$$

Based on this initial work, further advances have been made critical charge formulation. Autran (2015) proposed that the critical charge of a single event upset could be obtained by the following equation:

$$Q_{crit} = C_{node} \times \frac{V_{DD}}{2} \quad \text{Equation 3.3}$$

The "off" transistors in CMOS circuits struck by a heavy ion in the junction area are the most vulnerable to single event upset. Minority carriers are produced when these particles impact the silicon bulk, and if collected by the source and drain diffusion areas, the voltage value changes. When a particle hits the channel region of an off NMOS transistor or the drain region of an off PMOS transistor, it can cause a single event upset. In a p-n junction, ionisation can cause a current pulse and create a single event upset at the affected junction when the charge injected by the current pulse at a sensitive node exceeds the critical charge (Q_{crit}). Transients are distinct based on supply voltage, technology, output load and the energy and strike location of the particle. A particle track that goes across an n-diffusion layer in the off-state, holes can be moved out from the depletion layer and cause a single event fault (Ibe, 2015).

A single event transient is produced in Figure 3.3 when an ionising particle is introduced close to sensitive device nodes on silicon as presented in a paper by Baumann (2004). Along the particle track, a dense radial distribution of electron-hole pairs is

produced. If the ensuing ionisation track reaches the depletion zone, carriers are quickly absorbed by the electric field, compensating for the charge stored in the junction. The non-equilibrium charge distribution causes a transient funnel-shaped potential distortion along the event's track, boosting charge collection by drift.

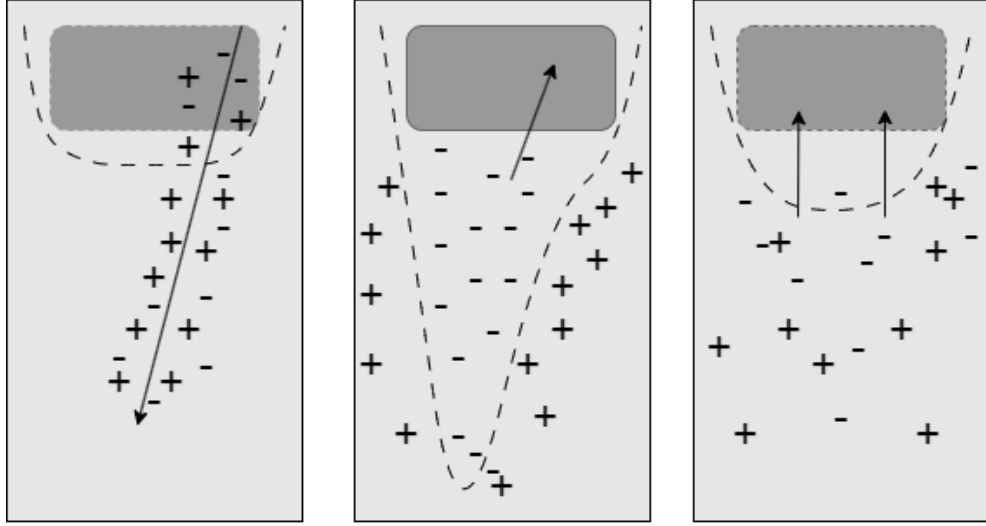


Figure 3.3: Charge collection in a silicon junction.

Consequently, a period of charge collection will commence as the funnel gradually collapses, which will then be followed by the diffusion process for the excess carriers until the junction area is free of charges. A current pulse will be created from the charges, lasting 200 picoseconds. A data flip may occur if the collected charge is (Q_{coll}) sufficient.

A model usually employed to analyse waveforms for induced transient currents uses a double-exponential form (Messenger, 1982).

$$I(t) = \frac{Q_{coll}}{\tau_\alpha - \tau_\beta} (e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}}) \quad \text{Equation 3.4}$$

$$Q_{coll} = 10.8 \times L \times LET \quad \text{Equation 3.5}$$

Collected charge is denoted as Q_{coll} , the collection time constant is $\tau\alpha$, and the time constant for ion-track to establish is $\tau\beta$. These timing constraints are tied to the technology used.

$$\tau\alpha = \frac{k\epsilon_o\epsilon_r}{q\mu N_D} \quad \text{Equation 3.6}$$

The equation can be defined as the Boltzmann constant defined by k , the permittivity of a vacuum defined by ϵ_o , the relative permittivity of silicon as ϵ_r , and the electron charge as q . N_D , and q define the donor density and the electron charge respectively, while μ is referring to the electron mobility. The charge collection depth (L in micron) is 2 per 1 MeV-cm²/mg linear energy transfer (LET), and an ionising particle deposits 10.8fC charge per micron in bulk silicon. The produced transient voltage pulse can go through multiple levels of logic gates. A single event upset can be induced if the channel region of a NMOS transistor in its off state or the drain region of a PMOS in its off state. The overall charge collected at the sensitive node, as well as the temporal form of the current pulse and the device supply voltage, all influence the critical charge. The interval after the particle strikes at which the impacted node voltage surpasses the threshold voltage is described as "switching time" or "feedback time. Detcheverry et al. (1997) states that the output node voltage propagation condition is formulated as follows:

$$V \geq \frac{Q_{\text{crit}}}{C} = \frac{1}{C} \int_0^{t_{th}} I_{\text{drain}}(t) dt \quad \text{Equation 3.7}$$

The capacitance and the time constant of the RC define the width of the voltage pulse. A reduced load capacitance will produce a larger voltage pulse from a single event upset given an equal charge.

i. Package devices

The fabrication process of any device can be susceptible to impurities affecting the robustness of the device to single event upsets. This can be due to the impurities being radioactive in nature. Traces of uranium and thorium may be contained in the packaging material of improperly purified metals, such as tin or lead used in soldering processes (Velazco & Franco, 2007). The impurities will undergo radioactive decay, releasing alpha particles from within the chip packaging.

Pollutants such as uranium and thorium can be produced or infused into materials during the manufacturing process at various levels, from wafer to interconnection. These materials are naturally occurring and can exist as impurities in water and raw materials, therefore soft error rate (SER) calculation must consider precision modelling of alpha particle activity in order to simulate its behaviour. The radioactive decay of substances such as uranium in materials like silicon would produce alpha-particles within the bounds of 19 to 46 μ m, outsizeing the dimensions of contemporary memory bit-cells (Weide-Zaage et al., 2016).

As the threshold to produce an electron-hole pair is at 3.6eV, and the energy of alpha particles can range from 3 to 7 MeV, if a vulnerable node in the combinational logic of a system was struck, the path from the ionisation can produce a huge number of pairs. The depletion regions of transistor drains or reverse-biased p-n junctions as well as the drain/well and drain/substrate junctions in CMOS transistors are especially vulnerable to these particle strikes (Sayil, 2019).

ii. Cosmic rays

The effects of cosmic rays interacting with circuit functionality are well recorded phenomena, with reports of satellites suffering from single particle upsets from as early as the 1970s (Guenzer et al., 1979). It was recognised as a problem that required mitigative measures especially for machinery that would be used to conduct procedures in the field of aerospace. The secondary ions produced from the reactions of cosmic ray-sourced neutrons with silicon nuclei within semiconductor devices remain a threat to device integrity even at ground altitude, but risk of soft error increases with the activity of neutron flux with a rise in altitude (Wang & Agrawal, 2008).

Furthermore, Gadlage et al. (2017) states that while electron-induced soft errors are less frequent in relation to direct ionisation from alpha or neutron particle collisions, areas in which they are relevant include the aerospace field, especially deep space excursions, high radiation medical environments such as x-rays or cancer treatment, or during the use of linear accelerators wherein soft errors may be triggered by the scattering of particles striking sensitive equipment.

A soft error is triggered through two methods of energy deposition for high energy electrons in silicon, which varies based on the level of energy deposited and the critical charge, namely direct and indirect ionisation (Alia et al., 2020). Alpha particles and its like cause soft errors through direct ionisation, producing soft errors when electron hole pairs are created along its travel path which result in a transient when the charge is accumulated at the affected node.

Indirect ionisation sees a particle, typically a neutron, and atom interaction that results in a nuclear reaction. The resulting reaction produces a greater volume of electron-hole pairs than those produced by the particle alone which then produce a soft error (Ranjan et al., 2022). A distinct aspect of indirect ionisation is that photons can be created from the

subsequent braking radiation of an electron strike or the electron itself which can produce energetic particles like alphas, neutrons and protons through photodisintegration or photofission.

iii. Boron and cosmic neutron interactions

As boron sees prolific use as a dopant for p-type in silicon and can lead to the induction of radiation when interacted with neutrons from cosmic rays. It is used as an additive to phosphosilicate glass to lower the contact soldering temperature. The boron isotope ^{10}B reacts dramatically to neutron interactions as seen in Figure 3.2, experiencing fission which produces a lithium recoil nucleus and alpha particle, both particles of which are capable of inducing soft errors in electronics (Baumann, 2001).

Due to fact that the concentration of ^{10}B in phosphosilicate glass in comparison to its content in implants and diffusion is many magnitudes higher, it presents a risk for soft errors when adjacent to a silicon substrate. This establishes borophosphosilicate glass (BPSG) as a substantial origin for boron fission and subsequent soft errors (Baumann, 2001).

3.5 Current pulse model

The current pulse that results from the particle strike must be modelled mathematically in order to perform simulations. The soft error model can be modelled as a double exponential current pulse as below;

$$I(t) = \frac{Q_{total}}{\tau_f - \tau_r} (e^{-t/\tau_f} - e^{-t/\tau_r}) \quad \text{Equation 3.8}$$

The model has a rapid rise time, τ_r , and then falls slowly, with falling time τ_f . Q_{total} represents the total charge derived from the current pulse produced by the single event upset **Figure 3.4**. The selected rise and fall times as proposed by (Cha & Patel, 1993), are 50ps and 164ps respectively, with a pulse width of 10ps. This is to reflect the collection and diffusion phase of the electron hole pairs during the particle strike.

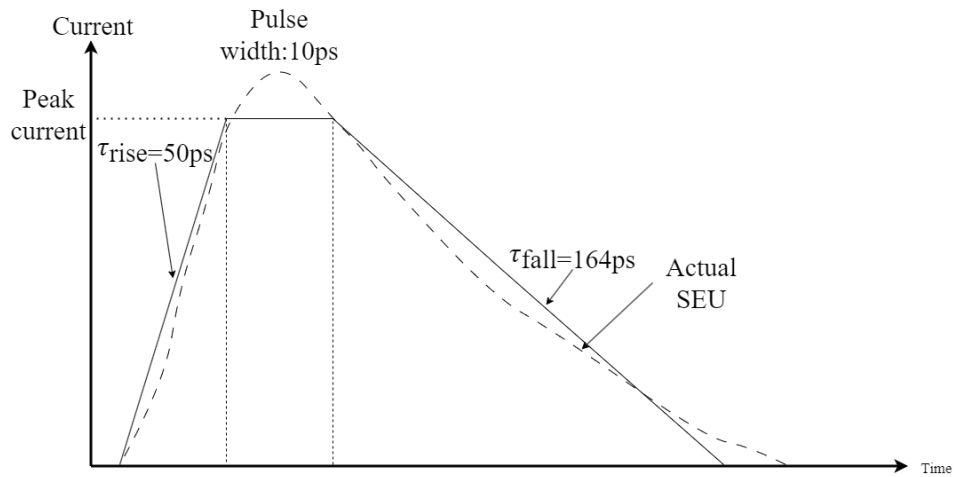


Figure 3.4: Soft error current model

3.6 Static Random Access Memory

Static random access memory (SRAM) is a highly important aspect of modern computing. It serves to provide an intermediary between high speed registers, and slower, large capacity memory storage.

3.6.1 6T SRAM

The 6 transistor (6T) SRAM consists of 6 MOSFET transistors, two of which are P-Channel MOSFETs (PMOS) and the remaining four are N-Channel MOSFETs (NMOS). The vulnerable points are the nodes Q and QB, which will serve as the injection points for

the current pulse. Figure 3.5 shows the schematic diagram of the 6T SRAM, with Figure 3.6 showing the same design as modelled in Cadence Virtuoso.

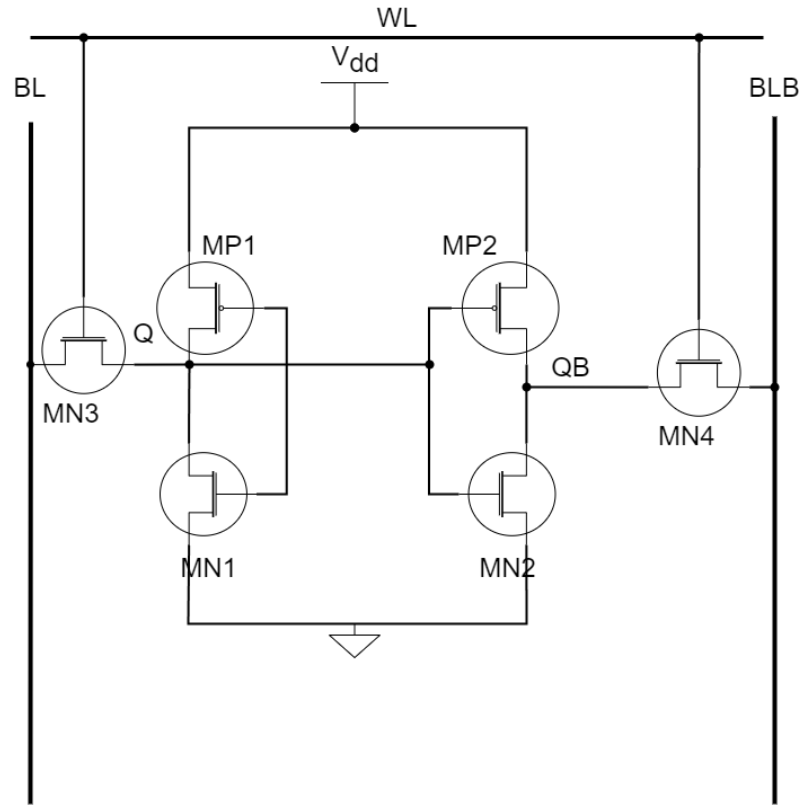


Figure 3.5: 6T CMOS SRAM cell

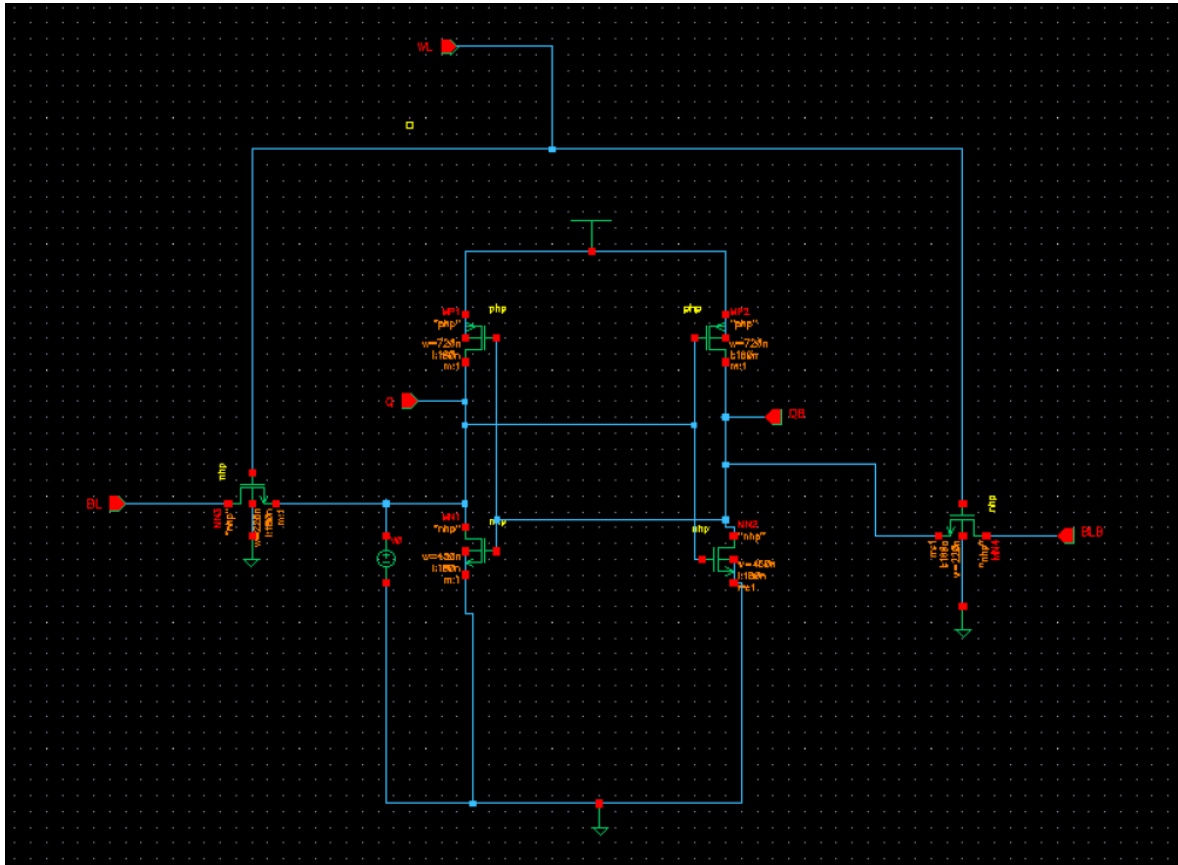


Figure 3.6: 6T SRAM in Cadence Virtuoso

i. Write operation

An inverter loop maintained by the two NMOS and PMOS transistors holds data that is written into it through the word line during a write operation. For a write operation, the word line will be turned on and activate the access transistors MN3 and MN4. This will allow access to the inverter loop. To write data '0' to Q, and '1' to QB, BLB will be charged to V_{DD} for logic level '1', while the BL will be driven to '0'. The transistor MP2 will be turned on and the voltage supply will pull QB to '1'. This will cause transistor MN1 to turn on and discharge node Q, reaching logic level '0'.

ii. Read operation

During a read operation, the bit line and bit line bar are pre-charged to voltage supply. To read data '0' from Q, and '1' from QB, the word line will be charged to engage the access transistors MN3 and MN4. The BL will discharge to ground through transistor MN1 and read as '0'. For the BLB, the transistor MP2 will be activated and cause BLB to be charged at voltage supply, allowing the node QB to be read as '1'.

iii. Hold operation

When the cell is idle, BL and BLB are kept at ground. The word line is disengaged, and thus the access transistors will be turned off. For as long as power is maintained to the cell, the data stored will be maintained by the PMOS transistors which will be at a complementary state. If Q is at '1', MP1 will be turned on and hold the value at V_{DD} . The transistor MP2 will then be turned off and node QB will be low, or '0'.

3.6.2 4T SRAM

The 4 transistor SRAM has four transistors in its implementation and polysilicon resistor loads in the place of PMOS transistors. The transistors employed are NMOS, due to their increased electron mobility relative to PMOS. It is also notable that while 4T SRAMs have been excluded in use in microprocessors due to the complexity of the fabrication process of its load element (W. Singh & Anil Kumar, 2015), it ultimately uses a lower cell current than its more modern descendants, the 6T and 9T SRAM. The circuit uses two polysilicon loads as pull up devices in place of PMOS transistors such as that in the 6T SRAM. Figure 3.7 shows the 4T SRAM schematic diagram while Figure 3.8 shows the 4T SRAM as modelled in Cadence Virtuoso.

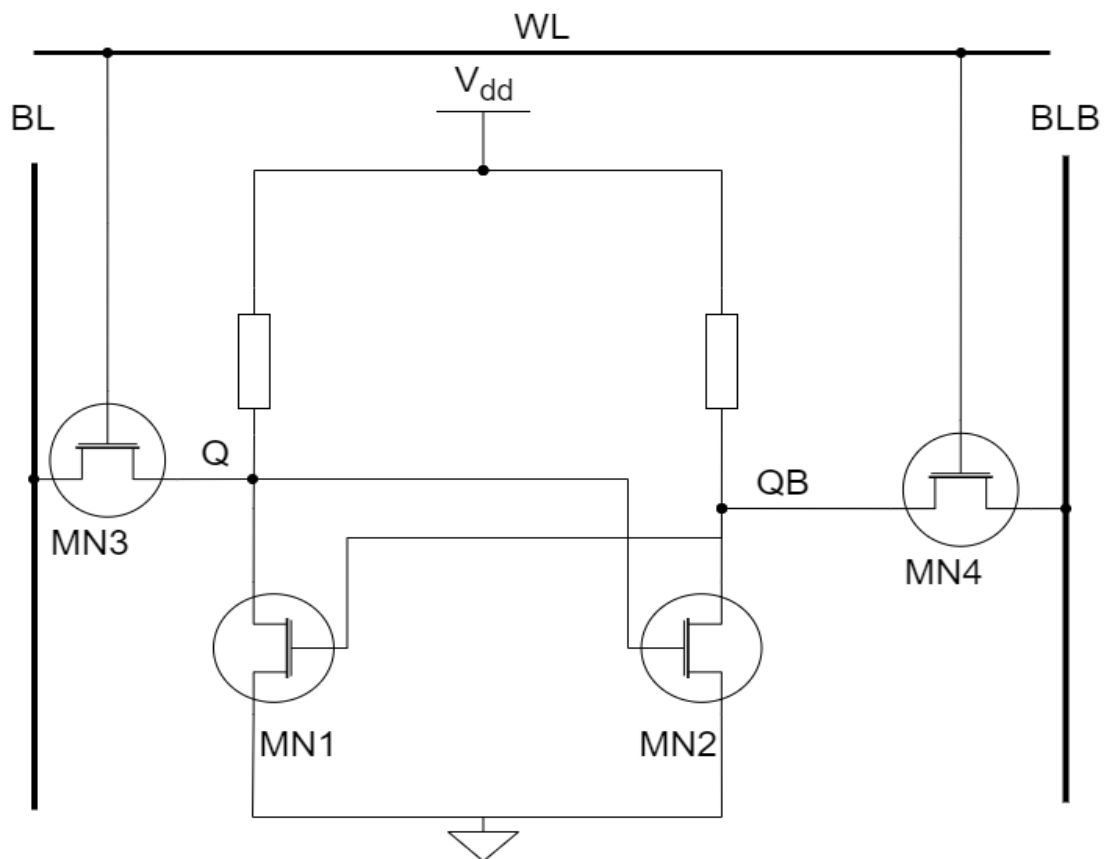


Figure 3.7: 4T CMOS SRAM cell

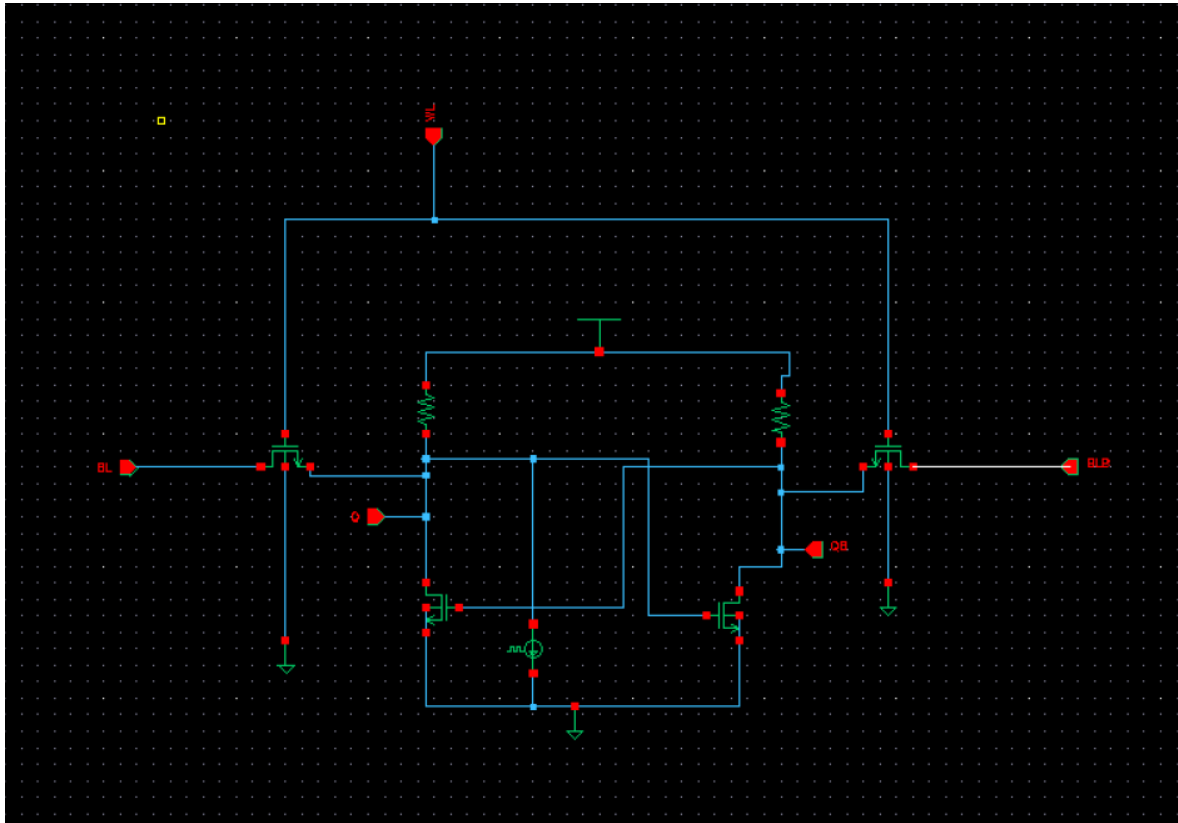


Figure 3.8: 4T SRAM in Cadence Virtuoso

3.6.3 9T SRAM

The 9T SRAM is similar in design to the 6T SRAM with an additional three NMOS transistors for a differential read that improves access time and stability. This causes a stronger pull-down effect, reducing the voltage rise at node during read operation. Figure 3.9 shows the schematic diagram for the 9T SRAM, while the Figure 3.10 shows the 9T SRAM as modelled in Cadence Virtuoso environment.

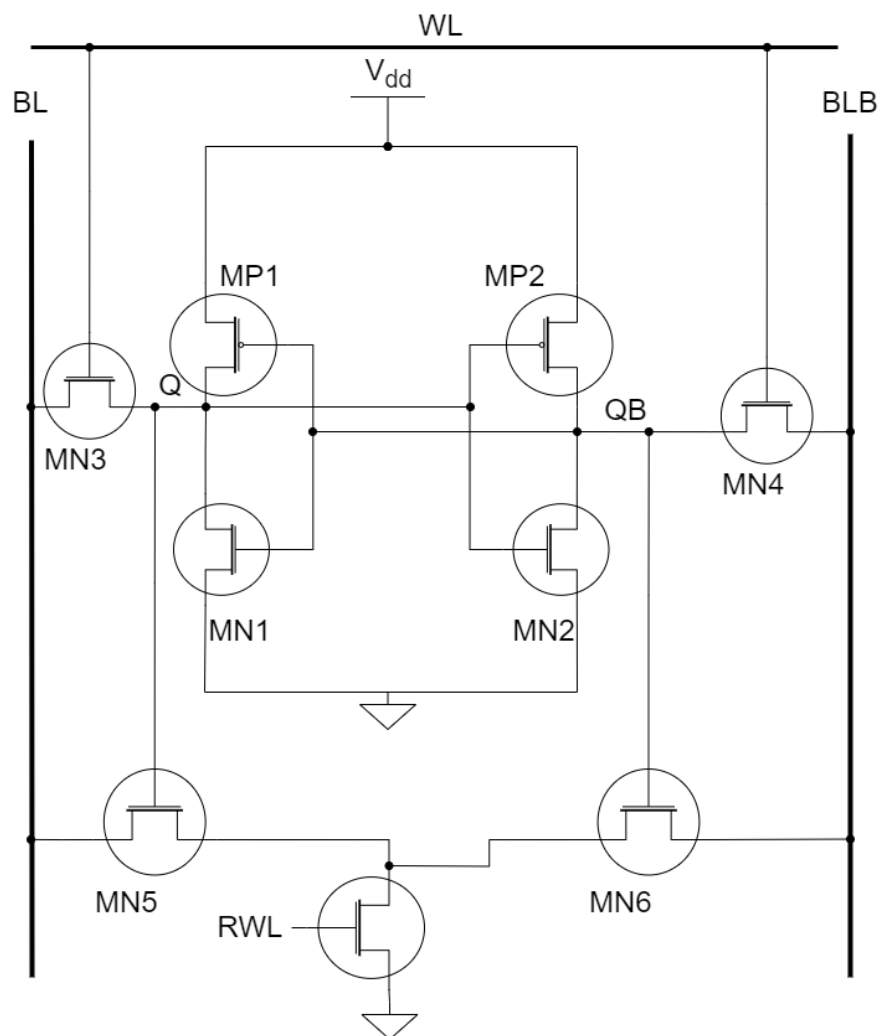


Figure 3.9: 9T SRAM cell

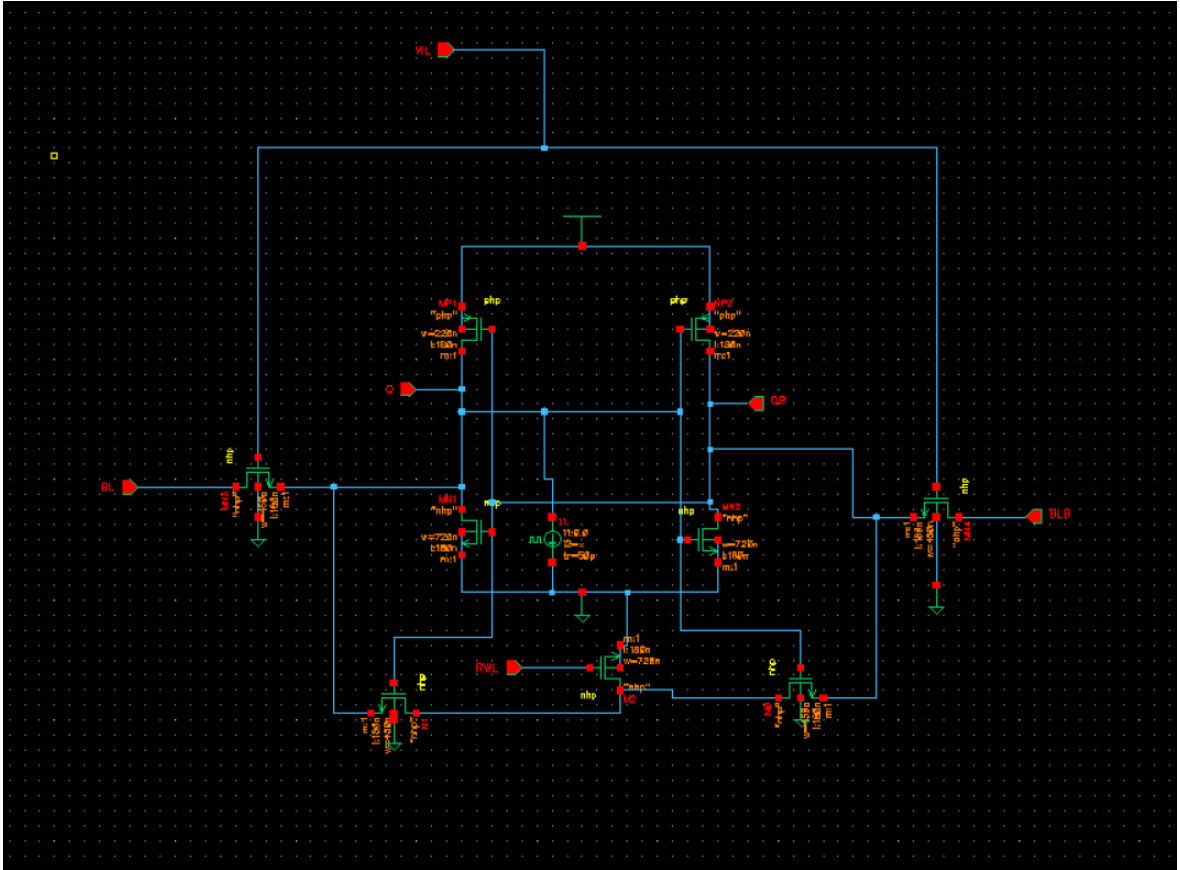


Figure 3.10: 9T SRAM as modelled in Cadence Virtuoso

3.7 Current pulse injection

The nodes Q and QB in each of the SRAMs will be injected with the current pulse modelled in Equation 3.. As the amplitude of the current injection is to be varied until a state flip occurs, the behaviour of the circuit response can be categorized into three scenarios, illustrated by Figure 3.11 and Figure 3.12.

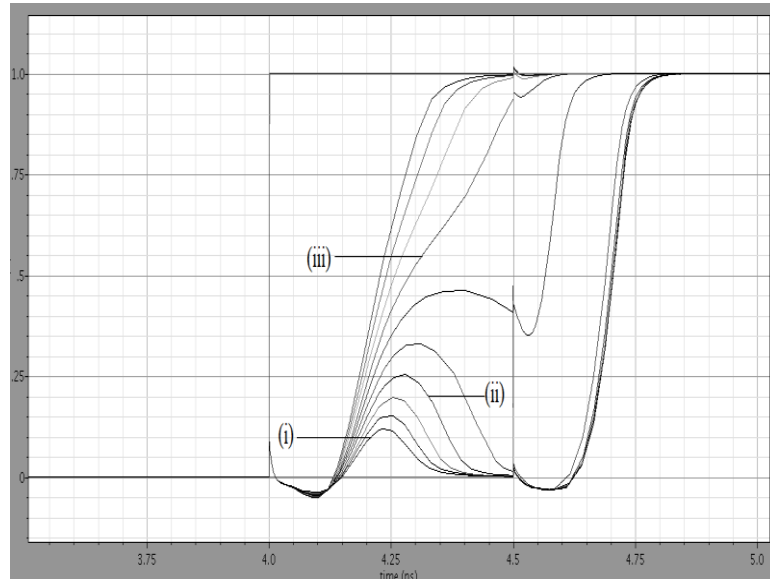


Figure 3.11: State holder change from low to high (0-1)

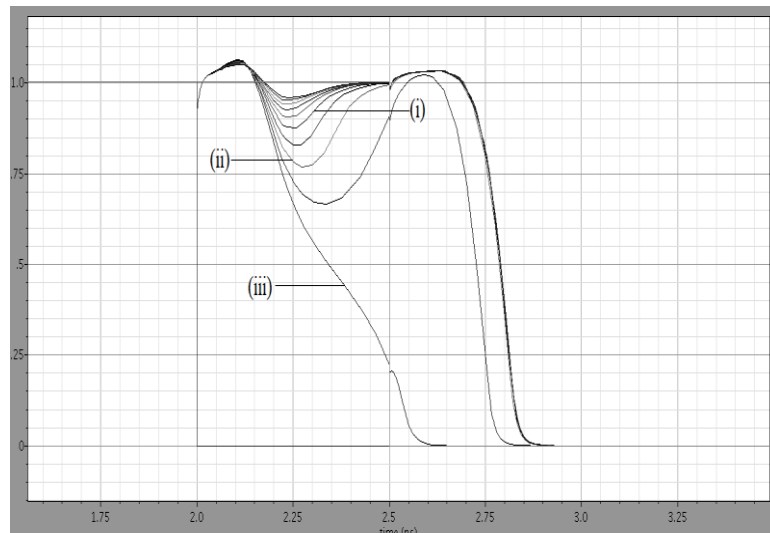


Figure 3.12: State holder change from high to low (1-0)

For the case of scenario (i), apparent in the change from low to high (0-1) in Figure 3.11 and high to low (1-0) in Figure 3.12. the subsequent pulse from the current injection does not cause a significant change in the state. The pulse is less than 20% of the original value and does not cause any lingering effects to the data stored. In scenario (ii) however,

the pulse generated is more than 20% of the supply voltage. While the pulse was not strong enough to incite a state change, it is strong enough to propagate through the system and ultimately cause systems to fail (Fuchs et al., 2009).

The soft error finally is able to incite a change in state as labelled in (iii), which illustrates the state changing from low to high in Figure 3.11 and high to low in Figure 3.12. The new, erroneous data is then able to propagate in the system and be read as such when the data is extracted from the SRAM cell. Parametric variations will also be implemented over the course of the simulations. As the nodes Q and QB are injected with the current pulse, the following variables will be observed;

- a) Supply voltage is ranged from 0.7V to 1.5V. The steps will be set at intervals of 0.1V. The temperature will be set at 27 °C
- b) Temperature is set at five points, namely -50 °C, 0 °C, 27 °C, 125 °C and 200 °C. These readings are taken with the supply voltage set at 1V.

The minimum current obtained from the readings must then be calculated to be presented as critical charge (Q_c). This is an indicator of the susceptibility of the system to be affected by soft error as an increased critical charge shows that the current pulse needed to overcome the original stored data must be stronger. The measure of critical charge against the variables of voltage supply and temperature will then be graphed. This is to illustrate the effects of changing voltage supply and temperature with greater clarity. The individual SRAM cell is tested to observe the response against single event upsets (Morifuji et al., 2007).

3.8 Soft error mitigation through transmission gate transient filter

Transmission gates see the most use as a bilateral switch, with complementary control voltages fed to the gates of the PMOS and NMOS. When the control voltage is low the switch is open, with the switch closing when the control voltage is high.

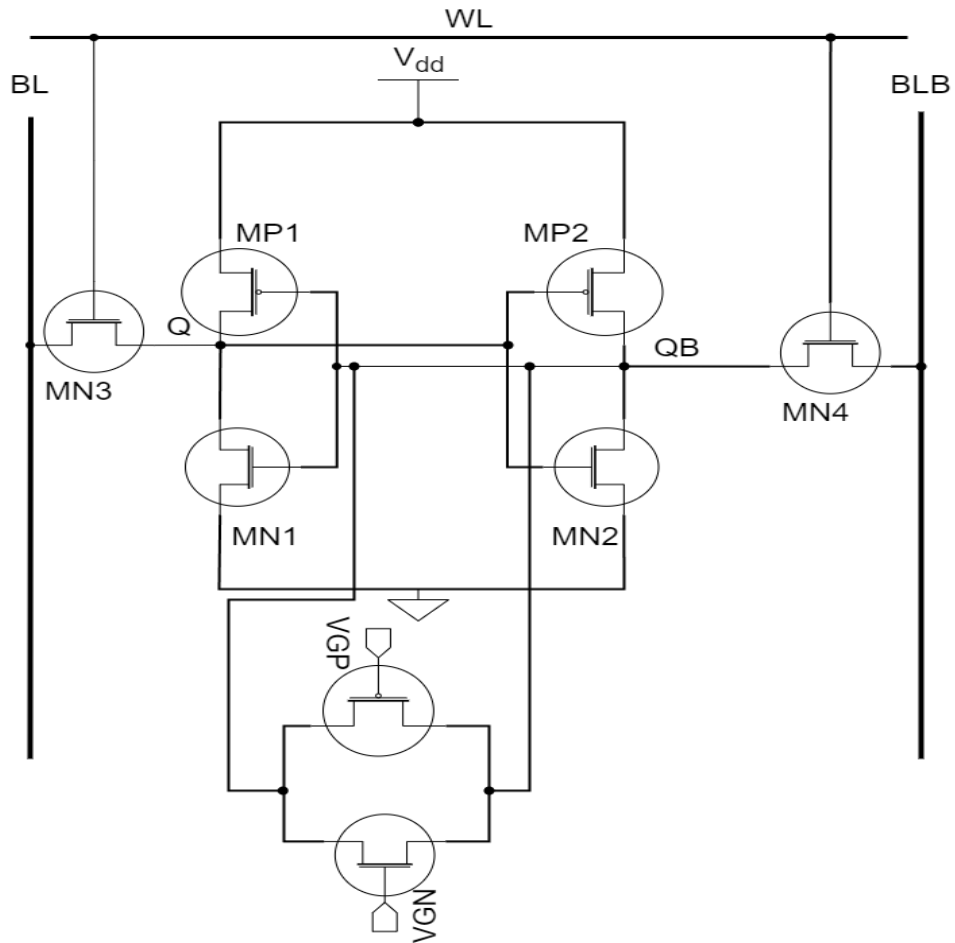


Figure 3.13: 6T SRAM with transmission gate filter

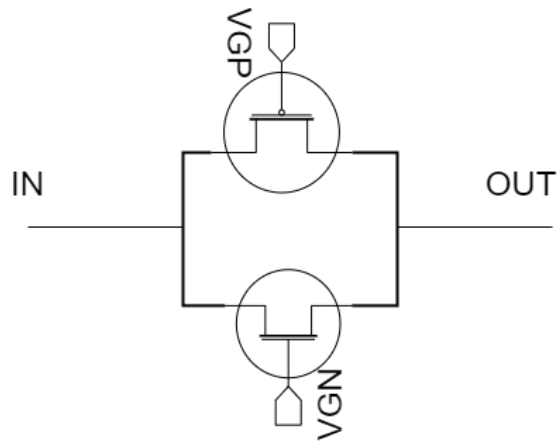


Figure 3.14: Transmission gate

Table 3.1: Truth table of transmission gate

Control	A	B
1	0	0
1	1	1
0	0	High impedance
0	1	High impedance

The width and length (W/L) sizing for the PMOS and NMOS transistors are 450nm/180nm. Transmission gates make use of symmetrical transmission gate sizing to simplify layout design and scaling, as well as allowing the gates to be controlled by the same signal, increasing efficiency and simplicity. The gate voltage of the NMOS transistor is tied to 0.67V and for the PMOS transistor it is 0.55V. The subthreshold resistance is used to achieve a filtering effect that will mitigate transient signals. The sizes of the transistors were

also selected to increase transistor resistance, which will come into play when parameter variations of temperature and voltage affect the robustness of the SRAM cell.

3.9 Probability formulation

Empirical data involving the charge collection of CMOS transistors when exposed to radiation has allowed the calculation of collection charge calculation for a given technology (Hazucha & Svensson, 2000). The equation for the scaling of collection charge for NMOS $Q_{s2,N}$, and PMOS, $Q_{s2,P}$ has been formulated as below.

$$Q_{s2,N} = \frac{fV_{2,N}}{fV_{1,N}} * \frac{fD_{2,N}}{fD_{1,N}} * Q_{s1,N} \quad \text{Equation 3.2}$$

$$Q_{s2,P} = \frac{fV_{2,P}}{fV_{1,P}} * \frac{fD_{2,P}}{fD_{1,P}} * Q_{s1,P} \quad \text{Equation 3.3}$$

Q_s refers to the scaling of the collection charge scaling. The collection charge based on respective technologies is denoted by the Q_{s2} and Q_{s1} . Equation 3. details the transformation that allows for the calculation to obtain the collection charge for NMOS, $Q_{s2,N}$, while the collection charge for PMOS, $Q_{s2,P}$, can be obtained through Equation 3.2. The doping effects is represented by $\frac{fD_2}{fD_1}$ while the V_{cc} scaling effect is represented by fV_2/fV_1 . The fV_1 and fD_1 of technology nodes of 0.8 μm ., 0.6 μm ., 0.35 μm . and 0.1 μm had been obtained by Hazucha and Svensson (2000). To obtain the fV_1 and fD_1 for the gate length of 0.18 μm , the equation was formulated in the NMOS and PMOS as below.

$$fV_N = 0. L_G + 1.01 \quad \text{Equation 3.4}$$

$$fV_P = \begin{cases} 0.32L_G + 0.79 & L_G \leq 0.35 \\ 0.0065L_G + 0.9 & L_G > 0.35 \end{cases} \quad \text{Equation 3.5}$$

$$fD_N = 1.4L_G + 0.14 \quad \text{Equation 3.6}$$

$$fD_p = 1.85L_G + 0.005 \quad \text{Equation 3.7}$$

Equation 3.3 denotes the graphical equation required to obtain the fV_N for a given gate length. Equation 3.4 shows the equation for calculating the fV_P given a specified gate length. Equations 3.5 and 3.6 show the calculation for obtaining the doping effect for NMOS and PMOS given a gate length. To find the collection charge Q_{s2} for NMOS, Equation 3.7 and 3.8 can be used. Equation 3.7 is obtained by substituting the Equation 3.3 and Equation 3.5 into Equation 3.1, and then simplified in Equation 3.8. Meanwhile, the collection charge for PMOS can be obtained from Equation 3.9, which is simplified in Equation 3.10. Equation 3.9 is derived from the substitution of Equation 3.4 and 3.6 into Equation 3.2. The gate length L_G of $0.18 \mu\text{m}$ can now be substituted into the Equation 3.8 to obtain the Q_{s2} for NMOS and Equation 3.9 for PMOS.

$$Q_{s2,N} = \frac{0.08L_G + 1.01}{fv_{1,N}} * \frac{1.4L_G + 0.14}{fD_{1,N}} * Q_{s1,N} \quad \text{Equation 3.8}$$

$$Q_{s2,N} = \frac{0.112L_G^2 + 1.44L_G + 0.14}{fv_{1,N}fD_{1,N}} Q_{s1,N} \quad \text{Equation 3.9}$$

$$Q_{s2,P} = \left[\begin{array}{l} \frac{0.32L_G + 0.79}{fv_{1,N}} * \frac{1.85L_G + 0.005}{fD_{1,N}} * Q_{s1,N} \quad L_G \leq 0.35 \\ \frac{0.0065L_G + 0.9}{fv_{1,N}} * \frac{1.85L_G + 0.005}{fD_{1n}} * Q_{s1,N} \quad L_G > 0.35 \end{array} \right] \quad \text{Equation 3.10}$$

$$Q_{s2,P} = \left[\begin{array}{l} \frac{0.59L_G^2 + 1.46L_G + 0.004}{fv_{1,P}fD_{1,P}} Q_{s1,P} \quad L_G \leq 0.35 \\ \frac{0.0129L_G^2 + 1.67L_G + 0.0045}{fv_{1,P}fD_{1,P}} Q_{s1,P} \quad L_G > 0.35 \end{array} \right] \quad \text{Equation 3.11}$$

To obtain the atmospheric cross section per unit area ρ_{ENV} for NMOS and PMOS, the formula for which is shown in Equation 3.11, the Equations 3.8 and 3.10 are substituted into Q_s . This allows for the derivations of Equation 3.12 and Equation 3.13 which is the atmospheric cross section per unit area for NMOS and PMOS respectively. The K denotes Coulomb's constant.

$$\rho_{ENV} = K \exp(-Q_{CRIT}/Q_s) \quad \text{Equation 3.12}$$

$$\rho_{N,ENV} = K * \exp\left(\frac{-Q_{CRIT}}{\frac{0.112L_G^2 + 1.44L_G + 0.14}{fv_{1,N}fD_{1,N}} Q_{s1,N}}\right) \quad \text{Equation 3.13}$$

$$\rho_{N,ENV} = K * \exp\left(\frac{-Q_{CRIT}}{\frac{0.59L_G^2 + 1.46L_G + 0.004}{fv_{1,P}fD_{1,P}} Q_{s1,P}}\right) \quad \text{Equation 3.14}$$

Table 3.2: Sensitive area for NMOS and PMOS of SRAM

No.	Item	Unit (m)
1.	$A_{NMOS,SRAM}^Q$	Sensitive drain area of NMOS at node Q
2.	$A_{PMOS,SRAM}^Q$	Sensitive drain area of PMOS at node Q
3.	$A_{NMOS,SRAM}^{QB}$	Sensitive drain area of NMOS at node QB
4.	$A_{PMOS,SRAM}^{QB}$	Sensitive drain area of PMOS at node QB

The calculation for the sensitive area of the SRAM is done by obtaining the area of the sensitive SRAM node Q and QB from the width and length of a given transistor as in Equation 3.14.

$$A_{PMOS,SRAM}^Q = length_{PMOS,SRAM}^Q \times width_{PMOS,SRAM}^Q \quad \text{Equation 3.15}$$

The total vulnerable area in the SRAM cell can be found in the equation below.

$$A_{vulnerable(SRAM)} = A_{NMOS,SRAM}^Q + A_{PMOS,SRAM}^Q + A_{NMOS,SRAM}^{QB} + A_{PMOS,SRAM}^{QB} \quad \text{Equation 3.16}$$

The probability of a data flip due to a single event upset can be expressed in Equation 3.16 for NMOS, $Prob_{NMOS}$ and Equation 3.17 for PMOS, $Prob_{PMOS}$. This is done by finding the atmospheric cross section per unit area multiplied with the area of a node as compared to the total sensitive area of the SRAM cell.

$$Prob_N = Kexp\left(\frac{-Q_{CRIT}}{\frac{0.112L_G^2 + 1.44L_G + 0.14}{f v_{1,N} f D_{1,N}} Q_{s1,N}}\right) \frac{A_{NMOS,SRAM}^Q}{A_{NMOS,SRAM}^Q + A_{PMOS,SRAM}^Q + A_{NMOS,SRAM}^{QB} + A_{PMOS,SRAM}^{QB}} \quad \text{Equation 3.18}$$

$$Prob_P = Kexp\left(\frac{-Q_{CRIT}}{\frac{0.59L_G^2 + 1.46L_G + 0.004}{f v_{1,P} f D_{1,P}} Q_{s1,P}} L_G \leq 0.35\right) \frac{A_{PMOS,SRAM}^Q}{A_{NMOS,SRAM}^Q + A_{PMOS,SRAM}^Q + A_{NMOS,SRAM}^{QB} + A_{PMOS,SRAM}^{QB}} \quad \text{Equation 3.19}$$

3.9.1 Probability calculation example

With reference to Equation 3.14, the area of the sensitive node in an SRAM must be obtained in order to evaluate the probability of data flips in comparison to the size of the total area of the given SRAM as given in Equation 3.15. The calculations for the for the area of 4T SRAM is as follows.

$$W/L \text{ of NMOS} = \frac{720nm}{180nm} \quad \text{Equation 3.20}$$

In Equation 4.1, the width length ratio of the NMOS transistor in the 4T SRAM must be calculated in order to obtain the area of the sensitive node. The area of the NMOS node is then calculated as below in Equation 3.21.

$$\text{Area of node NMOS} = 720nm \times 180nm = 129,600nm^2 \quad \text{Equation 3.21}$$

Then the total area of the sensitive nodes is found in Equation 3.22, before the ratio of a single node is calculated against the total area in Equation 3.23.

$$\text{Total area (2 NMOS)} = 129,600nm^2 \times 2 = 259,200nm^2 \quad \text{Equation 3.22}$$

$$\frac{\text{Node Q NMOS area}}{\text{Total area}} = \frac{129,600nm^2}{259,200nm^2} = \frac{1}{2} \quad \text{Equation 3.23}$$

The below sensitive area calculations apply for the 6T, 9T and transmission gate filter SRAM as the number and size of sensitive nodes are identical across the architectures.

$$W/L \text{ of NMOS} = \frac{720nm}{180nm} \quad \text{Equation 3.24}$$

$$\text{Area of NMOS at node Q} = 720nm \times 180nm = 129,600nm^2 \quad \text{Equation 3.25}$$

$$\begin{aligned} \text{Total area of NMOS (2 NMOS)} &= 129,600nm^2 \times 2 = \\ &259,200nm^2 \end{aligned} \quad \text{Equation 3.26}$$

The same is then done for the dimensions of the PMOS transistors.

$$W/L \text{ of PMOS} = \frac{220nm}{180nm} \quad \text{Equation 3.27}$$

$$\text{Area of PMOS at node Q} = 220nm \times 180nm = 39,600nm^2 \quad \text{Equation 3.28}$$

Then the total area of the PMOS transistors is obtained.

$$\text{Total area of PMOS (2 PMOS)} = 39,600nm^2 \times 2 = 79,200nm^2 \quad \text{Equation 3.29}$$

The total vulnerable area of the SRAM cell is then obtained.

$$\text{Total area} = 259,200\text{nm}^2 + 79,200\text{nm}^2 = 338,400\text{nm}^2 \quad \text{Equation 3.30}$$

If the targeted node is the PMOS drain then the calculation of the ratio of the given node over the total area of vulnerable nodes would be as in Equation 3.31. Equation 3.32 denotes the same formula for the NMOS drain instead.

$$\frac{\text{Node Q PMOS area}}{\text{Total area}} = \frac{39,600\text{nm}^2}{338,400\text{nm}^2} = 0.117 \quad \text{Equation 3.31}$$

$$\frac{\text{Node Q NMOS area}}{\text{Total area}} = \frac{129,600\text{nm}^2}{338,400\text{nm}^2} = 0.383 \quad \text{Equation 3.32}$$

Once the ratio of the vulnerable area of node to the total area of node is achieved, the probability of the given SRAM can then be calculated using the Equation 3.16 and Equation 3.17.

In order to achieve the value of the scaling of the collection charge for NMOS and PMOS which is $Q_{s2,N}$ and $Q_{s2,P}$, respectively, the collection charge for NMOS, $Q_{s1,N}$ and PMOS, $Q_{s1,P}$ is achieved from Hazucha & Svensson (2000).

$$Q_{s1,N} = 13 \quad \text{Equation 3.33}$$

$$Q_{s1,P} = 6.2 \quad \text{Equation 3.34}$$

The value of the collection charge for NMOS and PMOS which is $Q_{s2,N}$ and $Q_{s2,P}$ can then be derived from the impact of supply voltage scaling $\frac{fV_2}{fV_1}$ and impact of doping effect. $\frac{fD_2}{fD_1}$. The doping effect fD_1 and voltage scaling effect fV_1 of technology $0.1\mu\text{m}$ has

been obtained from Hazucha & Svensson (2000). The doping effect fD_2 can then be obtained using formula from Equation 3.3 and 3.4 and voltage supply scaling effect fV_1 of technology node can then be obtained using formula from Equation 3.4

The voltage supply scaling effect fV_1 of technology node can then be obtained using formula from Equation 3.3 for NMOS and 3.4 for PMOS. Next, the doping effect fD_2 can then be obtained using formula from Equation 3.5 for NMOS and 3.6 for PMOS. L_G is set to be 0.18 to represent the gate length of technology node 0.18 μm .

$$fV_N = 0.08 \times 0.18 + 1.01 = 1.0244 \quad \text{Equation 3.35}$$

$$fV_P = 0.32 \times 0.18 + 0.79 = 0.8476 \quad \text{Equation 3.36}$$

$$fD_N = 1.4 \times 0.18 + 0.14 = 0.392 \quad \text{Equation 3.37}$$

$$fD_P = 1.85 \times 0.18 + 0.005 = 0.338 \quad \text{Equation 3.38}$$

The next step is to then calculate the collection charge at technology 0.18 μm for NMOS $Q_{s2,N}$ and PMOS $Q_{s2,P}$ as in Equation 3.1 and 3.2 respectively.

$$Q_{s2,N} = \frac{1.0244}{1.1} * \frac{0.392}{0.28} * 13 = 16.949 fFC \quad \text{Equation 3.39}$$

$$Q_{s2,P} = \frac{0.8476}{0.82} * \frac{0.338}{0.19} * 6.2 = 11.4 fFC \quad \text{Equation 3.40}$$

The atmospheric cross section per unit area for NMOS, $\rho_{N,ENV}$ and PMOS, $\rho_{P,ENV}$ can then be obtained from Equation 3.12 and 3.13 respectively. The critical charge would be obtained from simulation based on supply voltage and temperature variation.

$$\rho_{N,ENV} = K * \exp\left(\frac{-Q_{CRIT}}{16.949}\right) \quad \text{Equation 3.41}$$

$$\rho_{P,ENV} = K * \exp\left(\frac{-Q_{CRIT}}{11.4}\right) \quad \text{Equation 3.42}$$

The probability of the data flip can then be calculated by multiplying the atmospheric cross section per unit area with the calculated area of the respective SRAM cell. The probability calculation for 4T SRAM for polyresistor node is shown in Equation 3.43 and NMOS node in Equation 3.44.

$$Prob_P = K * \exp\left(\frac{-Q_{CRIT}}{11.4}\right) 0.117 \quad \text{Equation 3.43}$$

$$Prob_N = K * \exp\left(\frac{-Q_{CRIT}}{16.949}\right) 0.383 \quad \text{Equation 3.44}$$

The probability of the 6T, 9T and transmission gate transient filter SRAMs referenced from Equation 3.16 and 3.17, can then be substituted with the Equation 3.43 and Equation 3.44. The values of the ratio of the vulnerable area from Equation 3.31 and Equation 3.32 are substituted in Equation 3.16 and 3.17 respectively as well to finally obtain Equations 3.45 and 3.46.

$$Prob_P = K * \exp\left(\frac{-Q_{CRIT}}{11.4}\right) 0.117 \quad \text{Equation 3.45}$$

$$Prob_N = K * \exp\left(\frac{-Q_{CRIT}}{16.949}\right) 0.383 \quad \text{Equation 3.46}$$

3.10 Summary

The chapter had detailed the workflow of the project with each step and decision-making process explained thoroughly. The chapter also explains the chosen model of soft

error injection as well as the specifications of the current pulse and the mode of entry into the system in Cadence Virtuoso. The SRAMs tested and their normal mode of operation is explained and the state under the which the SRAM cells will be tested has also been stated. Furthermore, the conditions for a successful and unsuccessful state flip were detailed. The test parameters of temperature and voltage supply were also included within the exposition of this chapter.

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Introduction

This chapter covers the results of the study conducted in detail, with accompanying graphical representations. The results are divided by the response of the critical charge to the parameter variations of supply voltage and temperature. These readings were taken for the read and hold states of the SRAM cell. The SRAMs tested were the 4T, 6T and 9T SRAMs, as well as the proposed transmission gate SRAM. The results were further scrutinized by finding the standard deviation of the critical charge to elucidate the magnitude of shift when imposed upon by the parametric variation of voltage and temperature. The probability of a data bit being erroneously flipped is then calculated for each SRAM iteration to illuminate the degree of resilience against soft errors with a novel formulation.

4.2 SRAM critical charge against voltage and temperature

4.2.1 4T SRAM

i. Read state

Figure 4.1 presents the response of the critical charge of the nodes Q and QB over the course of the variation in voltage (a) and temperature (b). Because the layout of the SRAM cell maintains symmetry, the critical charges for nodes Q and QB are equivalent in data states "0" and "1." The critical charges needed to switch data states from 0 to 1 and 1 to 0 for nodes Q and QB were explored over the voltage range of 0.7V to 1.5V and the temperature range of -50°C to 200°C. As depicted in Figure 4.1 (a) the rise in supply voltage corresponds to an increase in driving current and node capacitance, subsequently affecting the critical charge (Kumar et al., 2009) . This adds resilience to the cell, making it more

challenging to inadvertently overwrite stored data. On the other hand, the opposite is true for voltage reduction, wherein the cell becomes more susceptible to soft errors as the critical charge decreases.

For the 0-1 data flips, over the course of the voltage range from 0.7V to 1.5V, the critical charge increases by 417.42% for the node Q and 423.245% for the node QB. The slight variation of the critical charge despite the symmetry of the SRAM is due to the response of the simulation to the parametric variation and does not contribute to malfunctioning of the SRAM cell and is otherwise small enough to be considered negligible. The critical charge can be observed to increase steadily over the range of voltage supply values moving to the right of the graph, but the rise appears to slow as the voltage supply approaches 1.3V and beyond, showing that the effect of increasing the supply voltage on the critical voltage is lesser at this point. The effect of voltage supply on the critical charge increases as the voltage decreases, as shown by the steeper slope on the lower end of the voltage ranges. Similar findings have been reported in regards to voltage scaling effects on critical charge in nanometric (Soleimaninia et al., 2023).

The critical charge response to the parametric variation of temperature for data flips 0-1 and 1-0 are represented in Figure 4.1 (b). For the node Q, the reduction in critical charge is proportional to the increase in temperature as the drive current is weakened. The weakened drive current due to the increasing temperature thus results in a lower critical charge, leading to higher soft error susceptibility (Sootkaneung et al., 2018). The 0-1 data flip for the nodes Q and QB see a critical charge decrease by 43.3102% over the temperature change from -50°C to 200°C. For the 1-0 data flip, the critical charge for the nodes Q and QB decrease by 0.533%. The critical charge for the nodes holding “1” is much lower than that holding “0” due to the reduced pull-up power necessary to easily write “1” values into the PMOS

transistor in the inverter loop of the SRAM (Bajpai et al., 2021). Thus, it is apparent that it is much easier for the data flip 1-0 to occur, as reported by the lower critical charge.

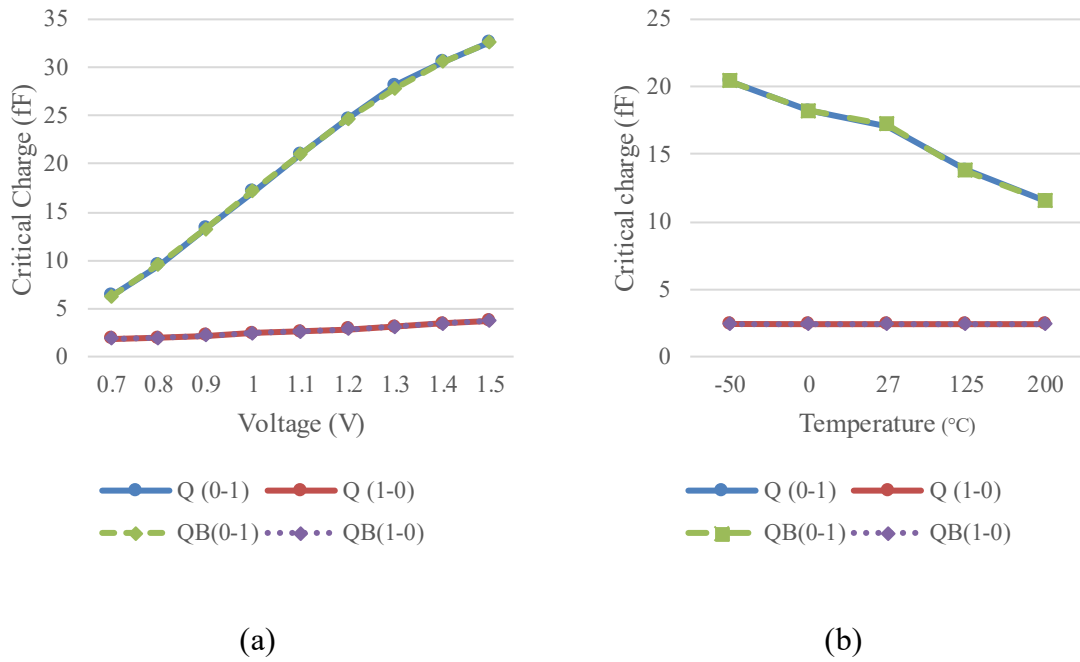


Figure 4.1: Graph of critical charge of 4T SRAM in read state against (a) voltage and (b) temperature

ii. Hold state

The same procedure was done on the 4T SRAM cell in the hold state. Figure 4.2 (a) illustrates critical charge over the voltage variation from 0.7V to 1.5V. The critical charge increases by 504.753% for the data flip 0-1 for the nodes Q and QB. The critical charge for the hold state is higher than that of the read state because the access transistors are not engaged in the hold state. In the read state, the internal storage node increases to be greater than ground, making it vulnerable to noise, and thus soft error transients are able to easily overwrite the data (Grossar et al., 2006b). The charge needed to flip the bit from 1-0 for the nodes Q and QB increases by 137.451% over the range of the voltage increase.

Figure 4.2 (b) shows the critical charge of the 4T SRAM against temperature variation. As the temperature is increased the critical charge decreased in turn, consistent with electrical response to heightened temperature parameters. Transistors in the ON state have a lowered drain current in high temperatures, hence transient pulses in the OFF state transistors of the node can override the former (Farjallah et al., 2018). The nodes Q and QB see a reduction in critical charge of about 37.12% and 37.44% for the data flip of 0-1. For the data flip of 1-0, the nodes Q and QB decreased by 3.99% and 5%. The variation of the critical charge for the 0-1 data flip is much greater than that for 1-0, as the critical charge of the PMOS is lesser than that of NMOS due to the smaller pull up ratio resulting in a weaker resistance to transient current pulses.

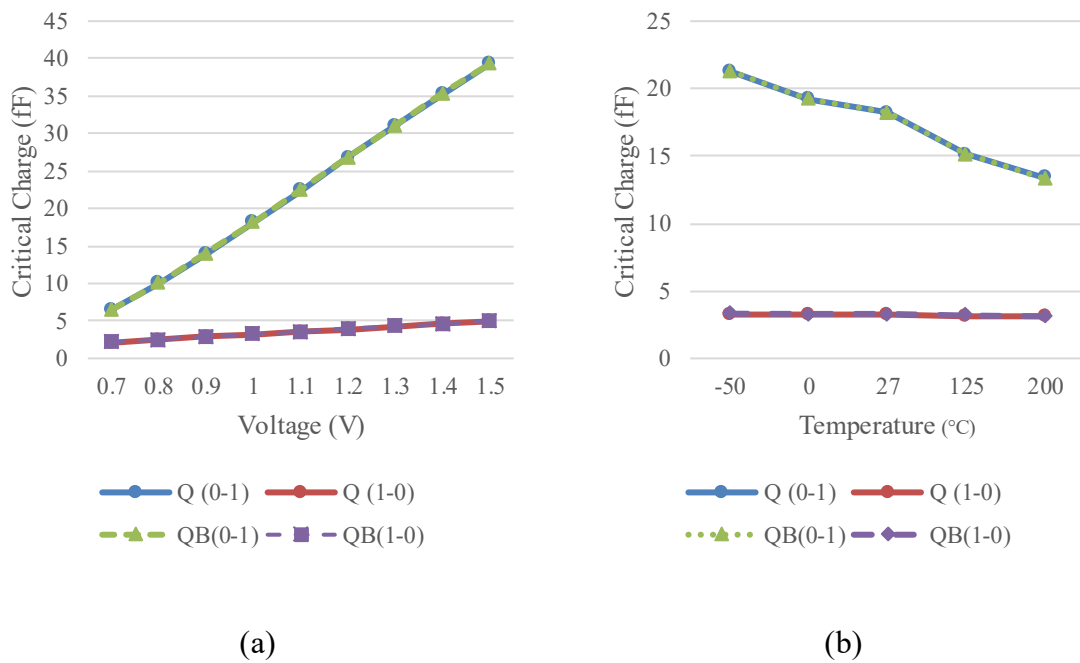


Figure 4.2: Graph of critical charge of 4T SRAM in hold state against (a) voltage and (b) temperature

4.2.2 6T SRAM

i. Read state

The critical charge required for the conventional 6T SRAM's read operation was determined. Figure 4.3 illustrates the variation in critical charge concerning changes in voltage (a) and temperature (b). The critical charge for transitioning from 0 to 1 experiences a 357% increase, while the transition from 1 to 0 sees a rise of 123.78% with escalating voltage. In the case of nodes Q and QB during the 1 to 0 state transition, the critical charge is notably lower, attributable to the smaller PMOS sizing that accommodates the requirement for a weaker pull-up power, essential for writing new data into the inverters (Jahinuzzaman et al., 2008a). Moving to Figure 4.1 (b), the graph showcases the critical charge variation across temperatures ranging from -50°C to 200°C. The elevation in temperature leads to a decline in carrier mobility, albeit to a lesser extent compared to fluctuations in the voltage supply, as seen earlier in Figure 4.1 (a) (Nie et al., 2017). Similar to the voltage variation, the critical charge for the 1 to 0 transition remains lower than that for the 0 to 1 transition. With an increase in temperature, the critical charge diminishes by 38% for 0 to 1 and 9% for 1 to 0.

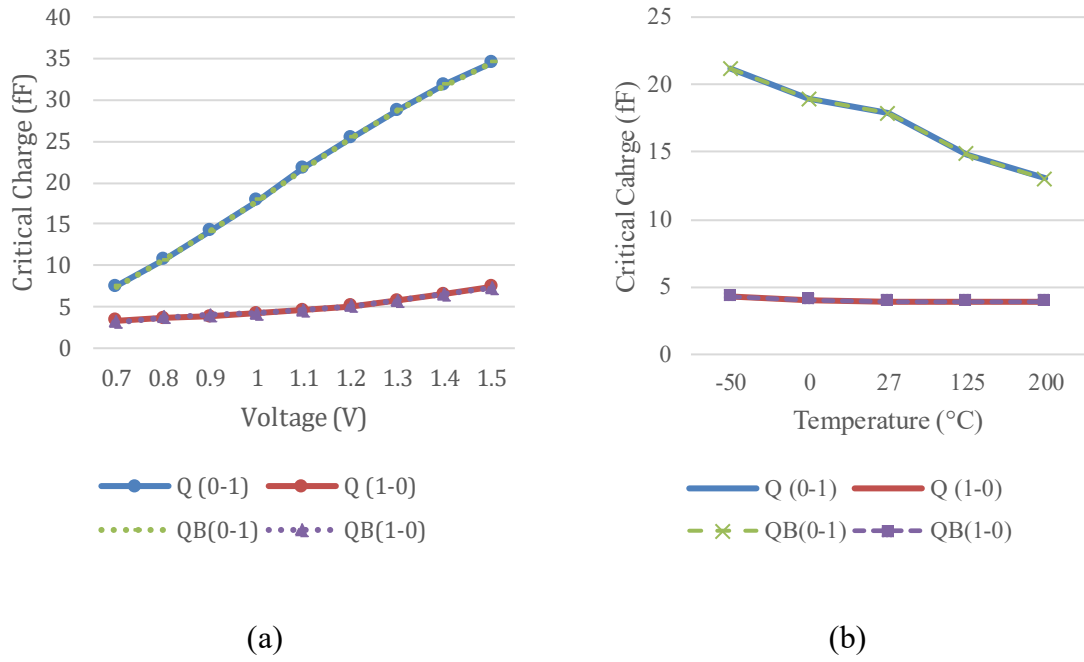


Figure 4.3: Graph of critical charge of 6T SRAM in read state against (a) voltage and (b) temperature

ii. Hold state

Figure 4.4 displays the critical charge during the "hold" state, subjected to variations in voltage supply and temperature. The critical charge exhibits comparable patterns to those observed in the "read" state when influenced by voltage and temperature changes, albeit with a diminished effect due to the "read" state being more vulnerable to potential data overwrites, given the connection to precharged bitlines. With an escalation in voltage supply, there's a corresponding elevation in the critical charge. Consequently, for the transitions 0-1 and 1-0, the charge of nodes Q and QB undergoes increments of 404% and 184% respectively as illustrated in Figure 4.2 (a). Figure 4.2 (b) shows that the critical charge in terms of temperature response, the critical charge dwindles as temperature rises and weakens the CMOS drive current due to lower mobility at higher temperatures (Bagatin et al., 2012). Over the range from -50°C to 200°C, the critical charge for nodes Q and QB displays

reductions of 34.26% and 5.81% for the transitions 0-1 and 1-0, respectively. To compare the critical charges from “read” to “hold,” the 6T SRAM’s critical charge at 1.5V experiences increments of 16.17% and 54% for transitions 0-1 and 1-0, correspondingly. At 0.7V, these increments stand at 5.24% and 21.31% for transitions 0-1 and 1-0 respectively.

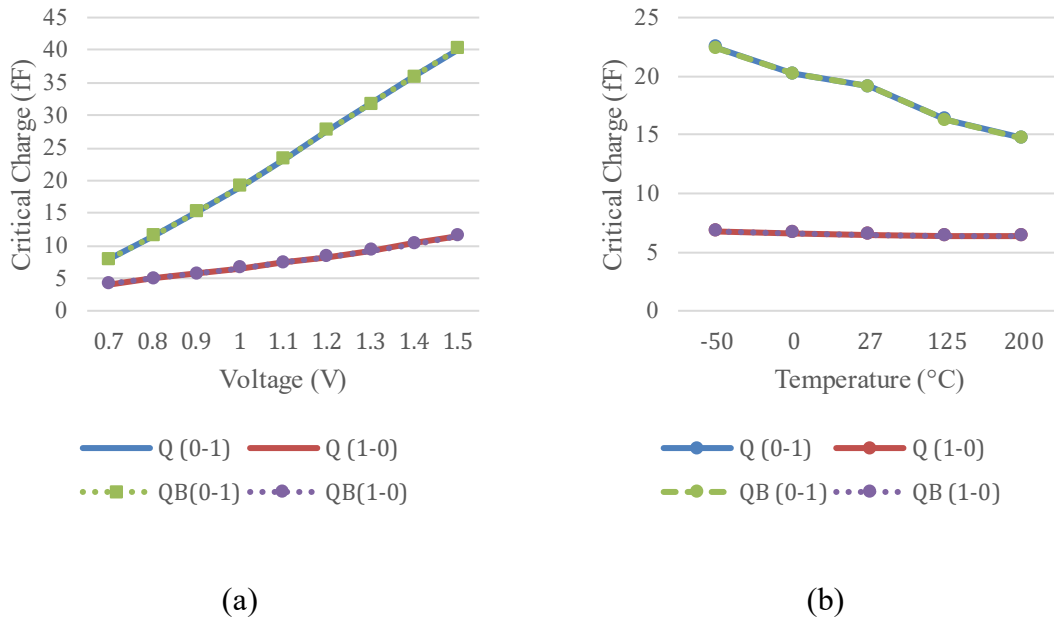


Figure 4.4: Graph of critical charge of 6T SRAM in hold state against (a) voltage and (b) temperature

4.2.3 9T SRAM

i. Read state

Attention was then focused on the response of the 9T SRAM critical charge to the temperature and voltage supply variation. The trend of the critical charge is similar to that of the 6T and 4T SRAM, with a higher overall critical charge due to the read state isolation mechanism that produces a strong pull down, affording the design more resilience against the single event transient current model overwriting the data (Athe & Dasgupta, 2009). Figure 4.5 (a) shows the critical charge over the change of voltage supply and Figure 4.5 shows the temperature variation critical charge response for the read state of the 9T SRAM.

With regards to Figure 4.5 (a), the critical charge for the data transition of 0-1 increased by 404.82% as the voltage increased from 0.7V to 1.5 for both node Q and QB. The critical change, when data changes from 1-0, sees an increase that mirrors the voltage supply increase. The nodes Q and QB see an increase of 166.62% over the ranges of voltage increase. The effects of the temperature increase on the critical charge of the 9T SRAM is illustrated in Figure 4.5 (b). The trend for both nodes at states 0-1 and 1-0 presents a decline with rising temperatures as the carrier mobility decreases and becomes more vulnerable to data bit corruption(Shah & Waltl, 2020). Thus the critical charge response shows a reduction of 37.9% for data transition of 0-1 and 3.4% for 1-0.

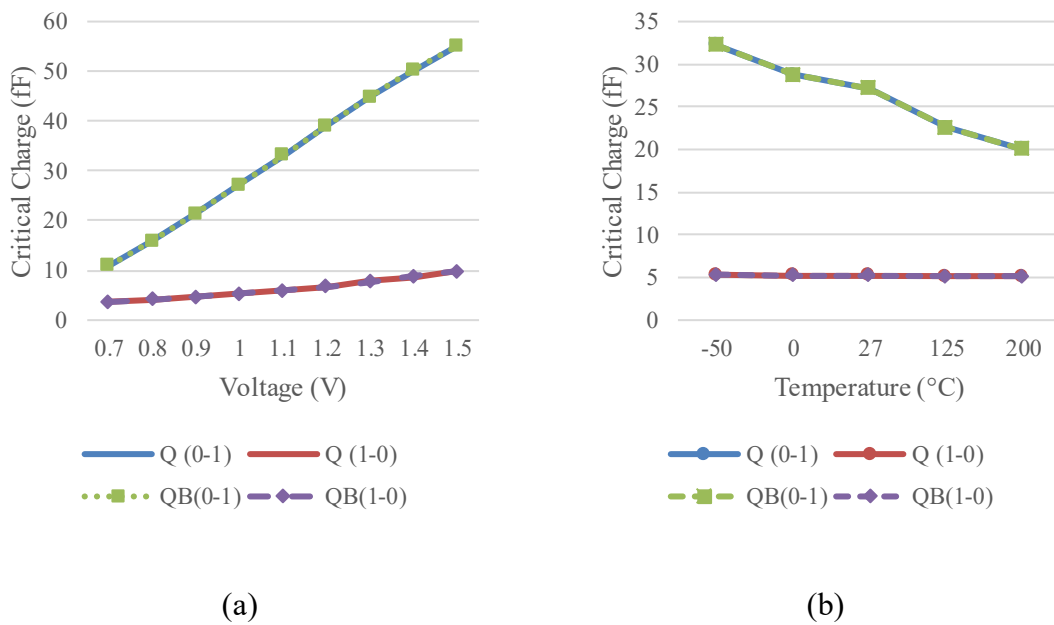


Figure 4.5: Graph of critical charge of 9T SRAM in read state against (a) voltage and (b) temperature

ii. Hold state

The results of the critical charge response to parameter variation for the hold state of the 9T SRAM is detailed as in Figure 4.6. The voltage variation is illustrated in Figure 4.6 (a) and the temperature variation in Figure 4.6 (b). For the data being flipped from 0-1, the

critical charge increased by a total of 343.636% as the voltage is increased from 0.7V to 1.5V. For 1-0, the critical charge rose by 165.96% over the increases of the same range. In Figure 4.6 (b), the graphical representation of the critical charge trend in response to temperature variation is shown. The data flip for 0-1 and 1-0 decreased by 43.11% and 3.77% respectively.

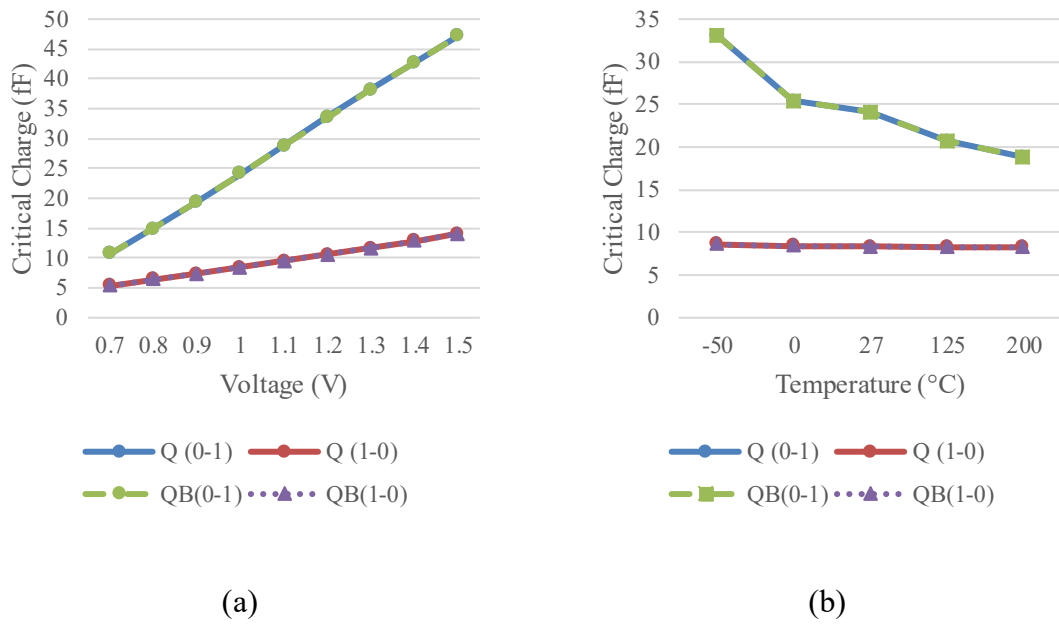


Figure 4.6: Graph of critical charge of 9T SRAM in hold state against (a) voltage and (b) temperature

4.2.4 SRAM with transmission gate filter

i. Read state

The susceptibility to single event upsets in the 6T SRAM is concentrated on two specific memory storage nodes, denoted as Q and QB, which are part of the inverter loop (Jahinuzzaman et al., 2008b). To assess how sensitive the proposed SRAM cell is to these upsets, we conducted experiments involving the injection of a double exponential current source into these storage nodes. Figure 4.7 illustrates the variation in the critical charge of

nodes Q and QB in the SRAM during read operations. This variation is observed under different supply voltages and temperatures to understand its impact.

In the context of Figure 4.7 (a), as the supply voltage increases, the critical charge also increases. This phenomenon occurs because the driving current and node capacitance increase correspondingly. Specifically, when transitioning from data state 0 to 1, as the supply voltage changes from 0.7V to 1.5V, nodes Q and QB experience a respective increase of 48.05% and 48.36% in critical charge. Similarly, when transitioning from data state 1 to 0, the critical charge for nodes Q and QB increases by 42.49% and 42.59%, respectively. Notably, it's observed that the critical charge for nodes holding "1" is significantly smaller than for those holding "0." This disparity arises due to the SRAM's design, where the PMOS is intentionally sized smaller than the NMOS to maintain a lower pull-up ratio, preventing unintended data overwrites during read operations (Fischer et al., 2008).

In Figure 4.7 (b), when subjecting the proposed circuit to varying temperatures, a rise in temperature leads to a decrease in critical charge, indicating an increased susceptibility to single event upsets at higher temperatures. Across the temperature range from -50 °C to 200 °C, the critical charge required to flip a bit from "0" to "1" for nodes Q and QB decreases by approximately 42.2% and 42%, respectively. Conversely, to flip a bit from "1" to "0," the critical charge decreases by approximately 14.54% and 14.22% for nodes Q and QB, respectively. This decrease in critical charge is attributed to the reduced carrier mobility of the devices at higher temperatures, resulting in a lower critical charge threshold.

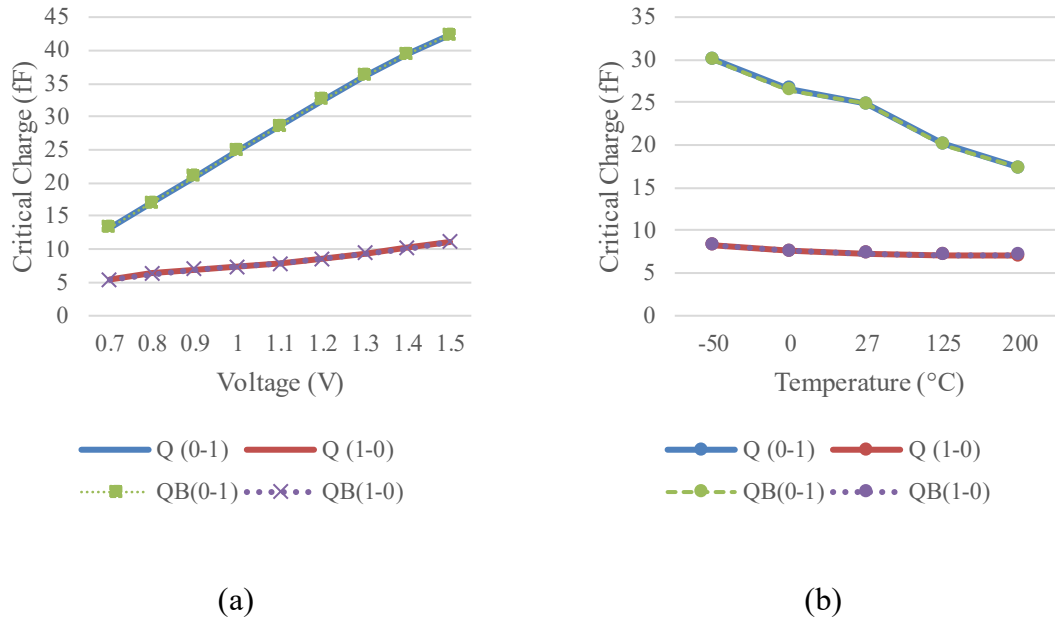


Figure 4.7: Graph of critical charge of transmission gate filter SRAM in read state against (a) voltage and (b) temperature

ii. Hold state

The critical charge trends in the hold state mirror those observed in the read state, both concerning voltage and temperature. However, the critical charge in the hold state is higher because the nodes are set to the supply voltage (Marques et al., 2021). Figure 4.8 (a) and (b) depict the critical charge response of the SRAM in the hold state to variations in voltage and temperature, respectively. Increasing the voltage, regardless of the state being held, leads to a corresponding increase in the critical charge of nodes Q and QB. However, this increase is more pronounced when the node is holding a "0" due to the smaller size of the PMOS transistor (Black et al., 2015).

Specifically, as the voltage is raised, the critical charge required to flip a bit from "0" to "1" for nodes Q and QB increases by approximately 54.6% and 54.9%, respectively. This is expected since a higher supply voltage makes the nodes less susceptible to transient

current injection. Conversely, to flip a bit from "1" to "0," nodes Q and QB experience a critical charge increase of 39% within the voltage range of 0.7V to 1.5V. Regarding temperature variation in Figure 4.8 (b), the observed trend closely resembles that seen in the read state simulation. When transitioning from "0" to "1," the critical charge for nodes Q and QB decreases by about 35.77% from -50 °C to 200 °C.

Conversely, when flipping a bit from "1" to "0," nodes Q and QB experience a decrease in critical charge of approximately 9.55% and 9.67%, respectively. Consequently, higher temperature levels render the system more susceptible to single event upsets. Comparing the read state to the hold state, at a voltage level of 1.5V, the critical charge of the TG SRAM increases by 12.68% for the 0-1 transition and by 41.5% for the 1-0 transition. At 0.7V, the critical charges for the 0-1 and 1-0 transitions increase by 6.7% and 26.16%, respectively, when moving from the read state to the hold state.

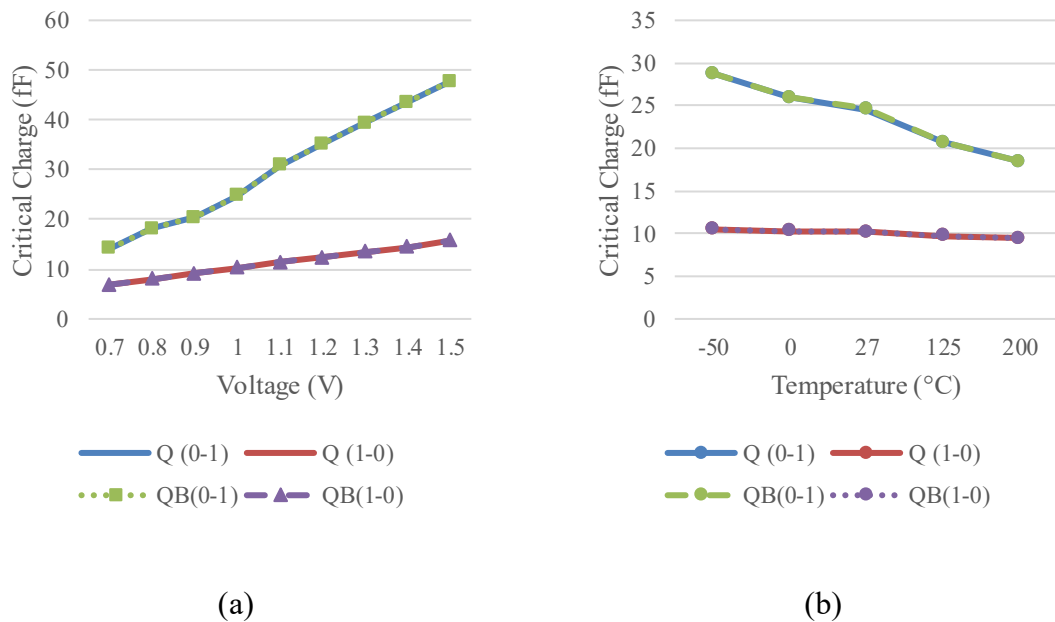


Figure 4.8: Graph of critical charge of transmission gate filter SRAM in hold state against (a) voltage and (b) temperature

4.3 SRAM Standard deviation

4.3.1 4T SRAM

As shown in Figure 4.9, the standard deviation of the critical charge of the 4T SRAM was obtained to evaluate the impact of voltage and temperature at the nodes Q and QB at the read (a) and hold states (b).

For the read state in Figure 4.9 (a), it should be noted that as the standard deviation of the temperature at the data flip of 1-0 is less than 1, the impact of temperature on the node holding a “1” value is very small in comparison to voltage, coupled with the miniscule initial critical charge, any observable variation was ultimately minimal. The 4T SRAM makes use of polyload resistors for the pull up network and two pull down NMOS transistors. While the size advantage is substantial compared to other SRAM configurations, the use of resistors presents a major weakness in regard to soft error resilience, as illuminated by the relatively small critical charge (Chandra, 2021). The 0-1 data flip is much larger when compared to that of the 1-0 standard deviation, though pales in comparison to the effect of voltage on critical charge. It is apparent that the manipulation of voltage supply has a much greater impact on the critical charge than that of temperature variation.

A similar trend can be observed in the hold state of the SRAM in Figure 4.9 (b). As the access transistors are not engaged in the hold state of the 4T SRAM operation, the critical charge is much higher in comparison as the inverter loop is isolated from the bitline and the auxiliary circuitry, resulting in added defence against single event transients. The standard deviation for the voltage for the data flip of 0-1 is the highest and is consistent with node Q or QB due to the symmetrical nature of the 4T SRAM. On the other hand, the 1-0 standard deviation is much reduced due to the smaller ranges of values of critical charge at the poly-

resistor nodes. The temperature variation yields an even smaller value of standard deviation, with the standard deviation being less than 1 at the 1-0 data transition.

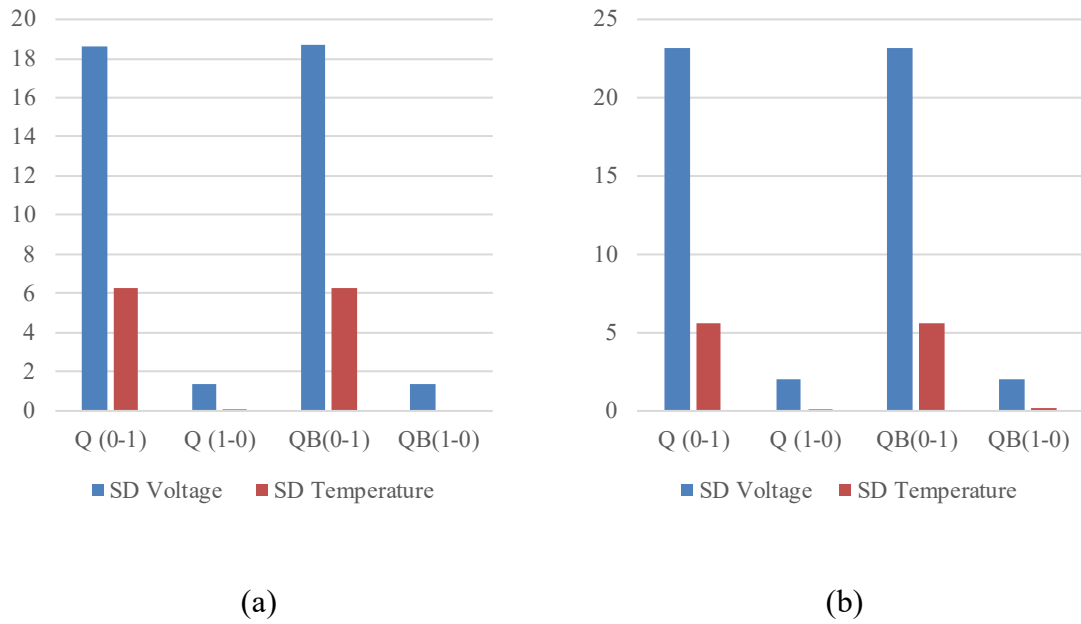


Figure 4.9: Standard deviation of critical charge for 4T SRAM for (a) read state and (b) hold state

4.3.2 6T SRAM

To assess the impact of the parameter variations on nodes Q and QB in different data states, we calculated the standard deviation of the critical charge, as depicted in Figure 4.10. In the context of this analysis, it's evident that the read state exhibits a lower standard deviation compared to the hold state, primarily due to the overall reduced critical charge. Notably, the voltage supply has a more pronounced influence on the critical charge, as evidenced in Figure 4.10 (a). Specifically, in the 0-1 data state, both read and hold states exhibit significantly higher deviations. This can be attributed to the fact that the NMOS holds the "0" state, which has a higher carrier mobility than the PMOS (Lin et al., 2010). In contrast, the temperature response has a comparatively minor impact on the critical charge for nodes Q and QB in the 0-1 and 1-0 data states. Furthermore, it's worth noting that the

read state necessitates the discharge of precharged bitlines as they access the inverters, making the SRAM cell inherently weaker in the read state as shown in Figure 4.10 (b) when compared to the hold state (Marques et al., 2020).

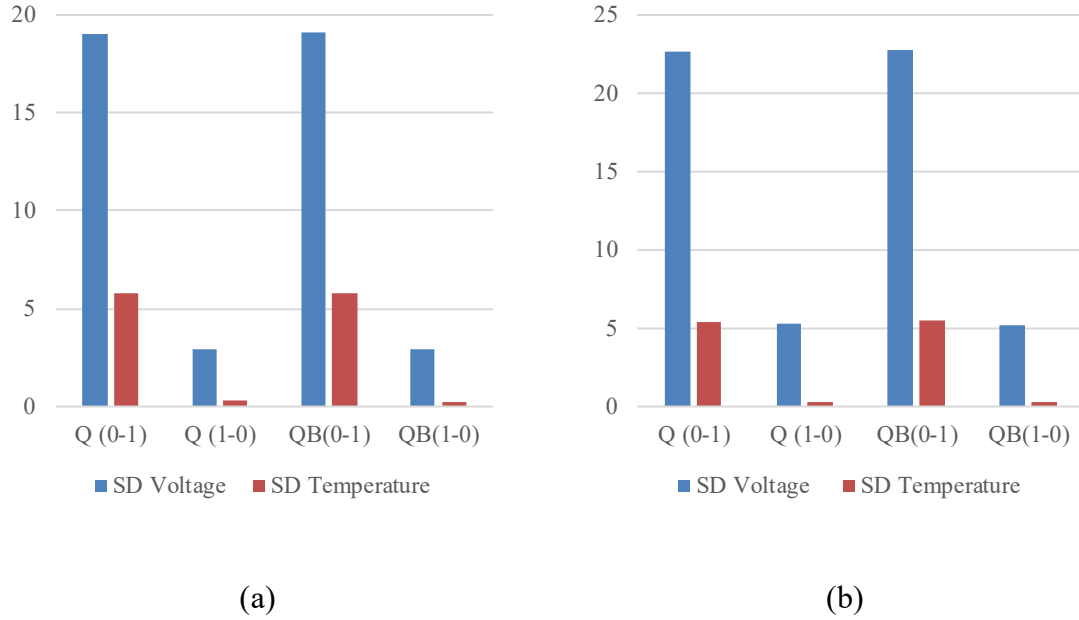


Figure 4.10: Standard deviation of critical charge for 6T SRAM for (a) read state and (b) hold state

4.3.3 9T SRAM

The standard deviation of the 9T SRAM was taken to observe the effect of the parameter variation on the critical charge. For the read state, the standard deviation of the 0-1 transition is much higher, indicating the wider ranges of critical charges obtained over the voltage ranges. As the 9T SRAM incorporates an isolated read node, the stability of the read state of the 9T SRAM is greater than during the hold state. The critical charge of the 9T SRAM scales very well with the downscaling of the voltage supply, with the critical charge of the 9T SRAM being the lowest out of the tested SRAMs. The standard deviation of the NMOS node, represented by Q and QB (0-1), is higher than that of the PMOS node, denoted by Q and QB (1-0). This is true for the temperature deviation as well. As the values of critical

charge for the NMOS node is higher, it is subject to a higher degree of deviation. Deviations to the PMOS node critical charge is less apparent as the critical charge of the node is very low.

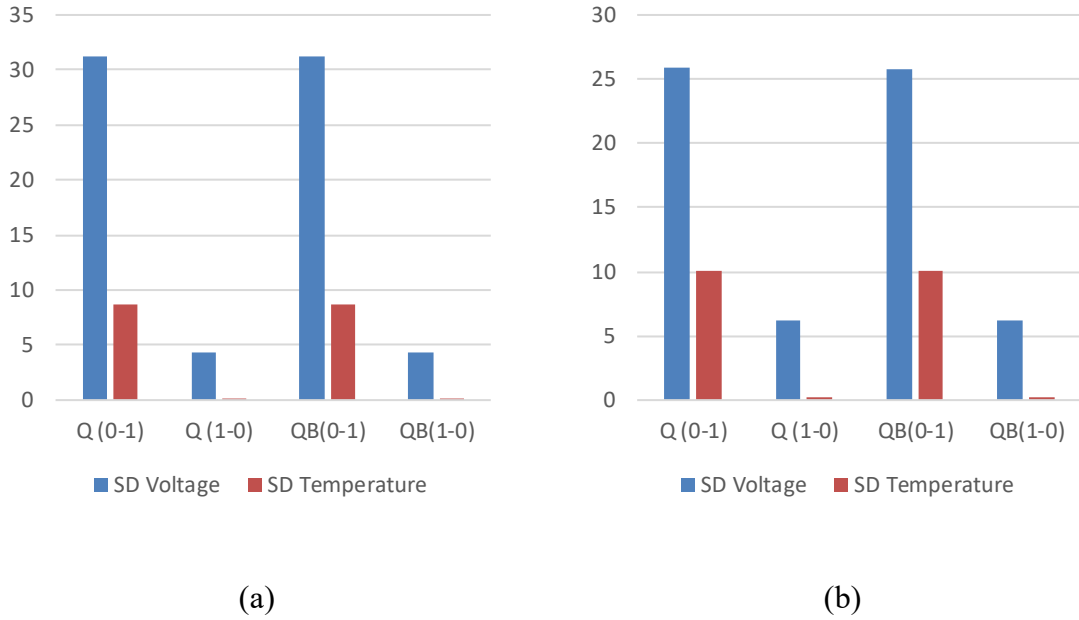


Figure 4.11: Standard deviation of critical charge for 9T SRAM for (a) read state and (b) hold state

4.3.4 SRAM with transmission gate filter

The standard deviation of the critical charge was calculated across various voltage and temperature ranges to assess their respective impacts on susceptibility to soft errors, specifically focusing on the transitions between data states 0-1 and 1-0 for each node. As depicted in Figure 8(a), the read state of the SRAM exhibits a lower standard deviation in critical charge, primarily because it is more sensitive to the risk of data being overwritten. Variations in voltage result in a broader range of critical charge values. Notably, for the state change from 0-1, nodes Q and QB display a higher standard deviation compared to the 1-0 transition. This disparity arises from the fact that the critical charge for the 1-0 transition is lower, attributed to the relatively higher carrier mobility of NMOS compared to PMOS (Lin

et al., 2009). Temperature fluctuations, while having a noticeable impact, exert a relatively smaller effect on the critical charge range for both nodes Q and QB. Overall, it can be observed that voltage supply variation exerts a more pronounced influence on critical charge than temperature does. In the hold state, similar trends are observed as in the read state, except for the increased critical charge across nodes Q and QB for both data states 0 and 1. This increase is due to the fact that the bit lines are not engaged during the hold state, reducing the cell's susceptibility to data corruption.

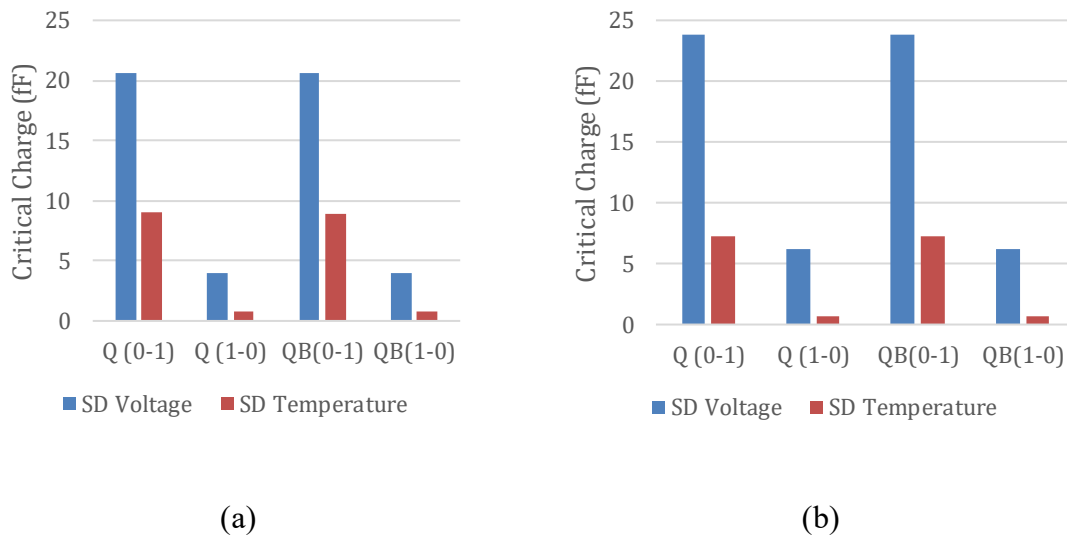


Figure 4.12: Standard deviation of critical charge for 9T SRAM for (a) read state and (b) hold state

4.3.5 Probability of data flip

a. 4T SRAM Read state

The probability of soft error over voltage is illustrated in the Figure 4.13. The resistor node, Q and QB (1-0) proves itself more vulnerable to error as the probability of an error occurring was found to be much higher than that of the NMOS, which is Q and QB (0-1). The probability for NMOS drain for both node Q and QB, which experiences the 0-1 data flip, decreases by 76.32% as the voltage supply is increased from 0.7V to 1.5V as the

required critical charge increases. The resistors holding the data state ‘1’ for node Q and QB on the other hand, sees a probability decrease of 15.27% as the voltage is increased due to the dependence of critical charge on the supply voltage. The critical charge is significantly affected by the level of operating voltage as observed in the increasing vulnerability of circuitry in the downscaling of dimensions and operating voltage (Soleimaninia et al., 2023). The high resistance of the resistors makes it vulnerable to soft errors and noise. A notable feature of Figure 4.13 is that the slope of probability decreases once the operating voltage is above 1.1V. This is due to the trip voltage of an SRAM increasing at a slower rate at the operating voltage of beyond 1V (Gopal et al., 2013).

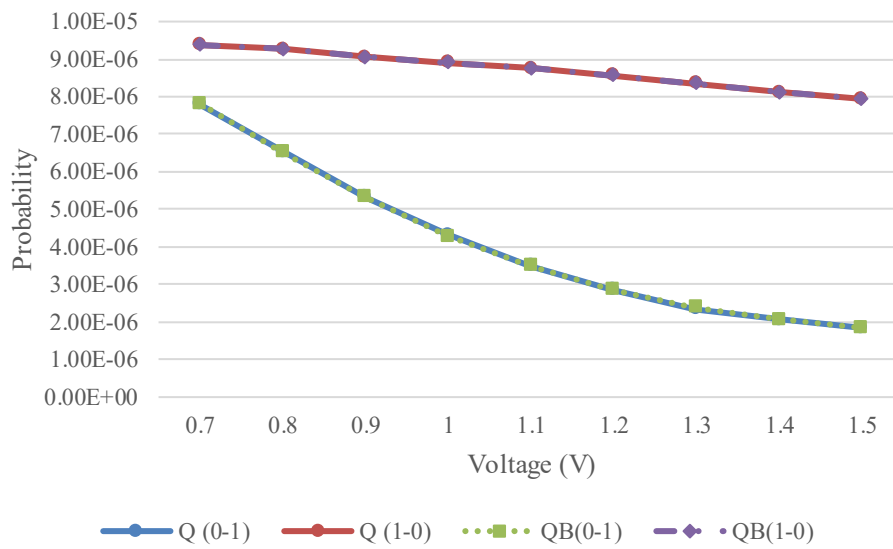


Figure 4.13: Probability vs voltage for 4T SRAM in read state

The effect of temperature on the probability soft error for the 4T SRAM in read state is as shown in Figure 4.14. As the temperature increases, the probability of the soft error increases due to the decrease in critical charge. Similar to the findings from the voltage variation, the resistor nodes have a higher probability of failure than that of the NMOS nodes.

The effect of temperature on the probability is not as severe as the variation of voltage. The nodes Q and QB for the NMOS drain which are Q (0-1) and QB (0-1) in the 4T SRAM sustain an increase in soft error probability of 62.21% as the temperature is increased from -50°C to 200°C. With reference to Figure 4.14 the resistor nodes which are Q and QB (1-0) of the 4T SRAM increase in probability by 0.114% as the temperature is increased from -50°C to 200°C. Increases in the temperature results in carrier mobility and threshold voltage degradation which in turn incites variation in transient current (Feeley et al., 2021). The collection charge of the device at higher voltages increases at a slower pace than the critical charge, resulting in a slower growth of the soft error probability at higher voltages (Narasimham et al., 2021).

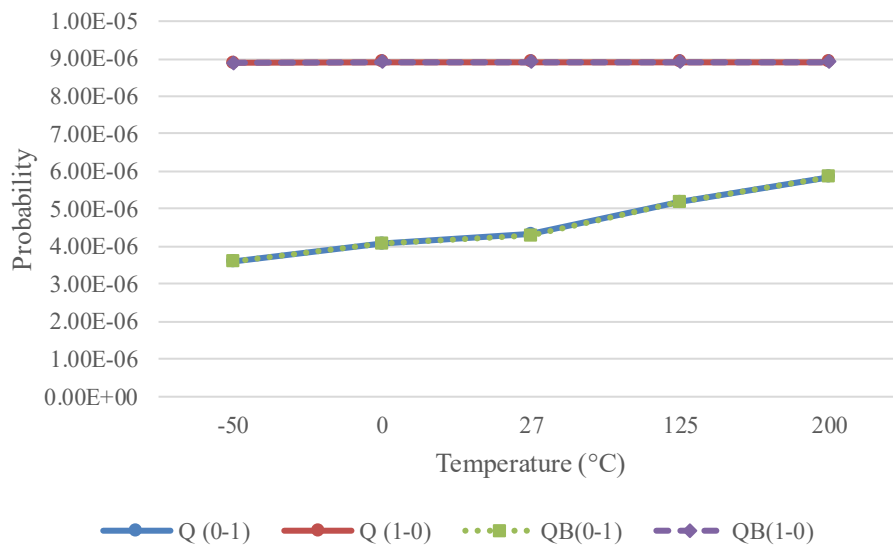


Figure 4.14: Probability vs temperature for 4T SRAM in read state

b. 4T SRAM Hold state

The probability of soft error with respect to voltage variation for the 4T SRAM in the hold state is as illustrated in the Figure 4.15. The soft error probability during the hold

state is higher than that of the read state due to the higher critical charge in this state. The probability of soft errors degrades as the voltage supply is increased. The resistor node, which is represented by Q and QB (1-0), has a much higher probability for soft error due to the high resistance of the resistors reducing the current in that node, allowing for transients to overwrite the data at the node.

The probability at nodes Q and QB for 1-0 have decreased by 22.23% as the supply voltage is increased from 0.7V to 1.5V. The probability of the drain of cross coupled NMOS transistors, Q and QB for 0-1, decreases by 83.4% as the supply voltage is increased from 0.7V to 1.5V.

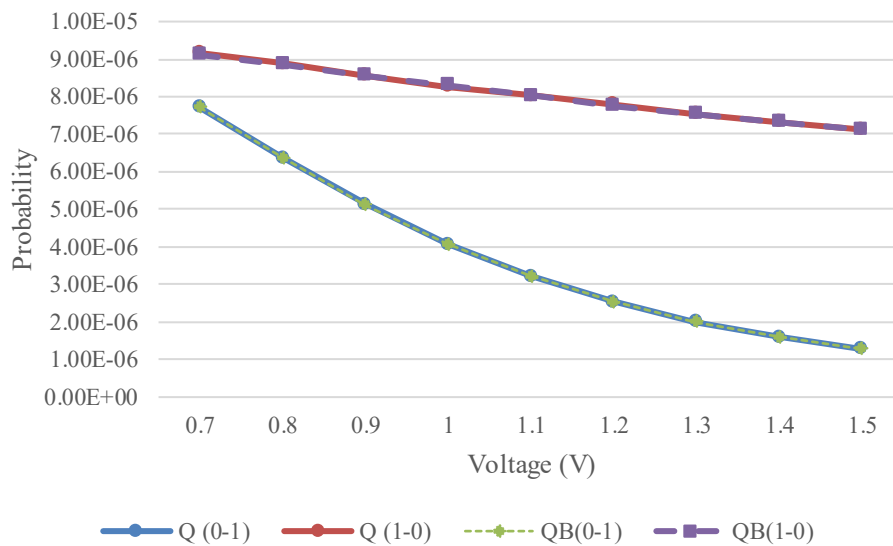


Figure 4.15: Probability vs voltage for 4T SRAM in hold state

The probability of soft error against temperature variation in 4T SRAM in the hold state is shown in the Figure 4.16. As the temperature is increased from -50°C to 200°C, the probability for the resistor node, Q and QB (1-0) increases by 1.15% as the temperature is increased from -50°C to 200°C. As for the drain of the NMOS in nodes Q and QB for 0-1,

the probability of soft error increased by 54.12% when the temperature is raised from -50°C to 200°C.

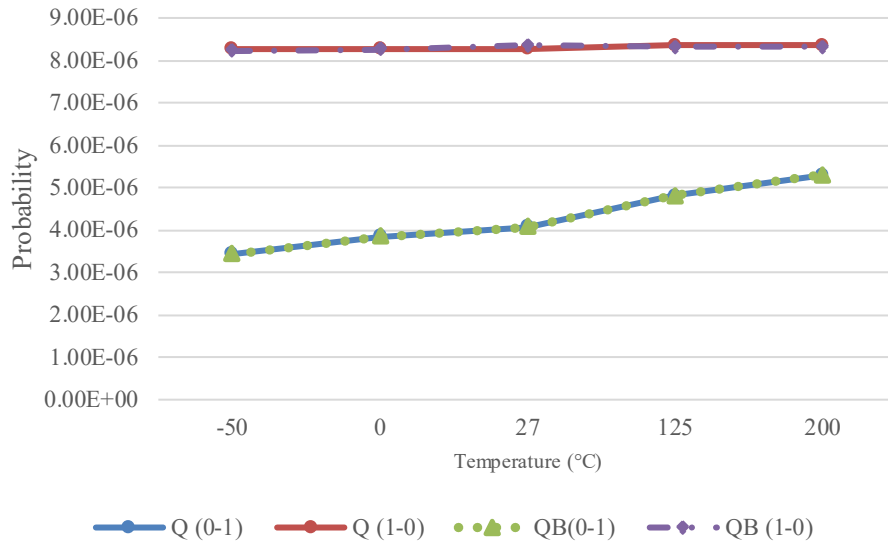


Figure 4.16: Probability vs temperature for 4T SRAM in hold state

c. 6T SRAM Read state

The probability against voltage for the 6T SRAM in read state is as illustrated as in Figure 4.17. As opposed to the 4T SRAM, the 6T SRAM has replaced the high impedance resistors in the 4T with two PMOS transistors. The PMOS transistors would be sized such that it would have the smallest widths in order to maintain the ease of writability of the SRAM cell, making the cell at its most vulnerable at the nodes holding the data state ‘1’. Also, unlike the 6T, the 4T SRAM lacks the restoring power of the interconnected PMOS and NMOS transistors of the 6T design, as well as having a relatively low nodal capacitance (Degalahal et al., 2003). Thus, 6T SRAMs present more soft error robustness compared to that of the 4T SRAM. The probability of soft errors for the PMOS for node Q and QB at 1-

0 decreased by 30.26% as the voltage is amplified from 0.7V to 1.5V. The soft error probability for the NMOS drain is represented by the nodes Q and QB (0-1) and decreases by 77.07% as the voltage rises from 0.7V to 1.5V. The cell at (0-1) sees a higher probability of soft error than (1-0) due to the larger area of the NMOS transistor that can be impacted by particle strikes. The NMOS drain begins to have a higher soft error probability when the voltage level is downscaled below the point 1.4V. The rate of increase of probability slows as the supply voltage reaches higher levels due to the unequal rate of growth for collection charge and critical charge. The critical charge increases at a higher rate than the collection charge at higher supply voltages, therefore the probability of the soft error occurring decreases as the critical charge exceeds the collection charge (Narasimham et al., 2021).

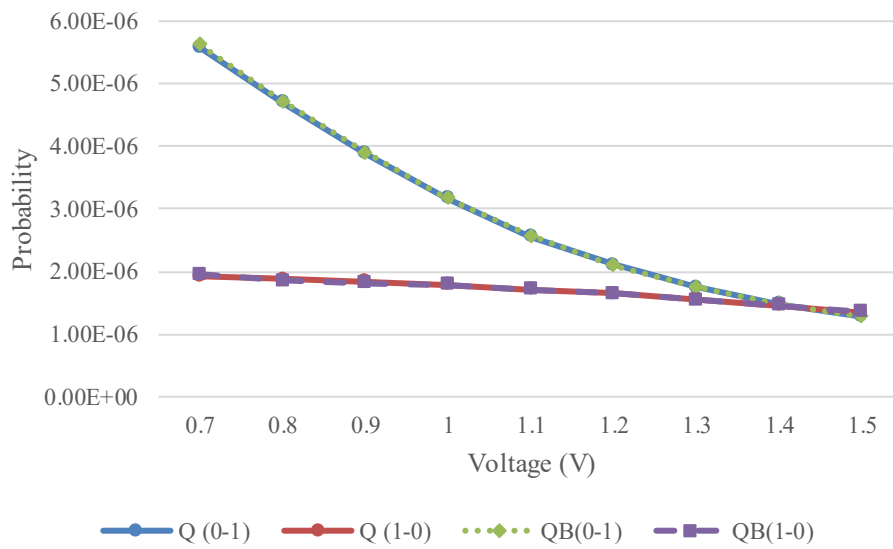


Figure 4.17: Probability vs voltage for 6T SRAM in read state

Figure 4.18 illustrates how this probability of soft error changes with variations temperature. Because the SRAM cell has a symmetrical layout, the probability is the same for nodes Q and QB when the data states are "0" and "1". The probability of the data states

flipping switch between data states of 0-1 and 1-0 for nodes Q and QB varies within the temperature range of -50 °C to 200 °C. An increase in temperature reduces carrier mobility, although not as significantly as voltage supply variation (Fishchuk et al., 2010). Figure 4.17, the critical charge for transitioning from 1-0 is lower than that for 0-1. As temperature rises, for Q and QB the probability increases by 55.99% for 0-1 and 3.52% for 1-0.

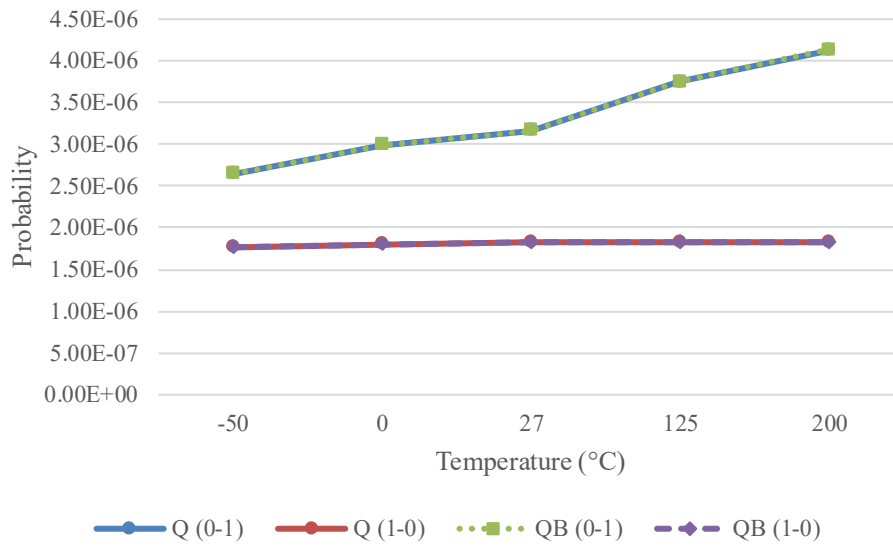


Figure 4.18: Probability vs temperature for 6T SRAM in read state

d. 6T SRAM Hold state

Figure 4.19 shows the probability of soft error response to the variation of supply voltage for the 6T SRAM in hold state, when the bitlines are unengaged. As the voltage was varied from 0.7V to 1.5V, the drain of the NMOS, represented by Q and QB (0-1), sees a decrease in soft error probability of 82.72%. The probability of soft error at the PMOS drain, denoted by the Q and QB (1-0), sees a decrease of 47.87%. The probability of the PMOS drain is distinctly higher than that of the NMOS due to the relatively smaller sizing, a design decision that is taken to form a weak pull-up, which allows for easier writing of data state

‘1’ into the cell. Consequently, the cell is vulnerable to noise and errors when the node holds a data state ‘1’. The probability of the soft error converges when the supply voltage is at 1.5V due to the fact that size of the NMOS also plays a factor in soft error susceptibility, presenting a larger area for particle strikes. When the voltage is downscaled, however, the NMOS transistor proves to be much more resilient in resisting soft errors.

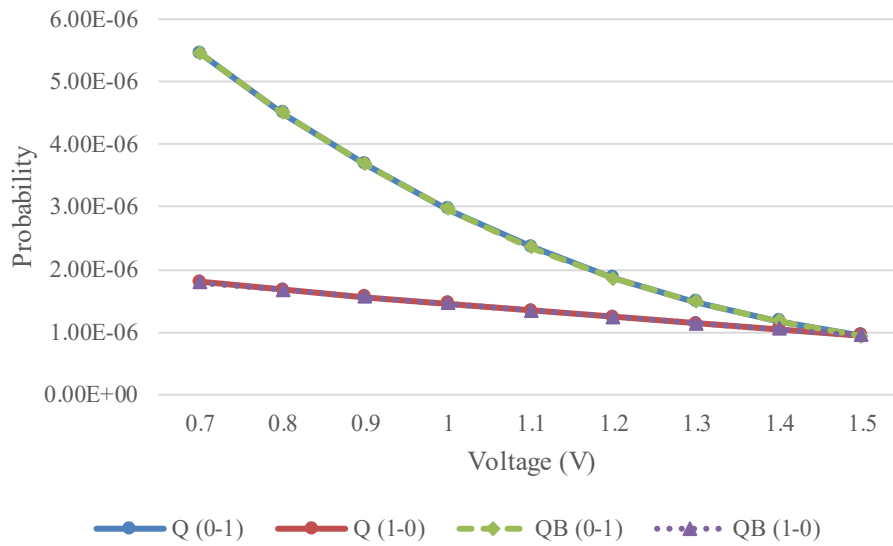


Figure 4.19: Probability vs voltage for 6T SRAM in hold state

Figure 4.20 shows the effect of temperature on the soft error probability of the 6T SRAM in the hold state, when the bitlines are unengaged from the cell. The NMOS drain, represented by Q and QB (0-1), sees a soft error probability increase of 52.27% as the temperature is raised from -50 °C to 200 °C. The PMOS drain on the other hand, sees an increase of 3.51% over the range of specified temperatures. The NMOS drain in the hold state has a slightly higher amount of resilience than in the read state, due to the smaller noise margins inherent in SRAMs in their read state (Marques et al., 2021).

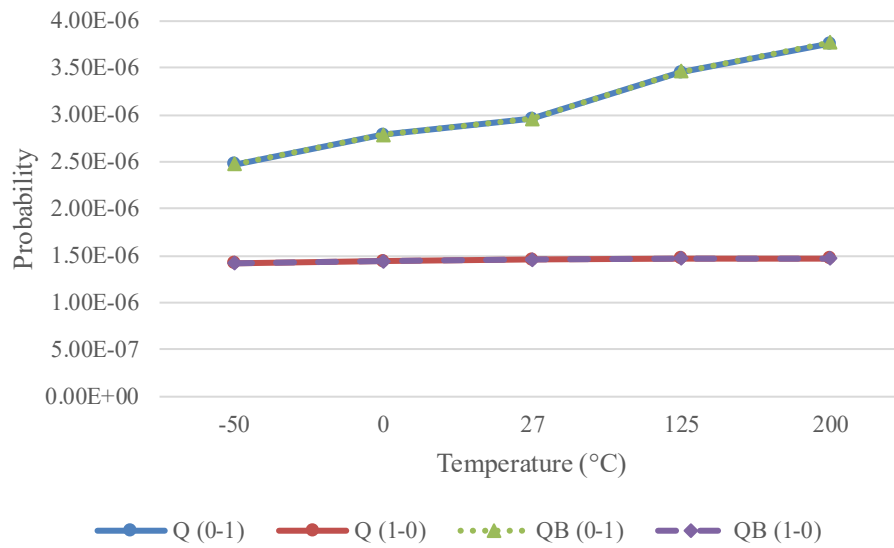


Figure 4.20: Probability vs temperature for 6T SRAM in hold state

e. 9T SRAM Read state

Figure 4.21 shows the probability of soft error against the variation of supply voltage for the 9T SRAM in the read state. The NMOS drain, represented by Q and QB (0-1) is lower in soft error probability to the PMOS drain, which is represented by the Q and QB (1-0) at voltage level 1.5V, but when the voltage level is reduced to below 1.1V, the NMOS drain weakens in its resilience when the larger area of the node that is vulnerable to particle strikes is taken into account. The soft error probability for the NMOS drain in the inverter loop, denoted by Q and QB (0-1) reduces by 91.09% as the voltage is increased from 0.7V to 1.5V. The soft error probability of the PMOS drain in the 9T SRAM inverter loop lowers by 41.89% over the range of voltage supply variation. The NMOS drain is more robust than the PMOS drain from 1.1V and below, displaying a higher resilience to downscaling in voltage supply compared to the PMOS drain.

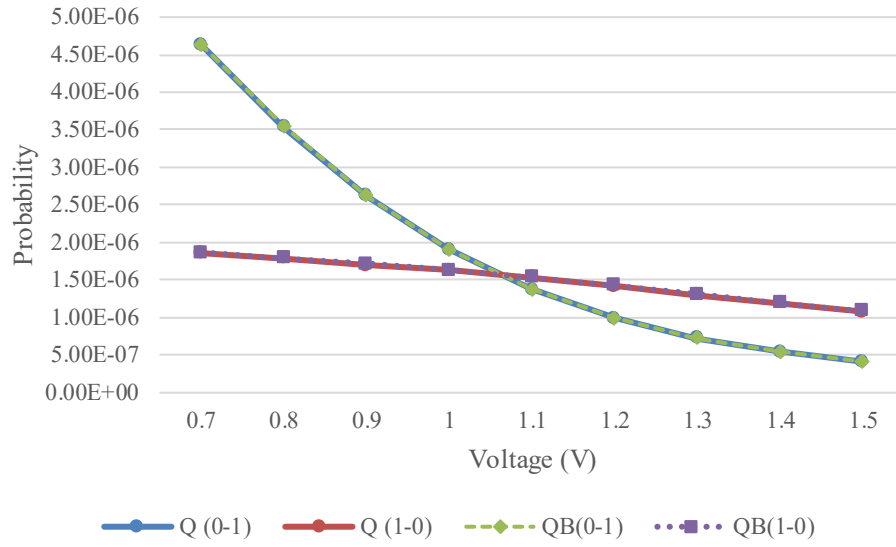


Figure 4.21: Probability vs voltage for 9T SRAM in read state

The probability of soft error response to temperature variation for the 9T SRAM in read state is illustrated in Figure 4.22. The increasing temperature results in a deterioration of threshold voltage, carrier mobility and saturation velocity (Douadi et al., 2023). The soft error probability of the NMOS drain, represented by Q and QB (0-1) increases by 95.19% as the temperature is manipulated from -50 °C to 200 °C. The PMOS drain, on the other hand, denoted by Q and QB (1-0), sees a probability increase of 1.5%. The probability of the soft error at the NMOS drain is greater than that of the PMOS drain as the temperature increases from 0 °C to 200 °C. The larger area of the NMOS drain provides a larger area that can become potential impact zones for single event upset inducing particle strikes.

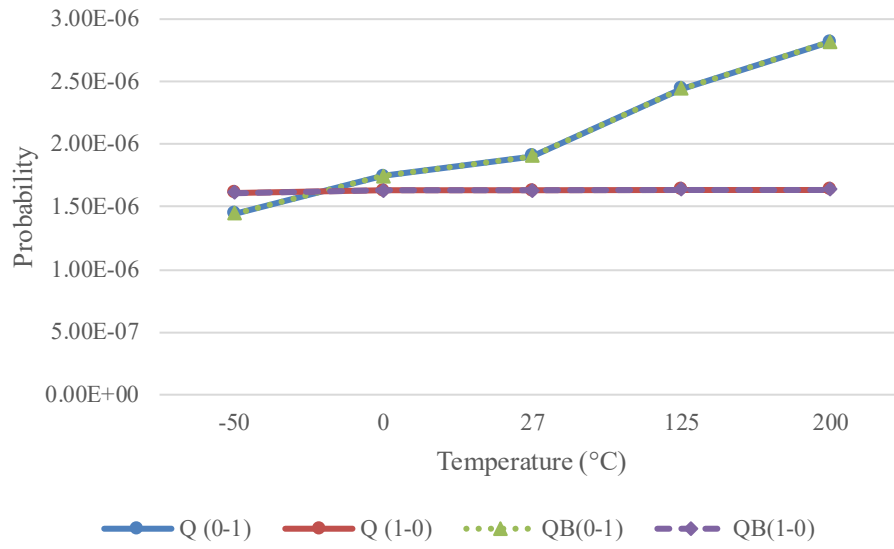


Figure 4.22: Probability vs temperature for 9T SRAM in read state

f. 9T SRAM Hold state

The soft error probability against supply voltage variation for 9T SRAM in hold state is illustrated in Figure 4.23. The probability of the soft errors is lower in the hold state due to the unengaged bitlines, allowing the cell to hold the data in latch. Therefore, the hold state is more stable and resistant to noise and soft error than that of the read state (Gadhe & Shirode, 2013). The NMOS probability is greater than the PMOS when the voltage is reduced below 1.4V. The soft error probability for the NMOS drain, denoted by Q and Q (0-1), decreases by 86.46% as the voltage supply is increased from 0.7V to 1.5V. The PMOS drain, denoted by Q and QB (1-0), decreased by 53.88% as the voltage supply is varied by the same amount.

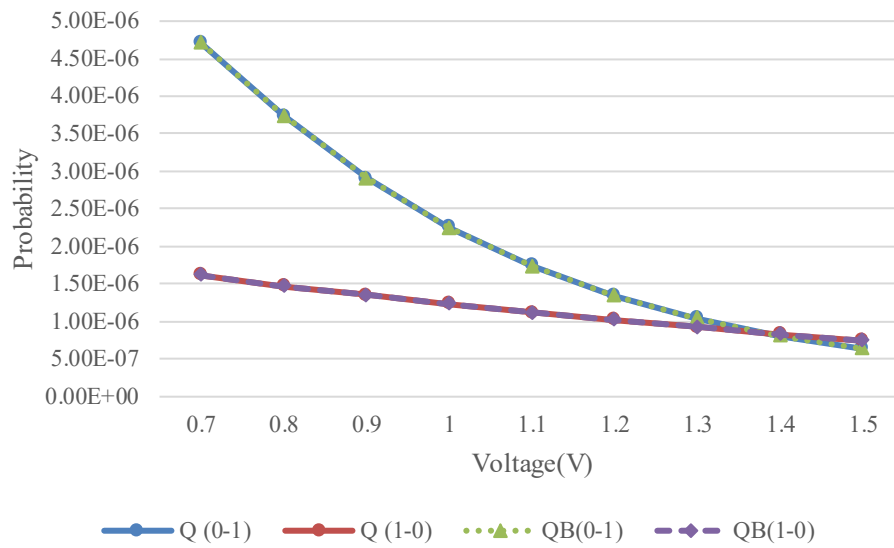


Figure 4.23: Probability vs voltage for 9T SRAM in hold state

The probability of soft error for the 9T SRAM during hold state against temperature variation is shown in Figure 4.24. The NMOS drain, denoted by Q and QB (0-1) has greater soft error probability than the PMOS drain, denoted by Q and QB (1-0), due to the greater susceptible area of potential particle strikes. The NMOS drain increases in soft error probability by 118.39%, while the PMOS drain increases by 2.89% as the temperature is increased from -50 °C to 200 °C.

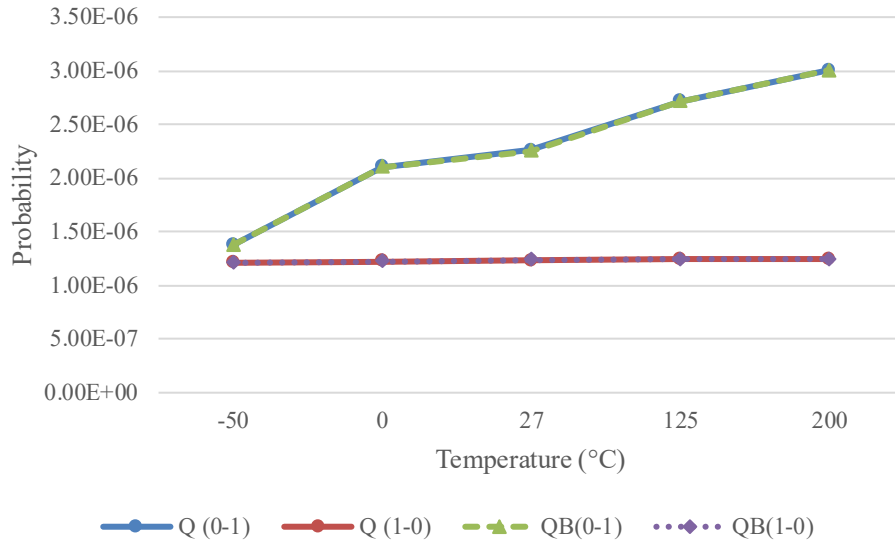


Figure 4.24: Probability vs temperature for 9T SRAM in hold state

g. SRAM with transmission gate transient filter read state

The probability of the soft error for the SRAM with transmission gate transient filter in read state is as shown in Figure 4.25. The design of the transient filter is based on a proposed transmission gate filter (Sayil et al., 2017). The NMOS drain of the inverter loop of the SRAM cell is represented by Q and QB (0-1). The transmission gate transient filter is attached to the Q and QB nodes of the 6T SRAM, allowing it to filter the transient current generated from single event upsets. The gate voltages of the transmission gate filter is controlled at 0.7V and 0.5V to take advantage of the strong filtering effect resulting from the reduced gate-source voltage for the NMOS pass transistor and the reduced source-gate voltage for the PMOS transistor.

The probability of soft error for the NMOS drain of the inverter loop, denoted by Q and QB (0-1), decreased by 79.68% as the supply voltage is increased from 0.7V to 1.5V.

The probability for the PMOS drain, denoted Q and QB (1-0) followed a similar trend, decreasing by 39.17% over the same voltage range.

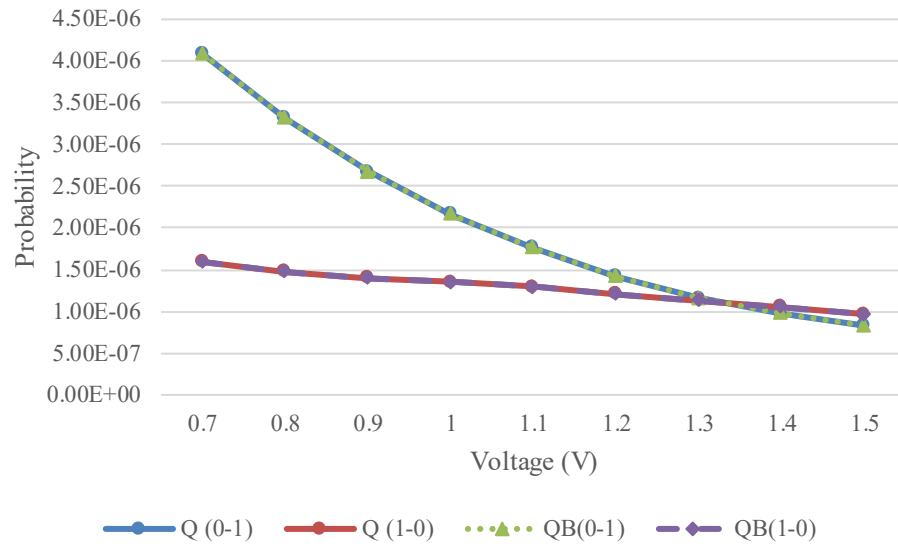


Figure 4.25: Probability vs voltage for SRAM with transmission gate transient filter in read state

The probability of soft error response to temperature variation for SRAM with transmission gate filter in read state is shown in Figure 4.26. The temperature is increased from -50 °C to 200 °C, causing an increase in soft error probability due to the decrease in critical charge as the temperature rises (Feeley et al., 2021). The NMOS drain, represented by the Q and QB (0-1) nodes, sees a soft error probability increase of 100.96% as the temperature is increased from -50 °C to 200 °C. The PMOS drain, represented by Q and QB (1-0) increased in soft error probability by 11.15% as the temperature is increased from -50 °C to 200 °C.

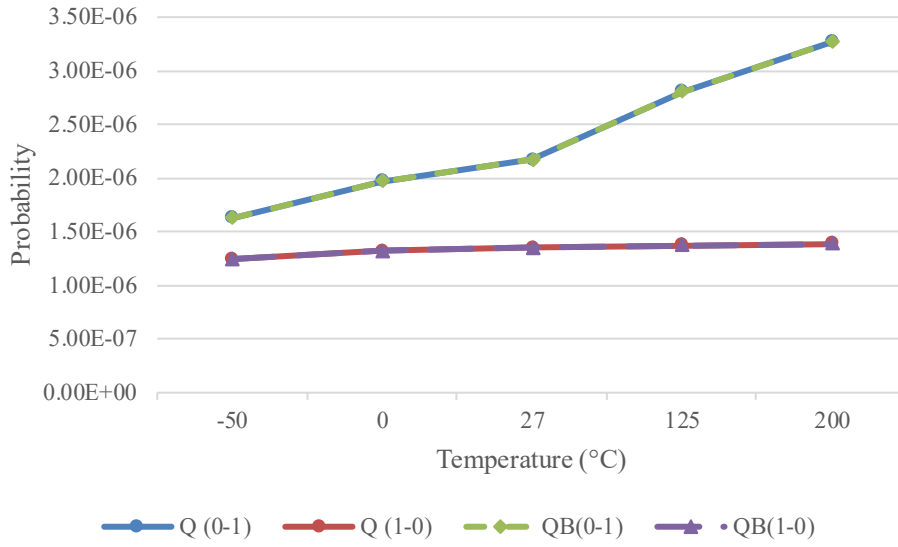


Figure 4.26: Probability vs temperature for SRAM with transmission gate transient filter in read state

h. SRAM with transmission gate transient filter hold state

Figure 4.27 shows the soft error probability response to voltage variation for SRAM with transmission gate filter in the hold state. The probability of the hold state is lower than that of the read state due to the higher noise margin and stability (Apollos, 2019). The probability of soft error for the NMOS drain represented by Q and QB (0-1), decreased by 84.1% as the supply voltage is increased from 0.7V to 1.5V. The probability for the PMOS drain, denoted Q and QB (1-0) followed a similar trend, decreasing by 54.03% over the same voltage range. The NMOS probability varies on a much greater magnitude than the PMOS, due to the higher variation of critical charge as the sizing of the NMOS is larger than the PMOS, thus resulting in a cell that has a stronger pull down strength .

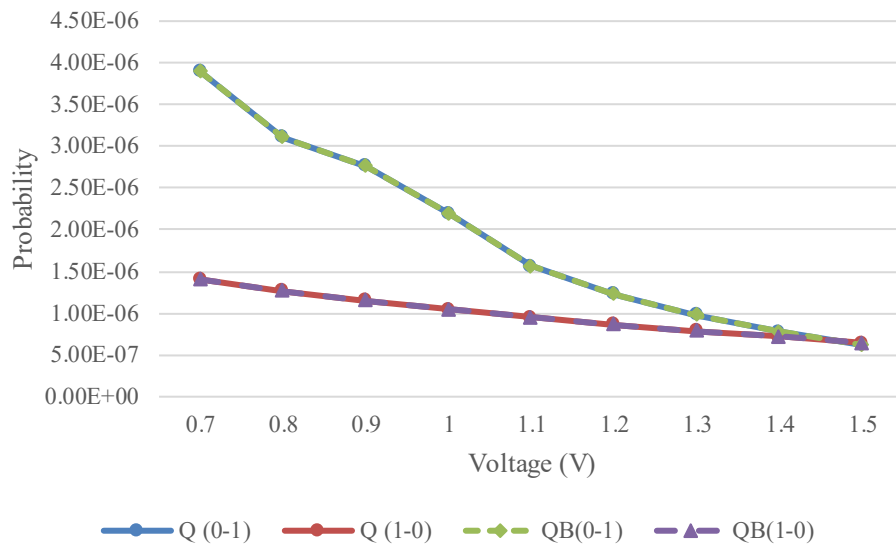


Figure 4.27: Probability vs voltage for SRAM with transmission gate transient filter in hold state

The response of soft error probability to the variation of temperature for the SRAM with transmission gate transient filter in hold state is as shown in Figure 4.28. The NMOS drain, represented by the Q and QB (0-1) nodes, sees a soft error probability increase of 75.68% as the temperature is increased from -50 °C to 200 °C. The PMOS drain, represented by Q and QB (1-0) increased in soft error probability by 9.2% as the temperature is increased from -50 °C to 200 °C. The PMOS drain sees a lower increase in probability in comparison to that of NMOS drain. As the sizing of the PMOS transistor in the feedback loop is smaller than the NMOS transistor the drain current is consequently lower, as well as the critical charge. As such, the temperature variation has a smaller visible effect on the soft error probability.

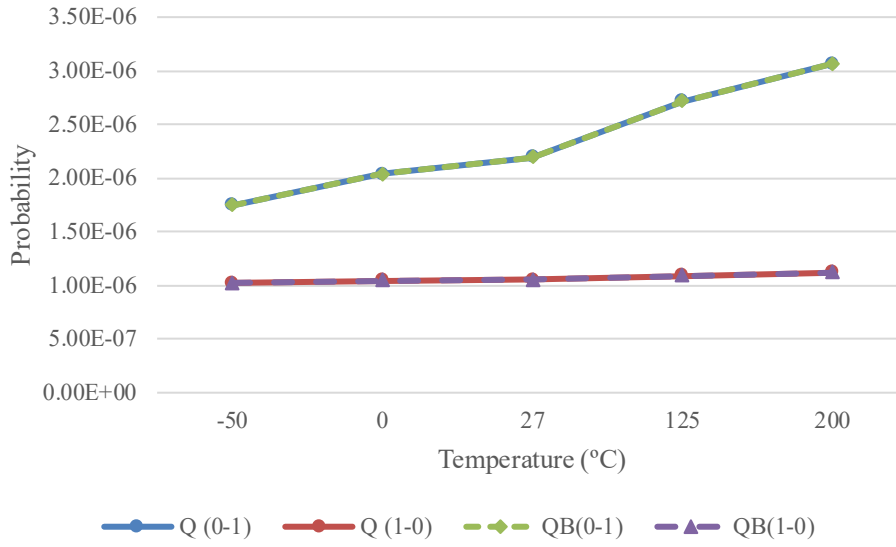


Figure 4.28: Probability vs temperature for SRAM with transmission gate transient filter in hold state

4.3.6 Performance comparison

i. Probability vs voltage for SRAMs in read state for NMOS drain (0-1)

Figure 4.29 shows the soft error probability response of the 4T, 6T, 9T, and transmission gate SRAMs to the variation of voltage supply for the NMOS drain, Q and QB (0-1). The 4T SRAM is displayed as being the least resilient to soft error, as the probability soft error is highest among the tested SRAM cells. The reasoning for this can be explained through the presence of a lower ratio of sensitive transistor area to total transistor area. As the 4T SRAM only holds two NMOS transistors for the pull down transistors and is lacking in pull up transistors, with polyresistors taking its place instead (Bhuvaneshwari et al., 2015). At voltages lower than 1V, the weakness of the 4T SRAM becomes especially apparent, with the gradient becoming much steeper, thus displaying a more dramatic trend in the rise of probability in data change as the critical charge increases.

a. 4T and 6T performance comparison under voltage variation

The 6T SRAM proves to be more resilient than the 4T, providing a lower probability across the voltage variations which is 28.4% less than the 4T at 0.7V and 30.7% at 1.5V. This is due to the increased ratio of sensitive node area over total node area. As compared to the 4T SRAMs, the pull up transistors not only provide a higher pull up strength, but also greatly increase the ratio of sensitive node area to total node area in the SRAM. The presence of the pull up transistors thus contributes to a lower error probability as compared to the 4T SRAM throughout the voltage supply levels. As with the 4T SRAM, however, the error probability increases at lower voltage supply, though at a visibly lower rate. This observation can be explained by the fact that at the nanometric scale SRAMs have much lower critical charges, therefore becoming more susceptible to soft errors (Soleimaninia et al., 2023).

b. 6T and 9T performance comparison under voltage variation

The 9T SRAM displays its robustness through its low probability throughout the increments of voltage variations, achieving a soft error probability of 16.9% at 0.7V and 15.5% at 1.5V less than the 6T SRAM. A major reason for this is the fact that the 9T SRAM possesses a higher pull down strength due to the dedicated read bit line, allowing the inverter loop to become stable when the memory node is holding a logic value 1. The probability decreases as the voltage supply increases, as the progression of this trend also brings about the increase of the critical charge, thus making it more difficult for the logic level to flip due to a transient current (Sachdeva & Tomar, 2022).

c. 9T and transmission gate transient filter performance comparison under voltage variation

The SRAM with transmission gate transient filter manages to outperform the 9T SRAM during the lower supply voltage levels, however, with it presenting the lowest soft error probability at the voltage level 0.7V and 0.8V. The 9T SRAM is known to underperform at lower voltage supply levels due to the dependence of critical charge on supply voltage which clarifies the increased error probability at voltage levels 0.9V and lower (Artola et al., 2014). The transmission gate transient filter SRAM provides a lower probability of 11.19% at 0.7V than the 9T SRAM. However, the probability of the transmission gate transient filter SRAM has a higher probability of 50.3% at 1.5V compared to the 9T SRAM. The transmission gate transient filter boasts a higher comparative critical charge at lower voltage supply levels relative to the other SRAM architectures, outperforming the 9T SRAM at voltage supply levels lower than 1V. The transient filter attenuates the transient current produced by the single event upset. The transient filter also presents an increased resistance between the memory nodes, which reduces the paths for leakage currents, resulting in a lower critical charge and error probability (Carbognani et al., 2008).

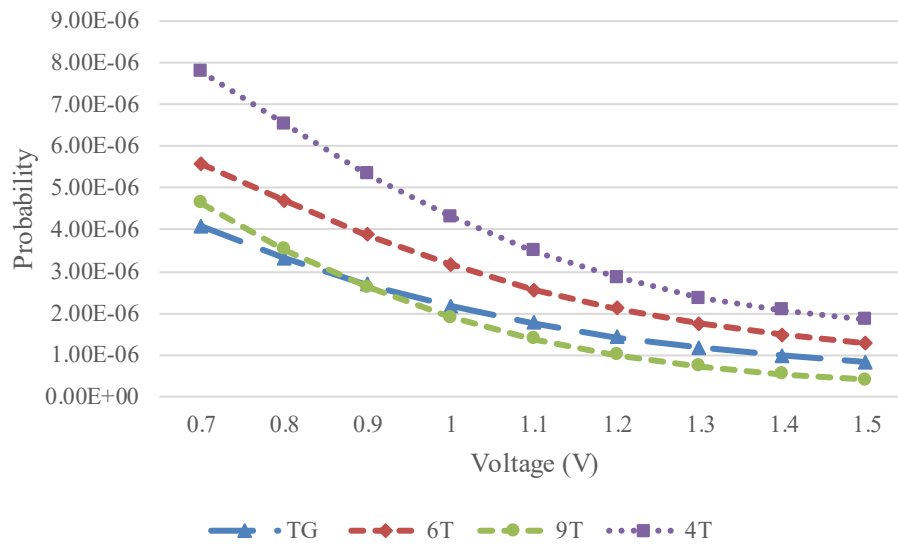


Figure 4.29: Probability vs voltage for SRAMs in read state for NMOS drain (0-1)

- ii. Probability vs voltage for SRAMs in read state for PMOS drain (1-0)
- a. 4T and 6T performance comparison under voltage variation

Figure 4.30 shows the probability of the 4T, 6T, 9T, and transmission gate SRAMs to the variation of voltage supply for the PMOS drain, which is represented by Q and QB (0-1). The least resilience to soft error is shown to be the 4T SRAM, with the highest soft error probability of the SRAM cells, exacerbated by the use of high impedance polyresistors in place of the PMOS transistors employed in the 6T, 9T and transmission gate filter SRAMs. Following that, the 6T SRAM presents a lower probability than that of the 4T SRAM by 79.5%,

- b. 6T and 9T performance comparison under voltage variation

With reference to the slopes of the 6T and the 9T SRAM in Figure 4.30, the performance shows a similar trend due to the pull up strength being similar as the 9T SRAM is only reinforced on its pull down strength, with 6T SRAM higher in probability than the 9T SRAM by 3.4% when the voltage supply is downscaled to 0.7V. The 9T SRAM however, still provides an improved performance due to the higher critical charge inherent to the design due to the higher cell read stability as compared to the 6T SRAM (Chandra, 2021).

c. 6T and transmission gate transient filter performance comparison under voltage variation

The SRAM with transmission gate transient filter provides the highest level of protection from soft error, with a lower soft error probability than the 9T SRAM by 16.7%. A notable difference between the transmission gate transient filter and the 9T SRAM is that the latter provides protection against transient currents, while the 9T SRAM does not provide any additional protection for the pull up transistors over the 6T SRAM. Therefore, the transient filter SRAM is capable of achieving the lowest error probability out of the selection of SRAM architectures. The probability of each of the SRAM cells is lower than those achieved from the NMOS drain due to the sizing of the PMOS in the SRAM, making it more vulnerable to soft errors. The probability of a soft error happening decreases as the supply voltage rises to higher levels because the growth rate of critical charge surpasses that of collection charge. At elevated supply voltages, the critical charge increases more rapidly than the collection charge, resulting in a slowdown in the probability's rate of increase (Narasimham et al., 2021).

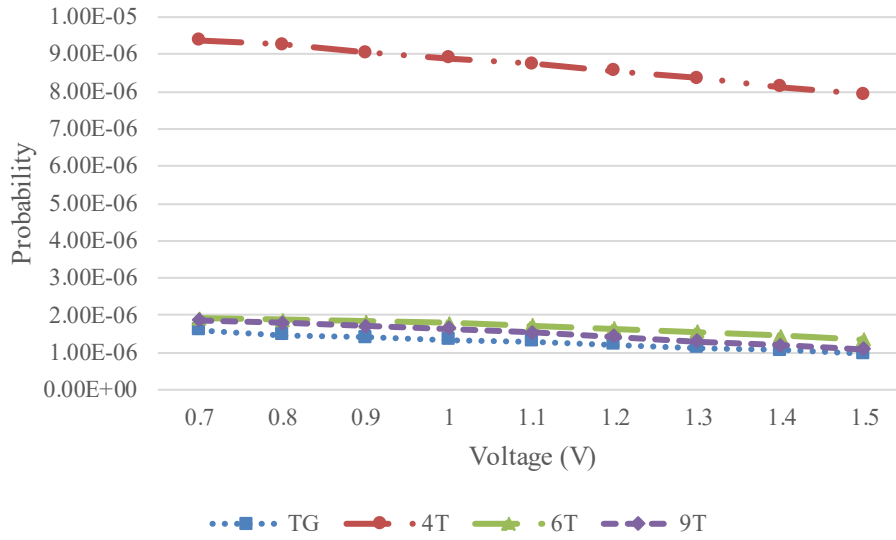


Figure 4.30: Probability vs voltage for SRAMs in read state for PMOS drain (1-0)

iii. Probability vs temperature for SRAMs in read state for NMOS drain (0-1)

a. 4T and 6T performance comparison under temperature variation

Figure 4.31 shows the response of soft error probability to temperature variation in read state for 4T, 6T, 9T, and transmission gate SRAMs for the NMOS drain, which is represented by Q and QB for (0-1). The 4T SRAM is shown to be least resilient to soft error through its poor showing in regards to its high probability of soft error. The probability of the 4T SRAM is higher by 26.61% and 29.42% than the probability of the 6T SRAM at -50 °C and 200 °C respectively. The temperature variation shows a trend that suggest a higher probability of soft errors at higher temperatures, consistent with the increased sensitive of transients with temperature (Ferlet-Cavrois et al., 2013).

b. 6T and 9T performance comparison under temperature variation

The 9T SRAM does perform much better than the previous 6T and 4T SRAMs, however, performing better than the 6T SRAM by 45.4% and 31.7% at the temperature of -

50 °C and 200 °C respectively. This is due to the data isolation from the bitlines during a read operation increasing the robustness of the data against noise (Gavaskar & Priya, 2013).

c. 9T and transmission gate transient filter performance comparison under temperature variation

The transmission gate transient filter SRAM has an improved resistance against soft errors in comparison to the 6T and 4T SRAM but is unable to match that of the 9T SRAM. At -50 °C and 200 °C, the 9T SRAM has an improved probability of 12.62% and 15.95% over the transmission gate transient filter respectively. However, it should be noted that the design of the 9T SRAM has a focus on strengthening the pull-down force of the cell while the transmission gate transient filter seeks to provide more coverage in its soft error mitigation, protecting against 0 and 1 flips (Zhiyu & Kursun, 2008).

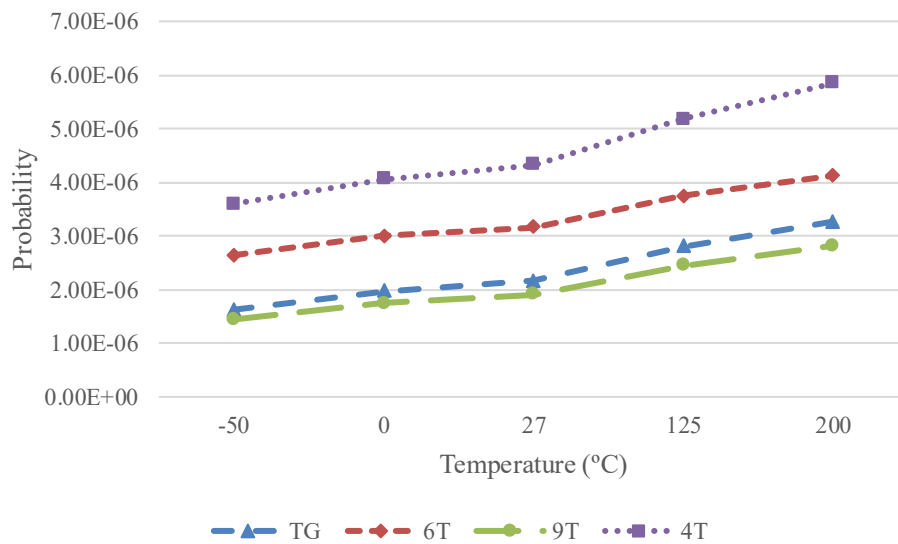


Figure 4.31: Probability vs temperature for SRAMs in read state for NMOS drain (0-1)

- iv. Probability vs temperature for SRAMs in read state for PMOS drain (1-0)
- a. 4T and 6T performance comparison under temperature variation

Figure 4.32 shows the soft error probability response to temperature variation in the read state for the 4T, 6T, 9T, and transmission gate SRAMs for the PMOS drain, which is represented by Q and QB for (1-0). The SRAM cells showed an overall higher probability of soft error due to the lower critical charge of the node when holding a data state '1', as the PMOS transistors are engaged. The 4T SRAM had the highest probability of soft error as the critical charge of the polyresistors are much lower compared to the 6T, 9T and the transmission gate transient filter SRAMs that have PMOS transistors in the inverter loop (Keren et al., 2019). The 6T SRAM has an improvement of 80.15% and 79.48% compared to the 4T SRAM in soft error probability at the temperatures of -50 °C and 200 °C respectively.

- b. 6T and 9T performance comparison under temperature variation

The 9T SRAM soft error probability is improved by about 8.71% and 10.5% compared to the 6T SRAM at temperatures of -50 °C and 200 °C respectively. The 9T SRAM is able to achieve this due to the higher read stability owing to the node isolation that occurs during read operation, an advantage that it has over the 6T SRAM (Zhiyu & Kursun, 2008).

- c. 9T and transmission gate transient filter performance comparison under temperature variation

The transmission gate transient filter on the other hand, also sees an improvement on soft error probability of 22.71% and 22.37% at temperature points of -50 °C and 200 °C respectively compared to 9T SRAM. The lower error probability is a more pronounced issue in the 9T SRAM as the transient pulse width is worsened with the increase of operating

temperature especially when it is unattenuated (Singh et al., 2013). The transmission gate transient filter can achieve lower probability values as the transient current is attenuated through the memory nodes, increasing the critical charge and subsequently reducing the error probability.

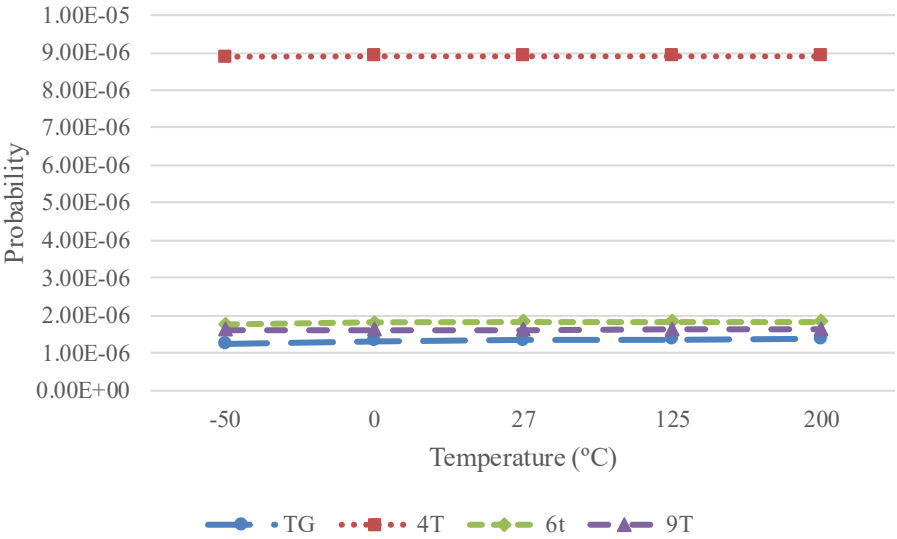


Figure 4.32: Probability vs temperature for SRAMs in read state for PMOS drain (1-0)

- v. Probability vs voltage for SRAMs in hold state for NMOS drain (0-1)
- a. 4T and 6T performance comparison under voltage variation

Figure 4.33 shows the soft error probability response to voltage variation in the hold state for the 4T, 6T, 9T, and transmission gate SRAMs for the NMOS drain, which is represented by Q and QB for (0-1). The soft error probability of the SRAM cells have a lower soft error probability in the hold state rather than in the read state due to the reduced stability during the read state (Apollos, 2019). The 4T SRAM is once again the SRAM cell with the highest probability of soft error amongst the tested SRAM configurations. The 6T SRAM provides a much better performance in soft error probability, presenting a lower

probability of 29.7% and 26.29% at 0.7V and 1.5V respectively in comparison to the 4T. In this case, the read stability of the 4T SRAM is much weaker than that of the 6T SRAM, thus leading to an ultimately lower critical charge and subsequent performance even with a smaller area for particle strikes (Fan et al., 2011).

b. 6T and 9T performance comparison under voltage variation

The 9T SRAM proves more robust than the previous two SRAM configurations, having a soft error probability 13.75% lesser at 0.7V and 32.43% lesser at 1.5V when compared to the 6T SRAM. The 9T SRAM has an increased read stability due to node isolation which allows it to maintain a low probability even with an increased sensitive node area (Athe & Dasgupta, 2009).

c. 9T and transmission gate transient filter performance comparison under voltage variation

The SRAM with transmission gate transient filter also manages to improve upon the performance of the 9T SRAM, with a soft error probability improvement of 17.3% at 0.7V and 2.88% at 1.5V. The 9T SRAM has a design that is focused on the improvement of read stability with the use of node isolation and stronger pulldown strength, with little regard for the node stability during hold state operation (Marques et al., 2020). The transient filter, on the other hand presents a higher critical charge for both read and hold operations, without increasing sensitive node area, allowing for a lower error possibility.

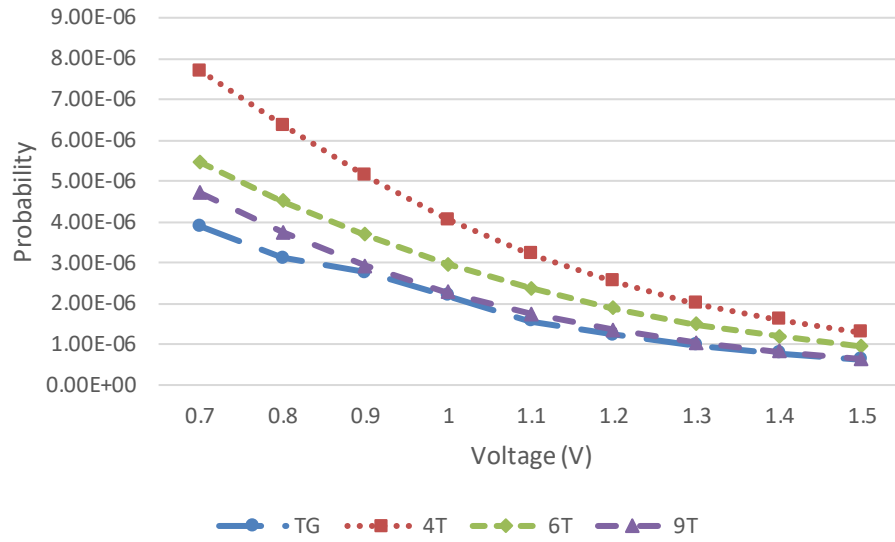


Figure 4.33: Probability vs voltage for SRAMs in hold state for NMOS drain (0-1)

- vi. Probability vs voltage for SRAMs in hold state for PMOS drain (1-0)
- a. 4T and 6T performance comparison under voltage variation

Figure 4.34 shows the soft error probability response to voltage variation in the hold state for the 4T, 6T, 9T, and transmission gate SRAMs for the PMOS drain, which is represented by Q and QB for (1-0). The 4T SRAM hold the data state '1' in the polysresistors in its configuration, resulting in it underperforming in regard to soft error probability amongst the SRAM cells (Zhu & Ohsawa, 2022). The 6T SRAM has a significant increase in resilience, holding a soft error probability that is 80.28% and 86.78% lesser than the 4T SRAM at 0.7V and 1.5V respectively.

b. 6T and 9T performance comparison under voltage variation

The 9T SRAM improves upon this resilience further, with its soft error probability reducing by 10.6% and 20.89% at 0.7V and 1.5V respectively in comparison to the 6T SRAM. The 9T SRAM has a comparatively increased signal noise margin, allowing it to tolerate more noise before the data of the memory node is corrupted (Singh et al., 2010). As such, it presents a higher critical charge and lower error probability than the 6T SRAM.

c. 9T and transmission gate transient filter performance comparison under voltage variation

The transmission gate transient filter is able to achieve the lowest soft error probability of 13.01% at 0.7V and 13.31% at 1.5V lesser than the 9T SRAM. The 9T SRAM node isolation feature presents an advantage for the read operation but also operates at a low power threshold in the hold state which results in a lower critical charge and higher error probability, as opposed to the mitigative effect of the transient filter which allows the transmission gate SRAM to achieve a comparably lower error probability (Manoj Kumar & Sridevi, 2018).

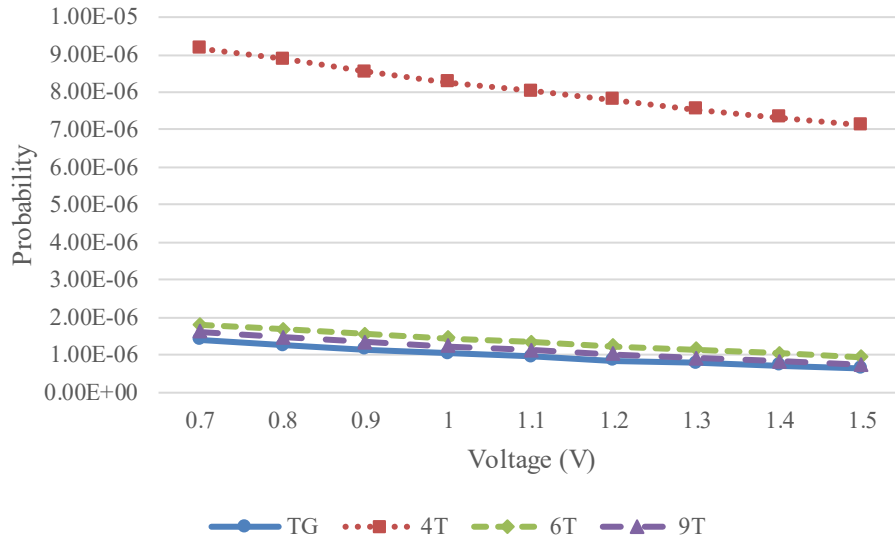


Figure 4.34: Probability vs voltage for SRAMs in hold state for PMOS drain (1-0)

vii. Probability vs temperature for SRAMs in hold state for NMOS drain (0-1)

a. 4T and 6T performance comparison under temperature variation

Figure 4.35 shows the soft error probability response to the temperature variation of the 4T, 6T, 9T, and transmission gate SRAMs for the NMOS drain, which is represented by Q and QB for (0-1). The 4T SRAM performed relatively poorly of the selected SRAM cells, with the 6T performing better by a margin of 28% and 28.87% at -50 °C and 200 °C. The increased critical charge of the 6T SRAM is due to the use of PMOS transistors as a pull up system as opposed to the polyresistors of the 4T SRAM, allowing for a lower error probability (Manohar et al., 2020).

b. 6T and 9T performance comparison under temperature variation

The soft error probability of the 9T SRAM is reduced further by 44.28% and 20.08% for -50 °C and 200 °C in comparison to the 6T SRAM. The stability of the 9T SRAM is due

to the increased static noise margin relative to the 6T SRAM, allowing for an increased critical charge and lower error probability (Marques et al., 2020).

c. 9T and transmission gate transient filter performance comparison under temperature variation

The transmission gate transient filter SRAM also has an improvement of soft error probability of 29.38% and 18.53% at -50 °C and 200 °C, respectively, relative to the 6T SRAM. It is apparent that the transmission gate transient filter is also capable of matching the performance of the 9T SRAM and even outperforming the 9T SRAM at voltages lower than 1V. One weakness of the 9T SRAM is that while it does have a stronger pull-down capability compared to the 6T SRAM due to its separate read bitline, the pull-up architecture is essentially identical to the 6T SRAM, providing no additional improvements on the memory nodes when the node is holding the logic value of 1. This can be compared to the transmission gate transient filter SRAM which provides mitigative protection on both the pull-up and pull-down nodes and increasing the critical charge on both aforementioned nodes, thus resulting in a more holistic defence against soft errors.

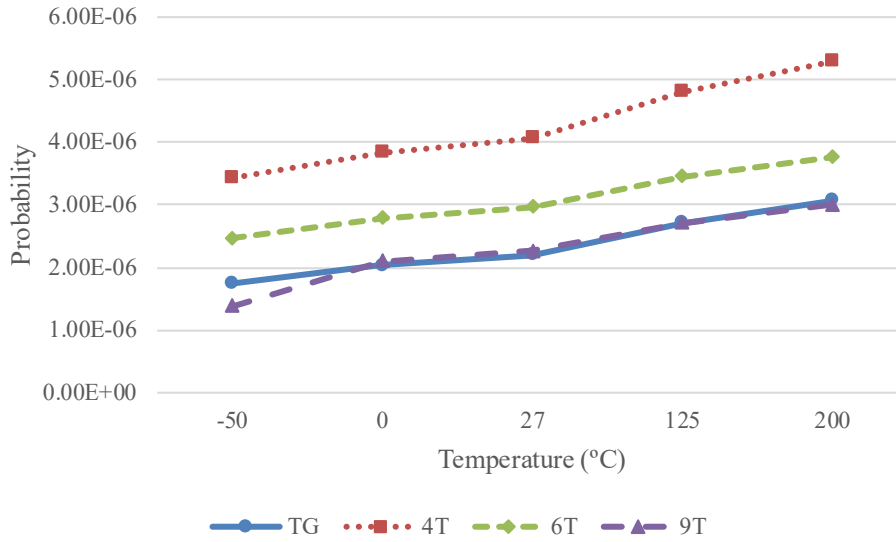


Figure 4.35: Probability vs temperature for SRAMs in hold state for NMOS drain (0-1)

viii. Probability vs temperature for SRAMs in hold state for PMOS drain (1-0)

a. 4T and 6T performance comparison under temperature variation

Figure 4.36 shows the soft error probability response to the temperature variation of the 4T, 6T, 9T, and transmission gate SRAMs for the PMOS drain, which is represented by Q and QB for (1-0). The SRAM that exhibits the highest probability for soft error is the 4T SRAM, followed by the 6T SRAM. The 6T SRAM presents an improvement in probability of 82.81% and 82.41% at -50 °C and 200 °C from that of the 4T SRAM. The additional transistor count lends to an additional resistance against the temperature variation, thus increasing the critical charge despite the increase in sensitive node area, ultimately resulting in a lower error probability (Wang & Tseng, 2019).

b. 6T and 9T performance comparison under temperature variation

The 9T SRAM improves upon its soft error probability, exhibiting a reduced probability of 14.77% and 15.28% at -50s °C and 200 °C compared to the 6T SRAM. The

increased node area resulted in an increased critical charge that was able to offset the increase in error probability, thus resulting in an improvement over the 6T SRAM (Rahman et al., 2016).

c. 9T and transmission gate transient filter performance comparison under temperature variation

The transmission gate transient filter also presents an improved soft error probability from that of the 9T SRAM, achieving a probability of 21.09% and 1.9% lower at -50 °C and 200 °C. While the transmission gate transient filter presents a lower error probability than the 9T SRAM, the difference is not so apparent at higher temperatures as the electron mobility increases at higher temperatures, causing an increase in soft error rate (Nie et al., 2017).

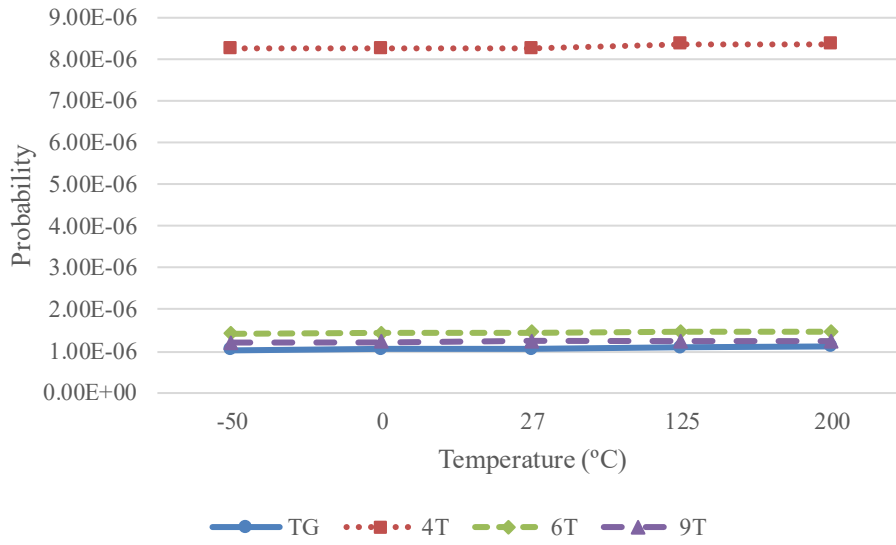


Figure 4.36: Probability vs temperature for SRAMs in hold state for PMOS drain (1-0)

4.4 Design comparisons

The transient filter proposed in this study has been compared in effectiveness against different strategies devised to increase soft error robustness through the strengthening of the critical charge of the device. Ahirwar et al. (2023) proposed that adjustments to the architecture of SRAM could be made to result in a product that boasted fewer sensitive nodes as well as error recovery. These improvements still come at the cost of a larger area overhead. The transient filter SRAM proposed in this study was able to achieve a greater improvement in critical charge while enforcing a lower cost in terms of area overhead. Furthermore, the transient filter critical charge improvement was also compared to that proposed by Cazeaux et al. (2005) which employed cell ratio optimising in SRAMs in order to produce a width length ratio in the transistors that would suitably ward off the transients that result from

single event upset. This method, however, must be used in conjunction with other mitigative strategies and its feasibility decreases as the process node approaches sub-nano sizes.

A similar approach was undertaken by Rajendran et al. (2011) wherein the ratio of the transistor sizing was modulated in order to achieve a desired level of optimisation of radiation tolerance with consideration towards operations within performance constraints of critical charge, write time delay and power consumption. This approach however, was able to achieve a critical charge improvement of 58% percent at most. The performance comparisons of the various designs are illustrated as shown in the Table 4.1 as below.

Table 4.1: Comparison against different single event transient strategies

No.	Technique	Critical charge improvement (%)
1.	Radiation hardening by design (Ahirwar et al., 2023)	81.88
2.	Cell ratio optimizing (Cazeaux et al., 2005)	24
3.	Transistor sizing ratio (Rajendran et al., 2011)	58
4.	Transmission gate transient filter	88.63

4.5 Summary

In this chapter, the results of the simulations were discussed and analysed. The critical charge of the SRAM cells in response to voltage and temperature variation from each node were obtained. Furthermore, the critical charges of the SRAM cells were studied in

terms of the standard deviation to deduce the effects of voltage and temperature. Finally, the probability of soft error was calculated for each respective SRAM. The soft error robustness of each SRAM in terms of soft error probability was then compared and analysed.

CHAPTER 5

CONCLUSION AND RECOMMENDATIONS

5.1 Conclusion

Reducing the size of electronics to the submicron scale has introduced a longstanding challenge along with a fresh concern: safeguarding circuitry from errors, particularly the issue of single event upsets. To ensure that complementary metal oxide semiconductor (CMOS) technology adheres to Moore's law, novel design strategies are imperative to sustain its ongoing progress. Shrinking technology dimensions result in increased circuit density within a limited space, thereby elevating vulnerability to soft errors.

This study has contributed to a method to formulate the probability of soft error corrupting a data node, allowing the evaluation of the likelihood of a bit flip occurring within a node in the inverter loop of an SRAM. The effects of voltage supply and temperature variation on the likelihood of soft error was investigated. The effect of voltage supply and temperature variation was investigated on memory nodes holding a '1' and '0'. The nodes were injected with a transient current of increasing magnitude until the stored data was inverted. The magnitude and the pulse width of the transient current was then used to calculate the critical charge of each node in the inverter loop of various SRAMs, then the calculation of the probability of soft error for each node by vulnerable as compared to the total vulnerable area of the inverter loop. The step was repeated for each increment of voltage supply and temperature to deduce the effect of voltage and temperature variation on the soft error probability. This method thus provides an alternative to the Monte Carlo, as the formulation of error probabilities can allow for the targeted evaluation of specific nodes

within a circuit rather than the entire circuit at large. As the formulation is based upon the empirical data obtained from previous work, the method produces an evaluation of error probability that is versatile and keeping pace with the downscaling of device dimensions.

Moreover, this method is capable of evaluating the soft error probability of both NMOS and PMOS transistors given the length and width parameters of the transistors are known. The study also analysed the reliability of the SRAMs against soft errors through the scrutiny of the critical charge subject to the variation of supply voltage and temperature, standard deviation of the SRAMs and the calculated probability of the soft error.

The study has also investigated the implementation of transmission gates as transient filters for the purpose of mitigating the transient currents that are induced as a result of particle strikes from radiation sources. The transmission gate functioned to successfully mitigate the transient between the memory nodes of the SRAM to a significant extent. When the transmission gate transient filter was amended to the 6T SRAM architecture, the magnitude of the transient current required to flip the bit stored at the memory is greatly increased. The increased resistance of the transmission gate due to the reduced gate voltages of the NMOS and PMOS transistors allowed for the filter to suppress larger magnitudes of transient currents, resulting in a more robust SRAM design. The study has also produced a transient filter that improved on the critical charge of the conventional 6T SRAM by up to 88%.

5.2 Recommendations

With the downscaling of technology comes an increase in soft error rates, therefore more research is needed in order to combat this phenomenon and maintain device robustness. Some paths that can be explored in future works are detailed as follows.

The probability formulation presented in this work can be tested on different CMOS structures such as FinFET or fully depleted silicon on insulator (FD-SOI). As different structures provide different subthreshold slopes, the trend of soft error probability across varying voltage and temperatures could provide valuable insight to the probability response. It is imperative that these CMOS structures are evaluated in terms of soft error probability, especially within the context of fields that require a high amount of robustness and reliability. Testing on these processes can also provide data on how the proposed probability model performs when evaluating the soft error probability of processes other than CMOS.

The aerospace industry has a high demand for SRAM-based technology, but the same technology can be vulnerable to soft errors induced by cosmic radiation. Failures in the technology can lead to a significant loss in life and resources, therefore it is essential that there is a method to evaluate the robustness of the designs. Furthermore, memory circuits in medical devices like pacemakers are exposed to a wide spectrum of radiation especially during air travel or treatments like radiotherapy. Thus the mitigation of soft errors that are area efficient and scalable would be suitable for implementation in such devices.

The probability formulation proposed in this study can be used to evaluate the designs of CMOS memory circuits from aerospace and medical devices. Parameters of memory circuits can be sourced from vendors that for aerospace and medical devices can be tested and evaluated for their robustness against soft errors. Furthermore, the sizing relationship of the proposed transmission gate transient filter should be described and formulated to be allow for ease of design before implementation. As the relationship of the transmission gate sizing and its mitigative effect has yet to be defined, the formulation of the method would be a great contribution.

Lastly, the transmission gate transient filter should undergo radiation testing to obtain empirical results for the transient filter response to actual radiation exposure. As the simulation defined a current pulse model, further investigation is warranted with irradiation experiments involving particle firing which would allow for characterization of the profile of the linear energy transfer, and thus provide an evaluation of the transient filter in real world use.

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APPENDICES