



Faculty of Engineering

**Efficient Control Strategy of Photovoltaic Grid-Connected
Microinverters with Improved Topology**

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Efficient Control Strategy of Photovoltaic Grid-Connected Microinverters with Improved Topology

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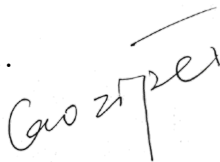
Faculty of Engineering
UNIVERSITI MALAYSIA SARAWAK
2024

DECLARATION

I declare that the work in this thesis was carried out in accordance with the regulations of Universiti Malaysia Sarawak. Except where due acknowledgements have been made, the work is that of the author alone. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

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ABSTRACT

The microinverter is the core component of modular photovoltaic grid-connected power generation systems. It offers advantages such as convenience, flexibility, high security, and high reliability. However, there are drawbacks of microinverters in terms of service life, conversion efficiency, and cost. This research focused on reducing losses, increasing efficiency, and lowering costs via an improved flyback topology structure and a novel control strategy. This thesis proposed an interleaved parallel passive clamp flyback topology with a compensation capacitor. By adding the compensation capacitor to reduce the switching frequency of the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET), a passive clamp is used to absorb the leakage inductance energy. Besides, an interleaved parallel topology is introduced to increase output power and suppress ripple, highlighting its stability and cost-effectiveness compared to other flyback topologies. Based on the topology structure, considering the parasitic parameters of various components and referencing various circuit parameters, along with the derived peak current reference curve, a novel multi-valley turn-on strategy is proposed to minimize the voltage stress during the MOSFET turn-on. Additionally, a prototype and experimental platform of a flyback microinverter based on the proposed topology structure and control strategy were constructed. Through simulation and experimentation, it was determined that the interleaved parallel passive clamp flyback topology with compensating capacitors can effectively extend the resonant period by 10.78%, reduce the peak voltage of the MOSFET by 9.8%, decrease the harmonic content by 0.91%, and simultaneously address the issue of component reuse. Based on the

multi-valley turn-on strategy, the microinverter achieves valley turn-on under different grid phases, with a maximum efficiency of 97.49% and a stable Total Harmonic Distortion (THD) ranging from 2.22% to 2.59% in the simulation. The final experimental prototype achieves a maximum efficiency of 96.01% at full load, with a THD of the grid current of 2.67%. By comparing simulation and experimental results, this thesis validated the stability of the proposed topology structure and the effectiveness of the control strategy, reducing switch losses, extending inverter lifespan, improving efficiency, and reducing costs. This research can be widely applied in the industrial field of microinverters, translating into practical outcomes and promoting the development of photovoltaic technology.

Keywords: Compensation capacitor, experimental platform, interleaved flyback topology, multi-valley turn-on control strategy, passive clamping

Strategi Kawalan Novel Bagi Pemacu Mikro Terhubung Talian Grid Fotovoltan dengan Struktur Topologi yang Diperbaiki

ABSTRAK

Mikroinverter adalah komponen utama dalam sistem penjanaan tenaga grid fotovoltai modular. Ia menawarkan kelebihan seperti kemudahan, fleksibiliti, keselamatan yang tinggi, dan kebolehpercayaan yang tinggi. Namun, terdapat kelemahan pada mikroinverter dari segi jangka hayat, kecekapan penukaran, dan kos. Penyelidikan ini memberi tumpuan kepada pengurangan kerugian, peningkatan kecekapan, dan pengurangan kos melalui struktur topologi flyback yang dipertingkatkan dan strategi kawalan yang baharu. Tesis ini mencadangkan topologi flyback penyepit pasif selari yang diselang-seli dengan kapasitor pampasan. Dengan menambah kapasitor pampasan untuk mengurangkan kekerapan suis Transistor Kesan Medan Semikonduktor Oksida Logam (MOSFET), penyepit pasif digunakan untuk menyerap tenaga aruhan bocor. Selain itu, topologi selari yang diselang-seli diperkenalkan untuk meningkatkan kuasa output dan menindas riak, yang menonjolkan kestabilan dan keberkesanan kosnya berbanding topologi flyback yang lain. Berdasarkan struktur topologi, dengan mengambil kira parameter parasit bagi pelbagai komponen dan merujuk kepada pelbagai parameter litar, bersama dengan lengkung rujukan arus puncak yang diperolehi, satu strategi turn-on multi-lembah yang baharu dicadangkan untuk meminimumkan tekanan voltan semasa MOSFET dihidupkan. Tambahan pula, satu prototaip dan platform eksperimen mikroinverter flyback berdasarkan struktur topologi dan strategi kawalan yang dicadangkan telah dibina. Melalui simulasi dan eksperimen, didapati

bahawa topologi flyback penyepit pasif selari dengan kapasitor pampasan dapat memanjangkan tempoh resonan sebanyak 10.78%, mengurangkan voltan puncak MOSFET sebanyak 9.8%, mengurangkan kandungan harmonik sebanyak 0.91%, dan pada masa yang sama menangani isu penggunaan semula komponen. Berdasarkan strategi turn-on multi-lembah, mikroinverter mencapai turn-on lembah di bawah fasa grid yang berbeza, dengan kecekapan maksimum sebanyak 97.49% dan Jumlah Harmonik Teranggu (THD) yang stabil antara 2.22% hingga 2.59% dalam simulasi. Prototaip eksperimen akhir mencapai kecekapan maksimum sebanyak 96.01% pada beban penuh, dengan THD arus grid sebanyak 2.67%. Dengan membandingkan hasil simulasi dan eksperimen, tesis ini mengesahkan kestabilan struktur topologi yang dicadangkan dan keberkesanan strategi kawalan, mengurangkan kerugian suis, memanjangkan jangka hayat inverter, meningkatkan kecekapan, dan mengurangkan kos. Penyelidikan ini boleh digunakan secara meluas dalam bidang industri mikroinverter, memberikan hasil praktikal dan mempromosikan perkembangan teknologi fotovoltai.

Kata kunci: *Kapasitor pampasan, platform eksperimen, topologi flyback bersilang, strategi kawalan pemutaran beberapa lembah, pengekalan pasif*

TABLE OF CONTENTS

	Page
DECLARATION	i
ACKNOWLEDGEMENT	ii
ABSTRACT	iii
ABSTRAK	v
TABLE OF CONTENTS	vii
LIST OF TABLES	xii
LIST OF FIGURES	xiii
LIST OF ABBREVIATIONS	xviii
CHAPTER 1 INTRODUCTION	1
1.1 Introduction	1
1.2 Study Background	3
1.3 Problem Statement	8
1.4 Research Hypothesis	9
1.5 Objectives	10
1.6 Scope of Study	11
1.7 Significant Contributions	12

1.8	Chapter Summary	13
CHAPTER 2 LITERATURE REVIEW		15
2.1	Introduction	15
2.2	Microinverter Topology	15
2.2.1	Classification of Microinverters	15
2.2.1.1	Microinverter with DC-link	16
2.2.1.2	Microinverter without DC-Link	20
2.2.1.3	Microinverter with Pseudo DC Link	23
2.2.2	Flyback Microinverter	28
2.2.2.1	Single-Ended Flyback Topology	28
2.2.2.2	Interleaved Parallel Flyback Topology	31
2.2.2.3	Clamping Technology	33
2.3	Flyback Topology Control Strategy	39
2.3.1	Classification of Operating Modes for Flyback inverters	39
2.3.1.1	Discontinuous Conduction Mode	40
2.3.1.2	Continuous Conduction Mode	44
2.3.1.3	Boundary Conduction Mode	46
2.3.2	Comparison of the Operating Characteristics of the Three Modes	47

2.3.3	Comparison of the Control Strategies for Three Modes	49
2.4	Summary	53
CHAPTER 3 RESEARCH METHODOLOGY		56
3.1	Introduction	56
3.2	Research Methodology Flowchart	56
3.3	Simulation Software	59
3.4	Design of the Topology Structure	59
3.4.1	Construction of the Conventional Topology	60
3.4.1.1	Construction of the Conventional Topology Model	60
3.4.1.2	Verification of the Conventional Topology Model	63
3.4.2	Design of the Improved Topology	64
3.4.2.1	Single-Ended Flyback Topology with a Compensation Capacitor	65
3.4.2.2	Single-Ended Flyback Topology with a Passive Clamping Circuit	70
3.4.2.3	Interleaved Parallel Passive Clamping Flyback Topology	74
3.5	Developed Control Strategy	78
3.5.1	Parameter Extraction Method	80
3.5.1.1	MPPT Algorithm	80
3.5.1.2	PLL Algorithm	83

3.5.2	Derivation Process of the Reference Current Curve	86
3.5.3	Implementation Process of the Control Strategy	89
3.6	Fabrication of the Experimental Platform	91
3.6.1	Design of Hardware Circuits	92
3.6.1.1	Design of the DC–DC Conversion Unit	93
3.6.1.2	Design of the DC–AC Conversion Unit	98
3.6.1.3	Design of the Grid-Connected Unit	98
3.6.1.4	Design of the Sampling Circuits	101
3.6.1.5	Design of the Driver Circuits	108
3.6.2	Design of Software Processes	110
3.6.2.1	Main Program and State Machine	110
3.6.2.2	ADC Interruption Subprogram	113
3.7	Summary	114
CHAPTER 4 RESULTS AND DISCUSSION		116
4.1	Introduction	116
4.2	Topology Structure	116
4.2.1	Single-Ended Flyback Topology with a Compensation Capacitor	117
4.2.2	Single-Ended Passive Clamping Flyback Topology	121

4.2.3	Interleaved Parallel Flyback Topology	125
4.3	Multi-Valley Turn-on Control Strategy	130
4.3.1	Simulation Results of the Peak Current Reference Curve	130
4.3.2	Simulation Results of the Control Strategy	131
4.4	Microinverter Experimental Platform	137
4.4.1	Construction of the Experimental Prototype	138
4.4.2	Construction of the Experimental Platform	139
4.4.3	Experimental Results and Analysis	141
4.4.3.1	Implementation and Comparison of Control Strategies	141
4.4.3.2	Implementation of the DC–DC Flyback Circuit	145
4.4.3.3	Implementation of the DC–AC inverter circuit	146
4.5	Summary	149
CHAPTER 5 CONCLUSIONS AND FUTURE WORK		150
5.1	Concluding Remarks	150
5.2	Future work	152
REFERENCES		154
APPENDICES		173

LIST OF TABLES

	Page
Table 2.1 Comparison of Microinverters with DC-Link	19
Table 2.2 Comparison of Microinverters without DC-Link	22
Table 2.3 Comparison of Microinverters with Pseudo DC-link	26
Table 2.4 Comparison of Microinverters with Three Topological Structures	27
Table 2.5 Comparison of Flyback Topologies	33
Table 2.6 Comparison of Clamping Technologies	38
Table 2.7 Comparison of the Operating Characteristics of the Three Modes	48
Table 2.8 Comparison of the Control Strategies for Three Modes	52
Table 3.1 Key Parameters of the Conventional Topology Model	62
Table 3.2 Key Parameters of the Improved Topology Model	78
Table 3.3 Design parameters of the Flyback Transformer	95
Table 3.4 Three States of the State Machine	113
Table 4.1 ElementNum Comparison of Different Clamping Topologies	129
Table 4.2 Component Parameters Required for the Control Strategy	131
Table 4.3 Comparison of Different Literature Studies	148

LIST OF FIGURES

	Page
Figure 1.1 Global Photovoltaic Installation Volume and Proportion by Type	2
Figure 1.2 Flow Chart of the Photovoltaic Grid-Connected System	3
Figure 1.3 Classification of Photovoltaic Inverters	3
Figure 1.4 Fire Cases at Photovoltaic Power Stations	5
Figure 1.5 Problems Encountered in Distributed Buildings	6
Figure 1.6 Organization of the Content of This Thesis	14
Figure 2.1 Structure with DC-Link	16
Figure 2.2 Topologies with DC-Link	18
Figure 2.3 Structure without DC-Link	20
Figure 2.4 Topologies without DC-Link	22
Figure 2.5 Structure with Pseudo DC-Link	23
Figure 2.6 Topologies with Pseudo DC-Link	25
Figure 2.7 Flyback Topology 1	29
Figure 2.8 Flyback Topology 2	30
Figure 2.9 Flyback Topology 3	30
Figure 2.10 Typical Topology of the Interleaved Flyback Microinverter	32
Figure 2.11 Active Clamping Circuit in Flyback Converters	35
Figure 2.12 Passive Clamping Circuit with RCD	36
Figure 2.13 Passive Clamping Circuit with a Dual-Transistor	37
Figure 2.14 Passive Clamping Circuit with LCD	37
Figure 2.15 Simplified Diagram of the Flyback Conversion Topology	39

Figure 2.16	Primary and Secondary Current Waveforms in DCM	41
Figure 2.17	Primary and Secondary Current Waveforms in CCM	44
Figure 2.18	Primary and Secondary Current Waveforms in BCM	46
Figure 2.19	Actual Primary Current Curves under Different Initial Values	52
Figure 3.1	Flowchart of the Research	58
Figure 3.2	Simulation Model of the Conventional Flyback Topology Circuit	61
Figure 3.3	Key Waveforms of the Conventional Flyback Topology Model	63
Figure 3.4	Single-Ended Flyback Topology with the Compensation Capacitor	65
Figure 3.5	Primary and Secondary Current Waveforms of the Flyback Transformer in DCM	67
Figure 3.6	Mode 1 of the Single-Ended Flyback Topology	68
Figure 3.7	Mode 2 of the Single-Ended Flyback Topology	68
Figure 3.8	Mode 3 of the Single-Ended Flyback Topology	69
Figure 3.9	Single-Ended Passive Clamping Flyback Topology	70
Figure 3.10	Operating Process Waveforms of Passive Clamping	71
Figure 3.11	Mode 1 of the Passive Clamping Flyback Topology	71
Figure 3.12	Mode 2 of the Passive Clamping Flyback Topology	72
Figure 3.13	Mode 3 of the Passive Clamping Flyback Topology	73
Figure 3.14	Mode 4 of the Passive Clamping Flyback Topology	73
Figure 3.15	Mode 5 of the Passive Clamping Flyback Topology	74
Figure 3.16	Mode 6 of the Passive Clamping Flyback Topology	74
Figure 3.17	Main Circuit Topology of the Interleaved Flyback Grid-Connected Microinverter	75
Figure 3.18	Current Waveforms of the Interleaved Flyback Topology in DCM	76
Figure 3.19	Flyback Converter Unit of the Improved Topology Model	77

Figure 3.20	Control Strategy Diagram	79
Figure 3.21	DC–DC Control System	80
Figure 3.22	Flowchart of the P&O Method	81
Figure 3.23	MPPT Algorithm Model	82
Figure 3.24	MPPT Model Simulation Result	83
Figure 3.25	DC–AC Control System	84
Figure 3.26	Control Block Diagram of SOGI-PLL	84
Figure 3.27	PLL Algorithm Model	85
Figure 3.28	PLL Model Simulation Result	86
Figure 3.29	System Functional Block Diagram of the Experimental Platform	92
Figure 3.30	Grid-Connected Unit Equivalent Circuit	99
Figure 3.31	Voltage Sampling Circuit of the Photovoltaic Modules	102
Figure 3.32	Current Sampling Circuit of the Photovoltaic Module	103
Figure 3.33	Current Sampling Circuit of the MOSFET	104
Figure 3.34	Voltage Sampling Circuit of Flyback Output	105
Figure 3.35	Grid Voltage Sampling Circuit	106
Figure 3.36	Zero-Crossing Signal Detector Circuit	106
Figure 3.37	Sampling Circuit of Grid-Connected Current	107
Figure 3.38	MOSFET Driver Circuit of the DC-DC Conversion Unit	109
Figure 3.39	Thyristor Driver Circuit	110
Figure 3.40	Software Flowchart of the Main Program	111
Figure 3.41	Software Flowchart for the State Machine Loop Subprogram	112
Figure 3.42	Software Flowchart of the ADC Interrupt Subprogram	114
Figure 4.1	Key Waveforms of Single-Ended Flyback Topology	118

Figure 4.2	Voltage across the Switch before and after Adding Compensation Capacitor	120
Figure 4.3	Transistor Power Loss with Different C_x	121
Figure 4.4	Key Waveforms of Single-Ended Passive Clamping Flyback Topology	122
Figure 4.5	Comparison of the Drain-Source Voltage Waveforms with and without the Clamping Circuit.	123
Figure 4.6	Grid Voltage and Grid-Connected Current Waveforms of the Single-Ended Passive Clamping Flyback Microinverter	124
Figure 4.7	Waveforms of the Grid Voltage and Grid-Connected Current of the Interleaved Flyback Topology	125
Figure 4.8	Primary Currents of Interleaved Flyback Topology	126
Figure 4.9	Overall Key Waveforms of the Interleaved Passive Clamping Flyback Topology	127
Figure 4.10	Detailed Key Waveforms of the Interleaved Passive Clamping Flyback Topology	128
Figure 4.11	Peak Current Reference Curves for Different Numbers of Resonances	130
Figure 4.12	Waveforms of the Transistor Voltage and Transformer Current	132
Figure 4.13	Waveforms of the Transistor Voltage and Transformer Current at Different Phases	134
Figure 4.14	Efficiency Curves of the Two Strategies	135
Figure 4.15	Voltage and Current Waveforms of Two Strategies	136
Figure 4.16	THD Values of the Two Strategies	137
Figure 4.17	Microinverter Prototype	138
Figure 4.18	Experimental Platform	141
Figure 4.19	MOSFET Q Waveforms of the Fixed-Frequency Control Strategy	143
Figure 4.20	Key Signal Waveforms of Multi-Valley Turn-on Control Strategy	145
Figure 4.21	Waveforms of the Driving Signals and Primary Currents	146

Figure 4.22 Waveforms of the Grid Voltage and Grid-Connected Current	147
Figure 4.23 Power Curve	147

LIST OF ABBREVIATIONS

AC	Alternating Current
BCM	Boundary Conduction Mode
CCM	Continuous Conduction Mode
CPU	Central Processing Unit
CT	Current sense Transformer
DC	Direct Current
DCM	Discontinuous Conduction Mode
DSP	Digital Signal Processor
EMC	Electromagnetic Magnetic Compatibility
LCD	Inductor-Capacitor-Diode
MCU	Microprogrammed Control Unit
MOSFET	Metal–Oxide–Semiconductor Field Effect Transistor
MPPT	Maximum Power Point Tracking
MPP	Maximum Power Point
MVTO	Multi Valley Turn-on
NMOS	Negative Channel Metal Oxide Semiconductor
P&O	Perturb and Observe
P-U	Power-Voltage
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
PMOS	Positive Channel Metal Oxide Semiconductor

PSIM	Power Simulation software
PV	Photovoltaic
PWM	Pulse-Width Modulation
RCD	Resistor-Capacitor-Diode
RMS	Root Mean Square
SOGI-PLL	Second-Order Generalized Integrator Phase-Locked Loop
SPWM	Sinusoidal Pulse Width Modulation
THD	Total Harmonic Distortion
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

CHAPTER 1

INTRODUCTION

1.1 Introduction

Energy is the key and foundation of a country's national economic lifeline. With the exhaustion of fossil energy and the environmental pollution caused by traditional energy power generation, the new energy revolution oriented towards clean and low carbon is booming around the world. It is urgent to find new energy sources to replace traditional fossils. Therefore, the increase in renewable energy power generation has attracted the attention of various countries and has become a research hotspot around the world. As a renewable and clean energy source, solar energy has many advantages, such as wide distribution, no pollution, low cost, and simple exploitation. Therefore, the photovoltaic power generation technology led by solar energy is undoubtedly the most favourable measure for solving the energy crisis, ecological environment destruction and sustainable development and has unlimited market and development prospects (Lee et al., 1999; Giwa et al., 2017; Sen & Ganguly, 2017).

According to the "Global Photovoltaic Tracker Market Report" published by IHS Markit in 2020, as shown in Figure 1.1, the global photovoltaic industry is developing rapidly, and the newly installed photovoltaic capacity is increasing annually. It is expected that by the end of 2025, the newly installed capacity will reach 400 GW, an increase of 167% compared with 150 GW at the end of 2021. The advantages of solar energy, such as its

cleanliness and convenience, will attract more countries' attention. The entire photovoltaic industry is divided into ground power stations, industrial and commercial power stations, and household use. The abovementioned industrial, commercial, and household users are collectively referred to as distributed photovoltaics. The proportion of distributed photovoltaics will continue to grow, and it is expected to reach 56% by 2025, especially in the household market, which has the largest growth space in the future.

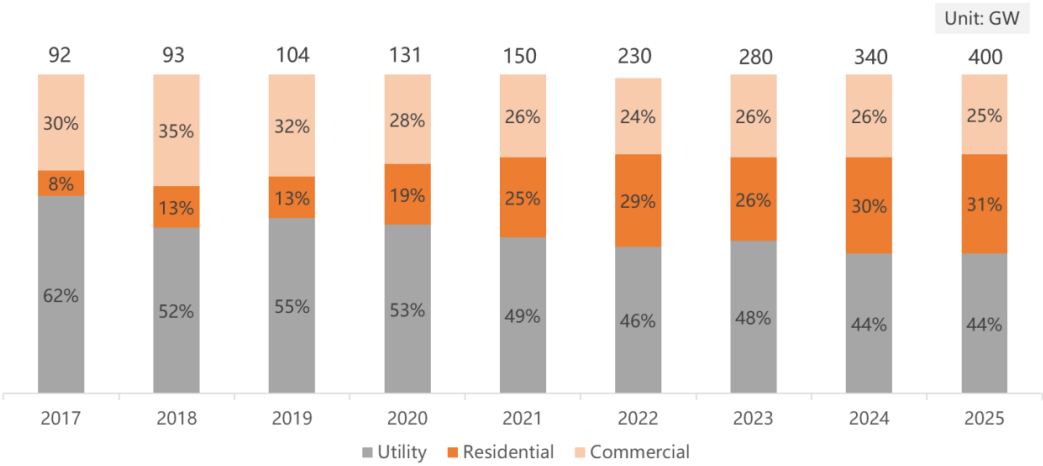


Figure 1.1: Global Photovoltaic Installation Volume and Proportion by Type

The composition of the photovoltaic grid-connected power generation system is shown in Figure 1.2 (Tang et al., 2022). The sunlight irradiates the photovoltaic panel to generate DC power. The DC power must be boosted by the grid-connected inverter and then converted into AC power to connect to the AC load or the public grid. The inverter is the core equipment and the energy transmission centre of the photovoltaic grid-connected system. Its performance plays a decisive role in the operating quality of the entire system (Tacca, 1998; Kjaer et al., 2005; Chiu et al., 2013; Shafiullah et al., 2022; Sutikno et al., 2022; Tang et al., 2022).

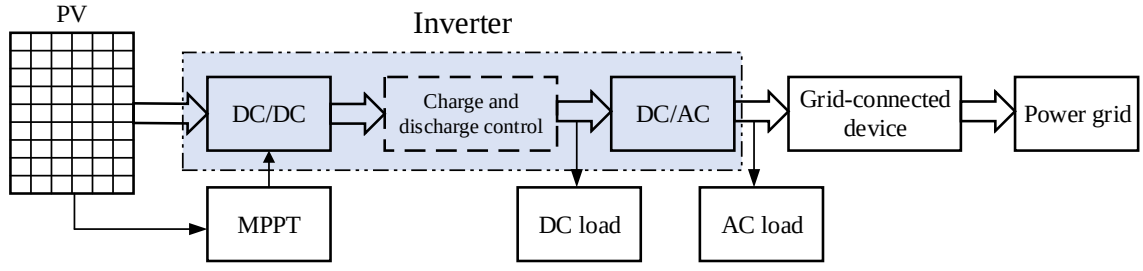


Figure 1.2: Flow Chart of the Photovoltaic Grid-Connected System

1.2 Study Background

The inverter can be broadly divided into three categories based on how it is connected to the photovoltaic module: centralized, string, and microinverter, as shown in Figure 1.3 (Zhang, 2016).

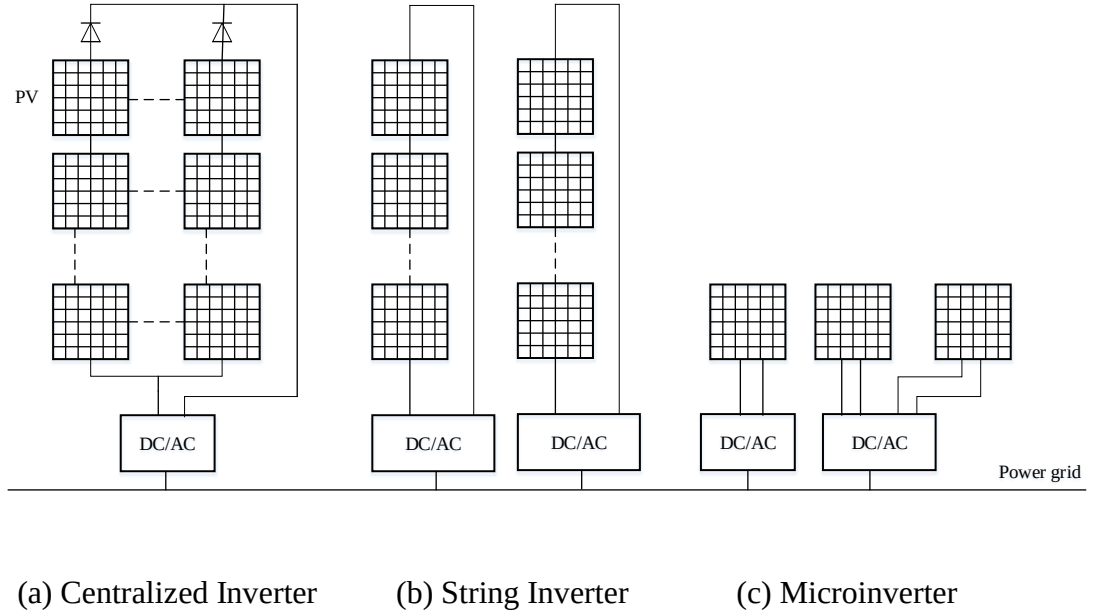


Figure 1.3: Classification of Photovoltaic Inverters

In a centralized grid-connected power generation system, solar photovoltaic modules are connected in series to obtain high-voltage DC, and then the photovoltaic combiner boxes are connected in parallel to increase the output power. Finally, the centralized grid-connected

inverter transfers the concentrated energy to the grid, as shown in Figure 1.3 (a). Its structure is simple, the scale of its application is more than 500 kW under high voltage and even ultrahigh voltage conditions, and it is mainly used in ground power stations (Bhattar & Chaudhari, 2023).

A string structure grid-connected power generation system connects the components in series and directly converts the DC power into AC power through a string inverter, as shown in Figure 1.3 (b). The application scale of this system is between 3 KW and 500 KW, and it can be used in ground power stations, distributed households, and industrial and commercial photovoltaic power stations at the same time (Kaundinya et al., 2009).

These two inverters are widely used, but there are two major problems, which are listed below (Shafiullah et al., 2022; Sutikno et al., 2022; Tang et al., 2022).

- i. Security risk: The high voltage on the DC side of conventional centralized and string inverters is the "tinderbox" on the roof. Statistics from numerous well-known photovoltaic websites show that more than 80% of fires in photovoltaic power stations are caused by faults on the DC side, particularly fires triggered by component hotspots, electrical circuit loose connections, and DC arcing issues. Figure 1.4 is four cases of photovoltaic power plant fires.



(a) Household Power Station



(b) Apple's Commercial Photovoltaic Power Station



(c) Village-Level Photovoltaic Power Station



(d) Rooftop Photovoltaic Power Station of a Primary School

Figure 1.4: Fire Cases at Photovoltaic Power Stations

- ii. Barrel effect: Due to dust, tree shadows, building occlusion, bird droppings, multidirectional roofs, human factors, etc., as shown in Figure 1.5, in distributed buildings, the power generation efficiency and instantaneous power of each component cannot be guaranteed to be completely consistent. The power generation capacity of conventional photovoltaic systems is determined by the weakest link in the series rather than the strongest link. Moreover, when the inverter fails, it will affect the power generation of the entire system. The barrel effect will lead to a loss of power generation.

Improving the power generation of photovoltaic systems is also a key issue that the industry has been exploring continuously (Aman et al., 2015).



(a) Shelter



(b) Dust and Guano



(c) Multi-Faceted Roof



(d) Human Factors

Figure 1.5: Problems Encountered in Distributed Buildings

In addition, users cannot expand the photovoltaic power generation system of any power according to their own needs and can only match the power of conventional inverters, so the scalability of the system is poor.

Microinverters solve all of the above problems. The microinverter grid-connected power generation system directly converts the electrical energy generated by each component into AC and then connects to the grid, as shown in Figure 1.3 (c). Compared with centralized or string photovoltaic inverters, photovoltaic grid-connected microinverters have the following advantages (Myrzik & Calais, 2003; Bidram et al., 2012; Scholten et al., 2013;

Meneses et al., 2013; Kouro et al., 2015; Blaabjerg, 2018; Yaqoob & Obed, 2021; Díaz et al., 2023):

- i. No barrel effect: Microinverters have strong adaptability to the influence of uneven lighting conditions. Each component independently performs Maximum Power Point Tracking (MPPT) through the microinverter. When a certain component is shaded, it will not affect the maximum power output of other components, which can increase the power generation of the system as a whole.
- ii. Convenience and flexibility. It is small in size, easy to realize modular production, convenient for installation and maintenance, flexible and easy to use, and can reduce maintenance and management costs;
- iii. High security. There is no high-voltage DC switching process in the system, and a DC arc will not be formed to cause fire. The low DC voltage of the system does not easily cause electric shock safety accidents
- iv. High reliability. Even if a photovoltaic (PV) module or microinverter fails, other modules and inverters will not be affected.

Although the global inverter market is currently dominated by string inverters, followed by central inverters, the market share of microinverters remains relatively low. However, based on these advantages, photovoltaic microinverters have developed rapidly in

recent years and are widely used in distributed photovoltaic power generation systems. According to data from the research firm Wood Mackenzie, the market share of microinverters, based on shipment value, has increased from 5% in 2018 to 10% in 2023.

1.3 Problem Statement

Like string and centralized grid-connected inverters, microinverters are also the core of the interaction between photovoltaic modules and the grid and must meet both the output characteristics of the module side and the requirements of grid-connection standards on the grid side. Because of their special structure and installation mode, as well as their competitive relationship with conventional grid-connected inverters, there are many challenges in the design of microinverters (Hasan et al., 2017; Çelik et al., 2018; Premkumar et al., 2018; Rojas et al., 2021). There are three main drawbacks of microinverters. In terms of stability and service life, since microinverters are exposed to harsh operating environments caused by their special installation methods, microinverters need more stable software and hardware foundations. Since the lifespan of photovoltaic modules is usually more than 25 years, to match the lifespan of microinverters with that of photovoltaic modules, such a long service life brings great challenges to the design of microinverters. Apart from that, compared with those of conventional centralized or string inverters, the conversion efficiency of microinverters is lower. In addition to the MPPT control algorithm, the energy utilization rate of photovoltaic modules also affects the conversion efficiency. Finally, current microinverters are high in cost. The AC module system is equipped with a microinverter for each photovoltaic module, which means that compared with centralized or

string inverters equipped with multiple photovoltaic modules, the use of microinverters is more expensive.

Therefore, in this research, an improved low-budget topology of photovoltaic grid-connected microinverters and a new control strategy should be researched to improve the lifespan, efficiency, and cost. The control strategy may focus on a novel method to improve the effectiveness of the system.

1.4 Research Hypothesis

- i. A few types of modifications can enhance the performance of microinverters. These modifications include adding a compensation capacitor, adopting the Inductor-Capacitor-Diode (LCD) passive clamping technology, and introducing an interleaved parallel flyback topology. These improvements can reduce switching losses, eliminate the spike voltage by about 10%, reduce THD values by about 0.9%, and reduce hardware costs.
- ii. Considering various parasitic parameters, including transformer leakage inductance, parasitic capacitance of the MOSFET, and parasitic capacitance of the rectifier diode, modal analysis and calculation can generate a peak current reference curve that aligns with practical engineering conditions. By integrating a multi-valley turn-on control strategy, precise control of the MOSFET's on-off state can be achieved, thereby reducing circuit losses and

harmonic content. The maximum power efficiency can reach over 97%, with a THD value below 3%.

- iii. The constructed experimental prototype and platform can obtain data such as efficiency, THD value, and current waveform using equipment like a power analyser, oscilloscope, and grid simulator. Through comparison, the effectiveness and reliability of the proposed topology and control strategy can be verified.

1.5 Objectives

This research focuses on the novel control strategy and improved topology of photovoltaic grid-connected microinverters. This research mainly studies the following two key technologies and an experimental platform.

- i. To design a topology structure of an interleaved parallel microinverter with compensation capacitors using passive clamping technology to achieve a smoother grid-connected current while reducing costs;
- ii. To model a control strategy based on an accurate peak current reference curve and the multi-valley turn-on method to achieve higher efficiency and lower THD values;
- iii. To develop an experimental flyback microinverter platform comprising hardware and software, and evaluate the performance of the proposed topology structure and control strategy.

1.6 Scope of Study

The scope of this research is to develop a topology structure and control strategy for microinverters operating in Discontinuous Conduction Mode (DCM). The detailed scopes of the study are as follows:

- i. To study and understand methods for designing an effective and efficient flyback topology of microinverters.
- ii. To study and design control strategies for microinverters operating in DCM with the aim of reducing the voltage stress on transistors and improving efficiency to over 97%.
- iii. Using PSIM simulation software and the constructed experimental platform, to simulate and experiment the topology structure based on the proposed multi-valley turn-on control strategy and fixed-frequency control strategy.
- iv. A comparative study is conducted on the performance of the topology structures and control strategies, verifying that in this research, the resonant period of this research is significantly extended, voltage spikes are suppressed, the number of components is reduced, harmonic content is lowered, and efficiency is improved.
- v. To develop and construct an experimental prototype of microinverters based on the topology proposed in this research using Printed Circuit Board (PCB)

construction techniques. The prototype should allow for modifications and programming of the control strategies. Combined with equipment such as a power analyser, photovoltaic simulator, and grid simulator provided by the experimental platform, it can complete all necessary experiments for validation.

- vi. By comparing current and voltage waveforms, analysing line charts of power loss, efficiency, and THD, as well as using tabular comparisons, to evaluate and compare the results obtained from the simulation and experimental works that have been carried out.

1.7 Significant Contributions

In this research, the low-cost topology structure and high-efficiency control strategy of a microinverter are analysed and studied in depth to improve the development of distributed low-power photovoltaic grid-connected microinverters.

- i. By improving an interleaved parallel passive clamping flyback topology with a compensation capacitor, the oscillation period is extended, the switching frequency of the switch tube is reduced, and the passive clamping technique is introduced to eliminate the spike voltage of the switch tube, thereby reducing switch losses, improving inverter conversion efficiency, and lowering hardware costs.

- ii. A novel multi-valley turn-on control strategy is proposed to accurately determine the switching of transistors under actual engineering conditions, achieve multi-valley turn-on, reduce circuit losses, and minimize harmonic content.

1.8 Chapter Summary

This thesis is organized into five chapters. A brief outline of the contents of the thesis is as follows:

Chapter 1 presents an introduction of the research problem. It comprises the research background and problem statement. In addition, the research objectives, scopes and contributions are highlighted and elaborated. The structure and the flow of the thesis are also outlined in this chapter.

Chapter 2 describes the current research overview and reviews related works on flyback microinverters. The topologies of the main circuit and photovoltaic grid-connected control strategies are highlighted. The gaps between earlier studies and the proposed topologies and control strategies are recognized and discussed.

Chapter 3 focuses on the construction and development process of the photovoltaic grid-connected microinverter proposed in this research. The basic topology structure and improved structure were constructed, and simulation parameters were determined. The algorithms in the control strategy are introduced. In addition, the software and hardware involved in the experimental platform are explained.

Chapter 4 highlights the improved topology circuit and the novel control strategy. Based on the research on key technologies, this chapter provides a detailed introduction to the specific implementation of the system. The effectiveness and stability of the developed system are verified through experimental analysis.

Chapter 5 provides a summary, draws conclusions from the entire study, describes the key findings, and proposes future research directions in the field.

The structural organization of the thesis is shown in Figure 1.6.

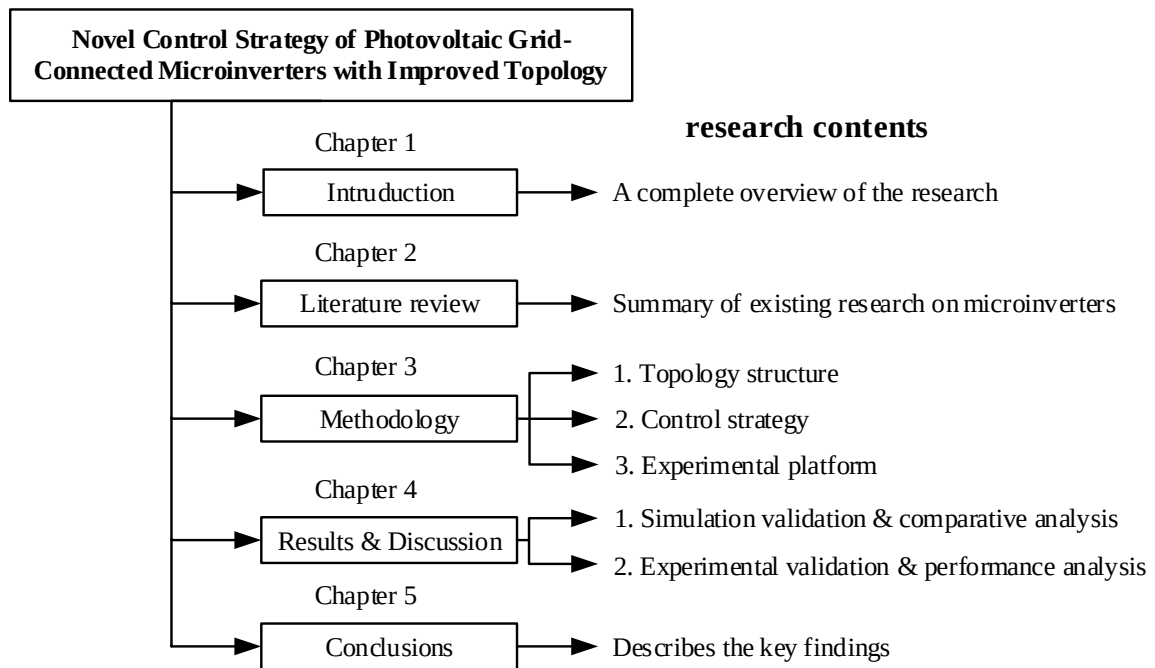


Figure 1.6: Organization of the Content of This Thesis

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

The focus of this research is to achieve high reliability, long life, high efficiency and low cost flyback microinverter. Therefore, this literature review focuses on two important parts of microinverters. The first part summarizes the research status of the topology of the main circuit in the inverter, focusing on the topology structure of the flyback inverter and the clamping technology. In the second section, the current flyback topology control strategy is emphasized. At the end of this chapter, the existing gaps in the current research are summarized, and suggestions for improvement are presented.

2.2 Microinverter Topology

The topology of the grid-connected inverter is the basis of the entire system. Choosing a reasonable inverter topology can not only improve the conversion efficiency of the system and reduce production costs but also help ensure the economical and reliable operation of the system. It is highly important to guide the development of the photovoltaic industry and improve its competitiveness.

2.2.1 Classification of Microinverters

Focusing on standards such as conversion efficiency, power density, reliability, and economy, scholars have successively proposed a series of circuit topologies suitable for

microinverters. According to the location and structural characteristics of the DC link, these topologies can be divided into three categories (Taghvaei et al., 2013; Bhattacharya et al., 2019; Zhang, 2020; Guo et al., 2021).

- i. Microinverter with DC-link;
- ii. Microinverter without DC-link;
- iii. Microinverter with pseudo-DC-link.

2.2.1.1 Microinverter with DC-link

The DC-link structure is shown in Figure 2.1. This type of circuit topology usually uses a DC-DC converter to realize the MPPT function. On the other hand, the lower photovoltaic module voltage is raised to the DC link voltage required by the grid-connected inverter. Then, the power quality of the grid-connected current is controlled using a DC-AC converter (Ahmed et al., 2013; Paul et al., 2023b).

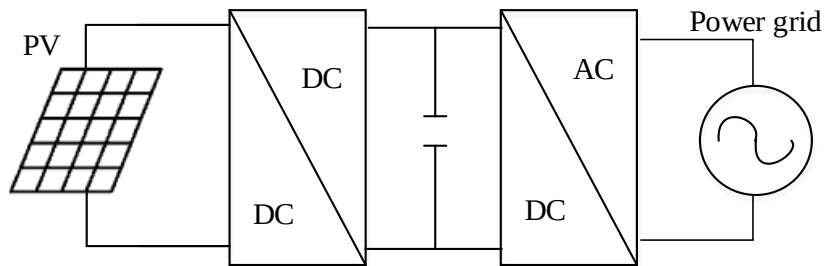
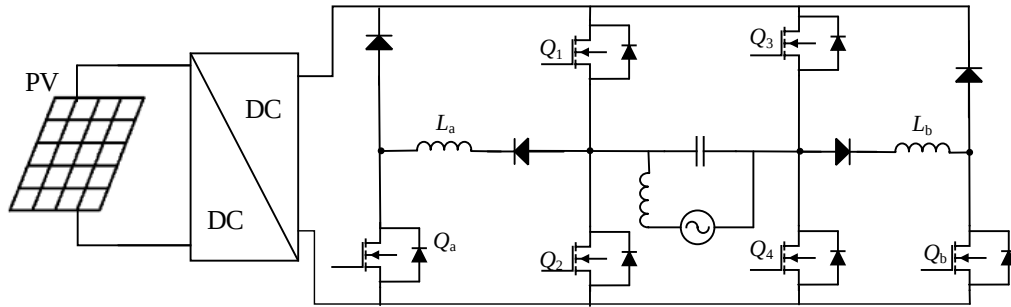


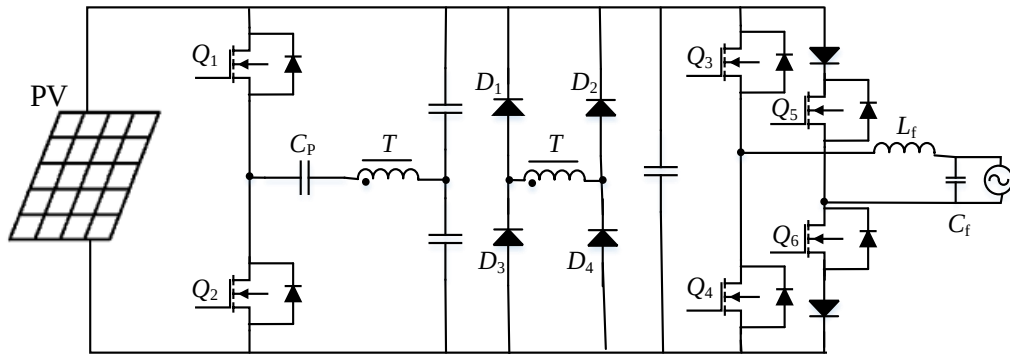
Figure 2.1: Structure with DC-Link

Figure 2.2 shows four microinverter circuit topologies based on the DC link structure, among which Figure 2.2 (a) applies soft switching technology to a full-bridge DC-AC converter (Andersen & Alvsten, 1995; Paul et al., 2023a). There is no innovation in the

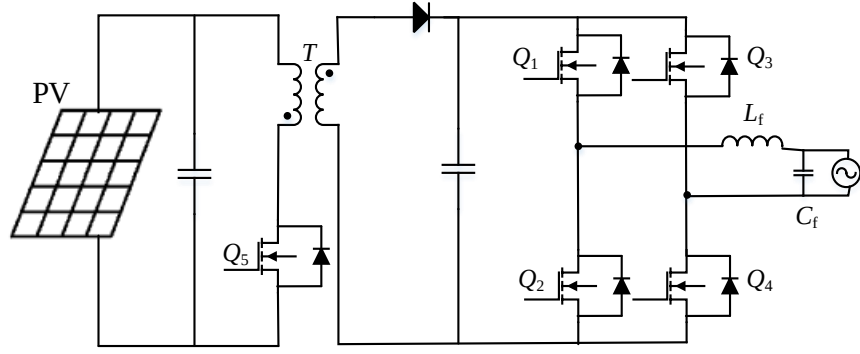
converter, so the detailed structure of the topology is not given. The DC-DC stage in Figure 2.2 (b) uses a series resonant half-bridge converter, and two additional diodes are added to the DC-AC stage to constitute an improved full-bridge inverter based on the full-bridge topology (Lohner et al., 1996; Wei et al., 2018). The DC-DC stage in Figure 2.2 (c) is a flyback converter, and the DC-AC stage uses a current-controlled full-bridge Pulse-Width Modulation (PWM) inverter circuit (Martins & Demonti, 2000; Ghavipankeh Marangalu et al., 2021); Figure 2.2 (d) uses a soft-switching dual-inductor boost converter as the DC-DC stage, and the DC-AC stage also uses a current-controlled full-bridge PWM inverter circuit (Wolfs & Li, 2002; Ramadhan et al., 2023).



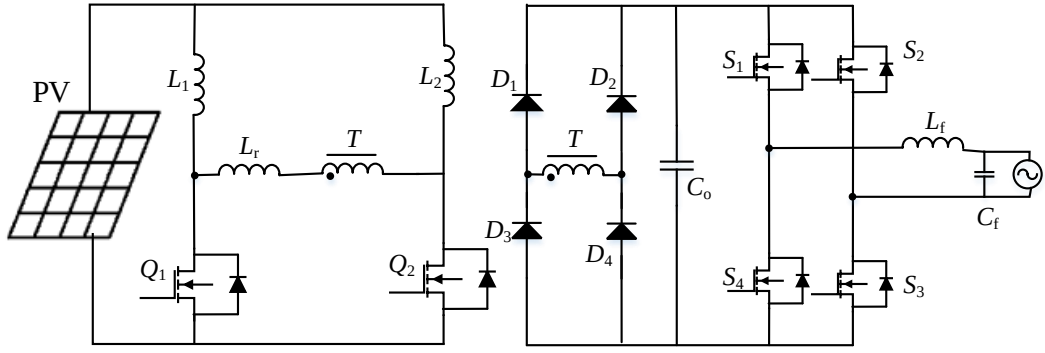
(a)



(b)



(c)



(d)

Figure 2.2: Topologies with DC-Link

Table 2.1 lists the main parameters of these four circuit topologies. The topology shown in Figure 2.2 (c) contains the least number of components, which contributes to the cost reduction and reliability of microinverters. However, it adopts a hard-switching strategy, and it is difficult to obtain an ideal conversion efficiency. The topologies in Figure 2.2 (a), (b) and (d) all use soft switching technology, which reduces switching loss and improves conversion efficiency, but the number of components is large. Moreover, power switching devices are subjected to relatively large voltage and current stresses.

Table 2.1: Comparison of Microinverters with DC-Link

Topology	Rated Power (W)	ElementNum				Maximum Efficiency	PCB Area (mm ²)
		Transistor	Diode	Magnetic Core	Winding		
Figure 2.2 (a)	200	>6	>4	>2	>2	96%	100* 480
Figure 2.2 (b)	250	6	6	1	2	-	-
Figure 2.2 (c)	100	5	1	1	2	-	-
Figure 2.2 (d)	100	5	4	4	5	90%	-

In general, the topology with a DC-link has two disadvantages: first, the voltage stress on the switching devices in the DC/DC circuit is high, leading to significant switching losses. Second, the DC/AC stage operates in high-frequency PWM mode, which also causes large switching losses, and the reverse recovery problem of the diodes is severe, resulting in lower overall efficiency of the inverter. To address these two issues, soft-switching technology can be applied to both stages of the circuit. However, this inevitably leads to further circuit complexity and additional cost, while the system reliability may decrease. Moreover, grid current control is relatively complex, which raises higher requirements for the controller, further increasing the cost of the inverter. From the perspective of power decoupling, decoupling capacitors are often connected in parallel with the DC-link. Due to the high voltage of the DC-link, the size of the decoupling capacitors can be reduced.

2.2.1.2 Microinverter without DC-Link

The structure without a DC-link is shown in Figure 2.3.

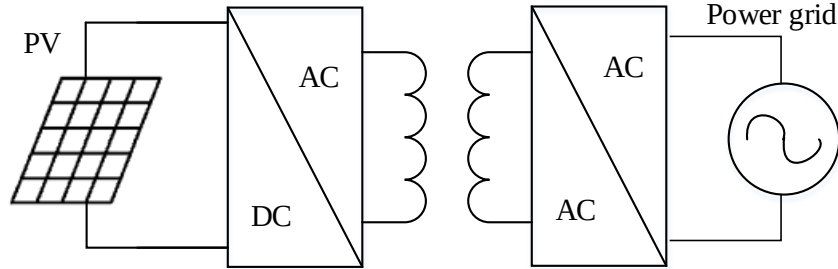


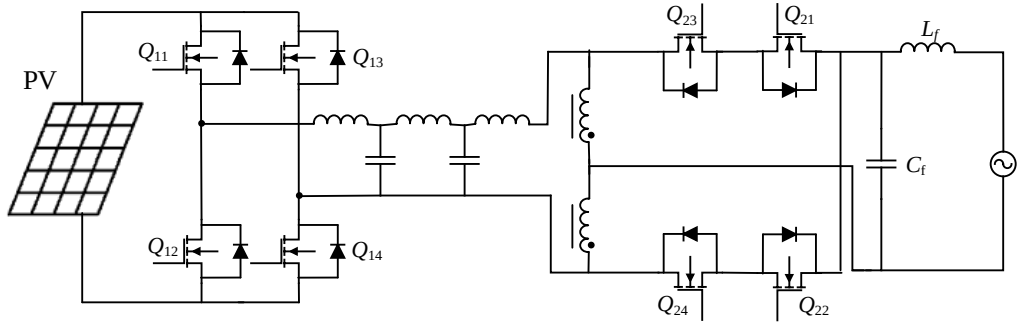
Figure 2.3: Structure without DC-Link

This type of inverter circuit usually uses a DC-AC converter to modulate the voltage of the photovoltaic module into a high-frequency AC square wave voltage firstly and then boosts it through a high-frequency transformer. Finally, the high-frequency AC square wave voltage is modulated into a power frequency AC sinusoidal voltage by a frequency converter (Goetz et al., 2019; Wu et al., 2020).

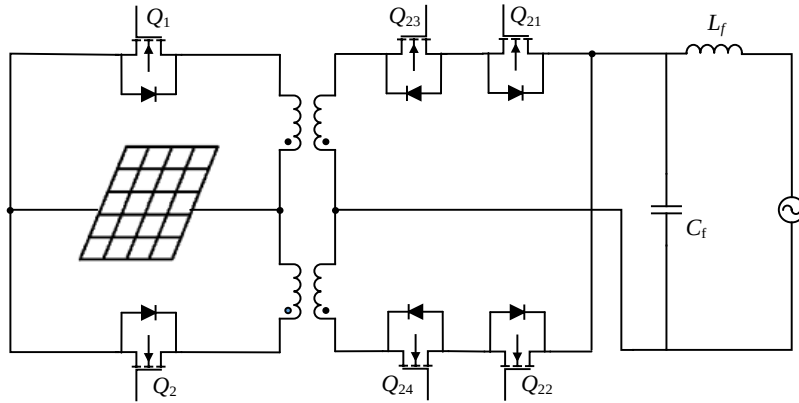
Figure 2.4 illustrates three topologies of microinverter circuits without a DC link. Figure 2.4 (a) uses an H-bridge inverter circuit to modulate the DC voltage into a high-frequency AC voltage, modulates the high-frequency AC voltage to a current source through impedance-conductance conversion, and finally modulates the high-frequency current to a power frequency current using a forced-phase commutation AC-AC converter (Yatsuki et al., 2001; Aamara et al., 2023; Jamatia & Sensarma, 2023b). Figure 2.4 (b) uses a push-pull circuit to modulate the DC voltage into a high-frequency AC voltage and then modulates the high-frequency voltage directly into an industrial-frequency voltage by a forced-phase commutation AC-AC converter (De Souza et al., 2002; Zhang, 2023). Figure 2.4 (c) uses a

dual-inductor boost converter to modulate the DC voltage to a high-frequency voltage AC current, and then the high-frequency AC current is modulated to a power frequency AC voltage by a matrix converter (Li & Wolfs, 2008; Qi et al., 2023).

The highlight of the topology shown in Figure 2.4 (c) is the use of a nonpolarizing capacitor at the load side to achieve power balancing, eliminating the coupling electrolytic capacitors normally present at the input of the converter. However, in practical applications, it is usually necessary to add an additional diode in series with the switch tube on the primary side of the transformer to solve the problem of negative drain-source voltage caused by the bidirectional flow of power.



(a)



(b)

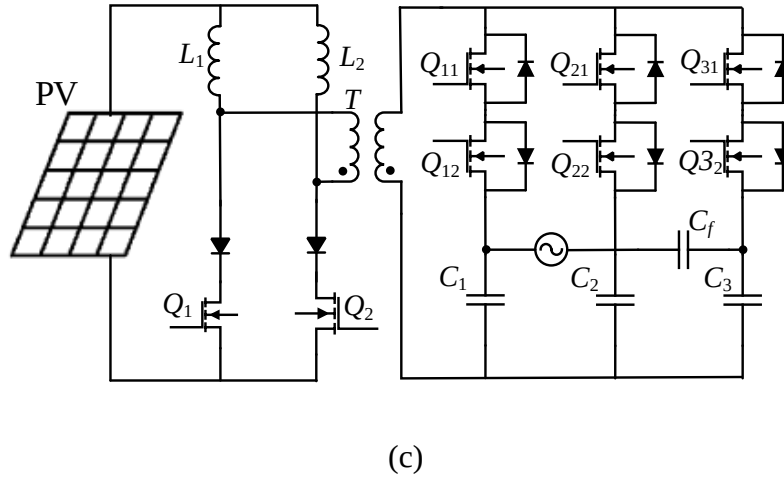


Figure 2.4: Topologies without DC-Link

The main parameters of these three circuit topologies are listed in Table 2.2.

Table 2.2: Comparison of Microinverters without DC-Link

Topology	Rated Power (W)	ElementNum				PCB Area (mm ²)
		Transistor	Diode	Magnetic Core	Winding	
Figure 2.4 (a)	300	8	0	4	5	100* 480
Figure 2.4 (b)	300	6	0	1	4	-
Figure 2.4 (c)	100	8	2	3	4	-

In inverter circuits without a DC-link structure, the cycloconverter uses bidirectional switches, which increases the number of components. Additionally, the cycloconverter forcibly interrupts the power flow at high frequencies, causing overshoot in the secondary voltage and increasing the voltage stress on the components.

2.2.1.3 Microinverter with Pseudo DC Link

Figure 2.5 shows the pseudo DC-link structure, including the DC-DC converter and DC-AC circuit with power frequency commutation. The DC-DC converter modulates the voltage of the photovoltaic module into a DC sinusoidal full-wave voltage and then modulates the DC sinusoidal full-wave voltage into an AC sinusoidal voltage through a power frequency commutation DC-AC circuit (Trujillo et al., 2016; Jaber & Shakir, 2021).

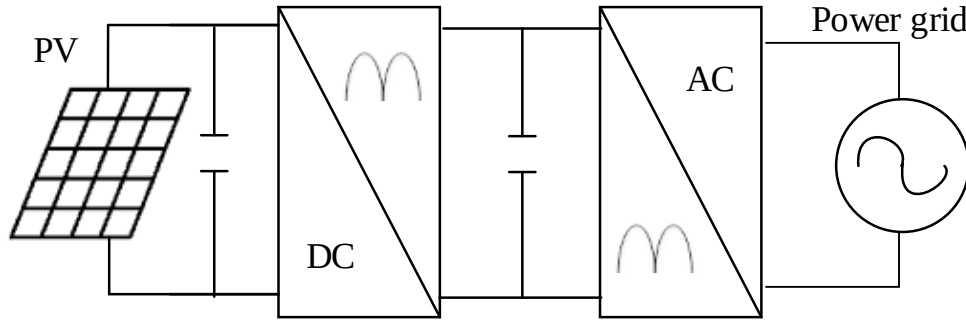
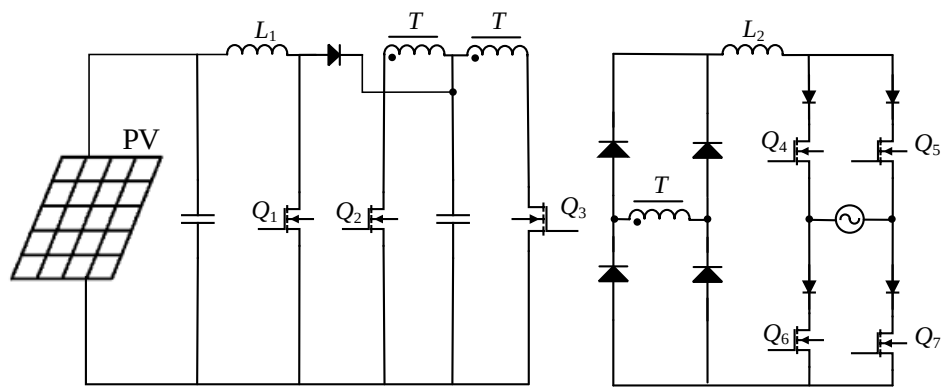
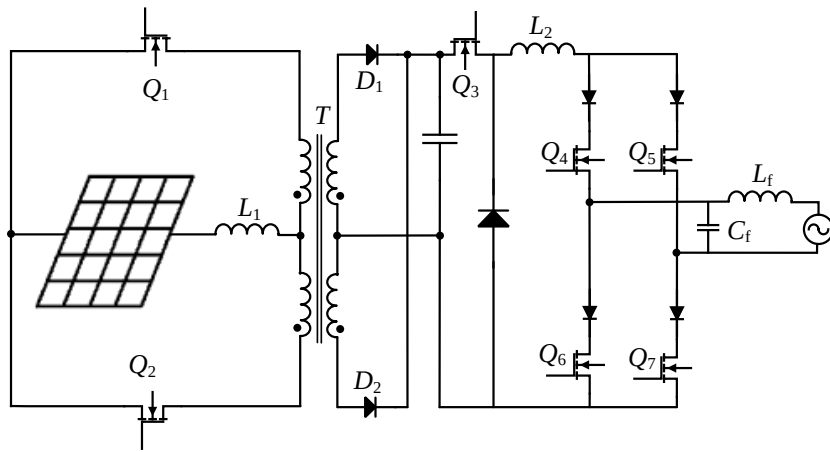


Figure 2.5: Structure with Pseudo DC-Link

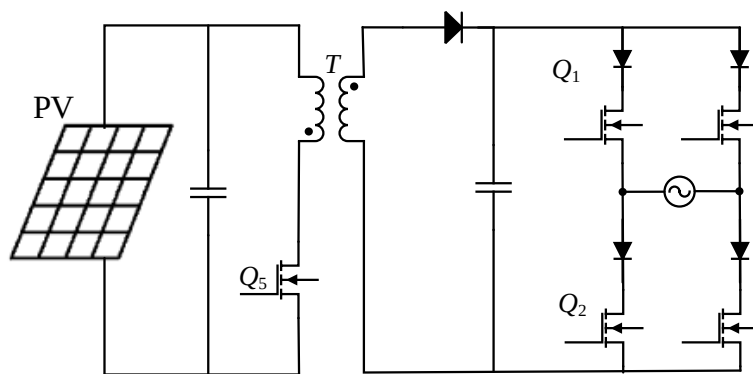
Figure 2.6 shows five topologies with pseudo DC-link, among which Figure 2.6 (a) firstly uses a boost converter to boost the input voltage and then uses a push-pull circuit to generate a DC sinusoidal full-wave current. Finally, the DC sinusoidal full wave is transformed into an AC sinusoidal wave by a power frequency commutation circuit (Herrmann et al., 1993; Paul et al., 2023). Figure 2.6 (b) uses a push-pull circuit to increase the input voltage, a buck converter to modulate a DC sinusoidal full wave, and finally an AC sinusoidal wave to be generated through a power frequency commutation circuit (Martins & Demonti, 2000; Ghribi et al., 2023).



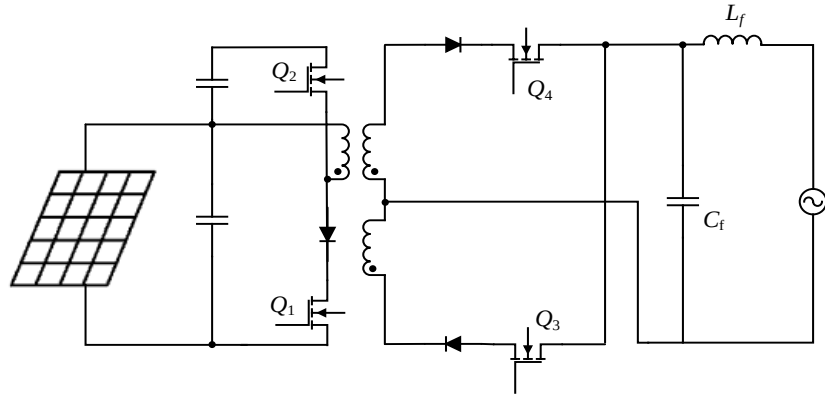
(a)



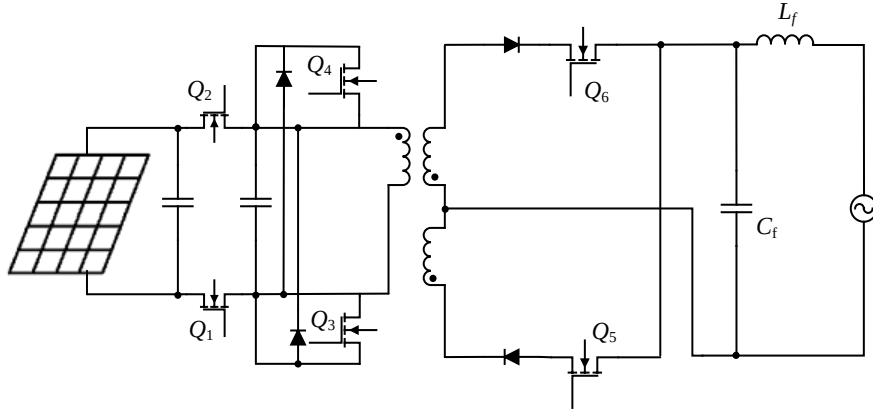
(b)



(c)



(d)



(e)

Figure 2.6: Topologies with Pseudo DC-Link

Figure 2.6 (c) uses a flyback converter to modulate a DC sinusoidal full wave and then generates an AC sinusoidal wave through a power frequency commutation circuit (Achille et al., 2004; Lin et al., 2024). This topology is similar to the DC link shown in Figure 2.2 (c), but the control strategy is completely different. The topology in Figure 2.6 (d) is essentially a combination of a buck-boost converter and a flyback converter. The energy is firstly transferred to the excitation inductance of the transformer through the switch tube of the buck-boost converter, then transferred to the intermediate capacitor through the switch tube

of the flyback converter, and finally injected into the grid through the center-tapped transformer and the two switches on the secondary side (Shimizu et al., 2006; Afshari et al., 2023; Jamatia & Sensarma, 2023a). The topology in Figure 2.6 (e) is an improvement of the topology shown in Figure 2.6 (d), adding the function of recovering the leakage inductance energy of the flyback transformer, which improves the conversion efficiency to a certain extent (Zhang et al., 2021; Pan et al., 2024). The main parameters of these five circuit topologies are shown in Table 2.3.

Table 2.3: Comparison of Microinverters with Pseudo DC-link

Topology	Rated Power (W)	ElementNum				Maximum Efficiency	PCB Area (mm ²)
		Transistor	Diode	Magnetic Core	Winding		
Figure 2.6 (a)	350	7	9	3	5	90%	100* 480
Figure 2.6 (b)	300	7	7	3	6	80%	-
Figure 2.6 (c)	150	5	1	1	2	93%	-
Figure 2.6 (d)	100	4	3	1	3	-	-
Figure 2.6 (e)	160	6	4	1	3	87%	-

The pseudo DC-link structure using a grid frequency polarity reversal circuit simplifies the control complexity of the inverter and reduces the switching losses in the main circuit.

However, the DC/DC circuit in this configuration needs to achieve both boost and sinusoidal current modulation functions, so the choice of topology for the DC/DC circuit and its corresponding control strategy is currently a key focus of research.

In summary, Table 2.4 compares the three types of microinverter topologies.

Table 2.4: Comparison of Microinverters with Three Topological Structures

Classification of Topologies		Topology with DC-Link	Topology without DC-Link	Topology with Pseudo DC Link
Control Methods	DC/DC	Fixed Duty Cycle	Matrix Control	SPWM
	DC/AC	SPWM		Square Wave with Grid Frequency
Decoupling Capacitor	Location	DC-Link	Input Side	Input Side
	Type	Electrolytic Capacitor / Film Capacitor	Electrolytic Capacitor	Electrolytic Capacitor
	Power Density	High	Medium	Low
Advantages		Independent Control of Bipolar Circuits	Fewer Power Level Changes	Low DC/AC Losses
Disadvantages		High DC/AC Losses	Bidirectional Switch, Matrix Control	Complex DC/DC Control

For modular photovoltaic grid-connected systems with a rated power of around 200W/400W, the choice of microinverter topology should not only pursue higher efficiency but also consider circuit reliability and cost factors. Among the various topologies, the

flyback inverter with a pseudo DC-link structure has the advantages of a simple structure and fewer components, which has attracted widespread attention and research in both industry and academia.

2.2.2 Flyback Microinverter

2.2.2.1 Single-Ended Flyback Topology

The flyback inverter features a simple structure and uses fewer components. Various commercial microinverters based on the flyback inverter are reliable in performance and remain the mainstream solution in the industry. Research on flyback inverters in academia began in the early 21st century, and after years of development, significant progress has been made in circuit topology and control strategies. (Dileep & Singh, 2017; Zhang, 2020).

The advantages of the flyback topology for power electronics circuits are listed below (Omar et al., 2023):

- i. The high-frequency transformer can act as a filter, reducing the harmonics of the output waveform.
- ii. There is only need for a high-voltage diode, resulting in a simple driving circuit and fewer required components, leading to lower costs.
- iii. The magnetic core of the flyback transformer resets naturally, eliminating the need for reset winding. When the turns ratio of the transformer is chosen appropriately, it can adapt to a wide range of DC input voltages.

To minimize the number of power components, a microinverter circuit based on the flyback topology was proposed by Papanikolaou et al. (2003), as shown in Figure 2.7. The two low-frequency switches Q_1 and Q_2 on the secondary side of the transformer conduct during the positive and negative half-cycles of the grid voltage, respectively. The main switch Q on the primary side of the transformer operates in Discontinuous Conduction Mode (DCM) and controls the grid-connected current through the SPWM. This topology requires fewer components and has relatively simple control; however, its main drawback is the high current stress on the main switch in DCM, leading to higher switching losses. Additionally, due to the leakage inductance in practical transformers, the energy stored in the leakage inductance cannot be transferred to the secondary side of the transformer, thereby reducing the efficiency of the microinverter. Moreover, a transformer with a central tap has a complex winding configuration and a large volume (Zhang et al., 2022).

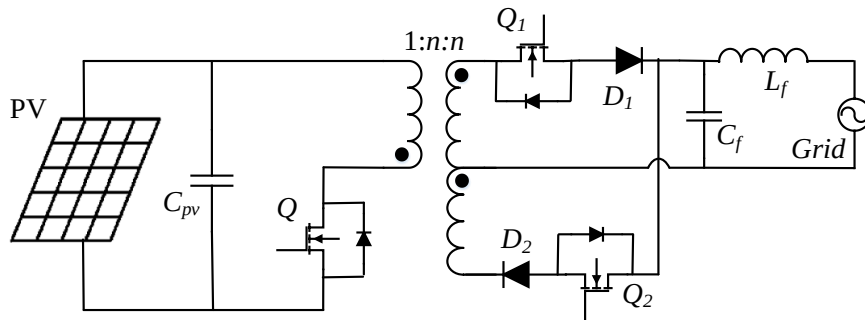


Figure 2.7: Flyback Topology 1

Then, a DC-AC circuit for grid frequency polarity conversion composed of four thyristors was proposed, as shown in Figure 2.8, to reduce the volume of the transformer (Achille et al., 2004; Cao et al., 2023).

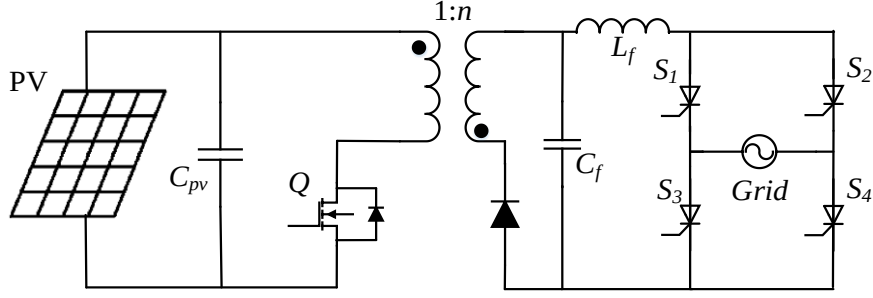


Figure 2.8: Flyback Topology 2

To address the drawback of high switching losses in conventional flyback microinverters, a soft-switching flyback inverter employing a variable frequency modulation method was proposed (Tian et al., 2010; Miao, 2022), as shown in Figure 2.9.

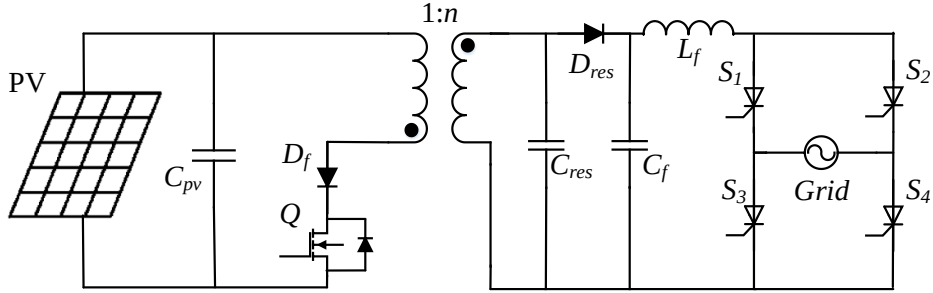


Figure 2.9: Flyback Topology 3

The main switch has a constant conduction time, and resonance is generated through the leakage inductance of the primary side and the secondary side capacitor C_{res} , achieving Zero Current Switching (ZCS) of the main switch Q . Meanwhile, the secondary side diode exhibits ZCS characteristics. The main drawback of this circuit is the high loss of diode D_f connected in series on the primary side. Additionally, due to the wide range of switching frequencies, it has some impact on the Total Harmonic Distortion (THD) of the grid-connected current.

2.2.2.2 Interleaved Parallel Flyback Topology

Usually, the flyback inverter is based on a single-end flyback topology circuit, which has the advantages of small size, simple structure, and wide voltage regulation range, and as such, it is widely used in low-power applications, such as circuit auxiliary power supplies. However, single-end flyback inverters also have various problems leading to their low efficiency, such as low circuit output power, which is generally used for power applications at approximately 100 W, and large ripple current, resulting in the use of large electrolytic capacitors for filtering, which easily affects the circuit working life (Tan et al., 2014; Kavathekar & Patil, 2020). It is necessary to make appropriate improvements to the single-end flyback topology structure to meet specific design requirements. Many scholars have conducted in-depth research on its topology structure. Among them, the interleaved parallel flyback topology is an improvement over the conventional flyback topology, which can effectively overcome the abovementioned shortcomings and is widely used in practical applications (Kasa & Iida, 2006; Shiroyama et al., 2007; Tao et al., 2008; Liu et al., 2011; Ji et al., 2014; Salihmuhsin, 2023). The topology of the interleaved flyback microinverter is shown in Figure 2.10.

The interleaved flyback topology is the parallel connection of the input and output sides of two independent single-ended flyback circuits. Usually, the parameters of these two independent circuits are completely the same, and the control strategies used are also the same. The only difference is that the control signals of the two circuits are staggered, so the implemented functions are completely the same. When photovoltaic cells of the same power

level and the same main switching frequency are used, the interleaved flyback circuit, compared with the single-ended flyback circuit, has an equivalent switching frequency that is twice that of the latter. The input–output ripple is smaller, and the volume of the input–output filter is also smaller. Meanwhile, any single-ended flyback circuit in the interleaved flyback circuit handles less power; therefore, the volume of the high-frequency transformer can also be smaller (Brindha et al., 2018; Thanikanti et al., 2021).

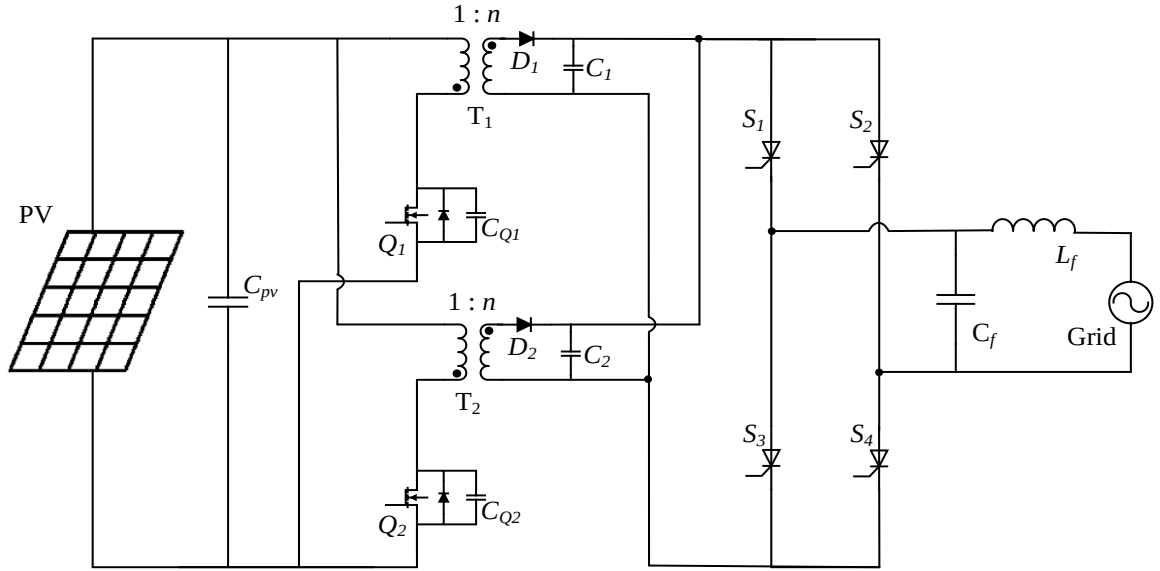


Figure 2.10: Typical Topology of the Interleaved Flyback Microinverter

Table 2.5 reviews the various methods for improving flyback topology circuits in the literature. The interleaved parallel flyback circuit is more suitable for the microinverter with a 400 W output power studied in this thesis. The issue of leakage inductance will be addressed in the subsequent section on clamping technology.

Table 2.5: Comparison of Flyback Topologies

Author	Methods	Main Findings	Drawbacks
Papanikolaou et al. (2003)	Secondary low-frequency switches and SPWM	It required fewer components and has relatively simple control.	High current stress on the main switch, leakage inductance, complex winding configuration and larger volume for the transformer.
Achille et al. (2004) Cao et al. (2023)	A grid frequency polarity conversion circuit with four thyristors	It reduced the volume of the transformer.	High current stress on the main switch, presence of leakage inductance.
Tian et al. (2010) Miao (2022)	A soft-switching flyback inverter	It achieved ZCS of the main switch and ZCS of the secondary diode.	High loss of the primary diode and wide range of switching frequency.
Salihmuhsin (2023) Ji et al. (2014)	Interleaved parallel flyback topology	Higher output power, lower ripple compared with the single-ended circuit.	Leakage inductance.

2.2.2.3 Clamping Technology

The implementation of a clamping soft switch is one of the key issues for interleaved flyback microinverters. Typically, the output power of a single photovoltaic module is approximately a few hundred watts, and the losses of the microinverter are relatively high

compared with the total system power. The leakage inductance of the flyback transformer is a major component of the total losses due to its air gap and winding process, and the losses caused by the leakage inductance are a significant part of the total losses. In addition to causing losses, the leakage inductance of the flyback transformer can also cause significant voltage stress on the main switch, which not only increases the electromagnetic interference of the system but also reduces the efficiency of the system. In severe cases, it can even damage switch devices, preventing the system from functioning properly (Rezaei et al., 2015; Zhang et al., 2019).

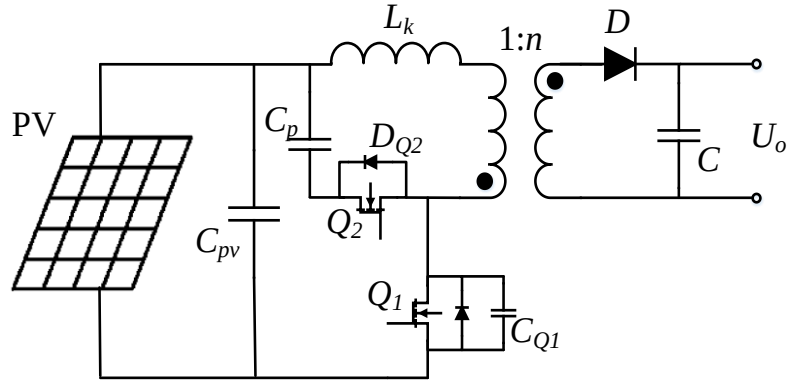
Currently, in dealing with the leakage energy of flyback transformers, namely, the clamping of leakage energy, there are two forms: active clamping and passive clamping (Kasa et al., 2005).

i. Active clamping

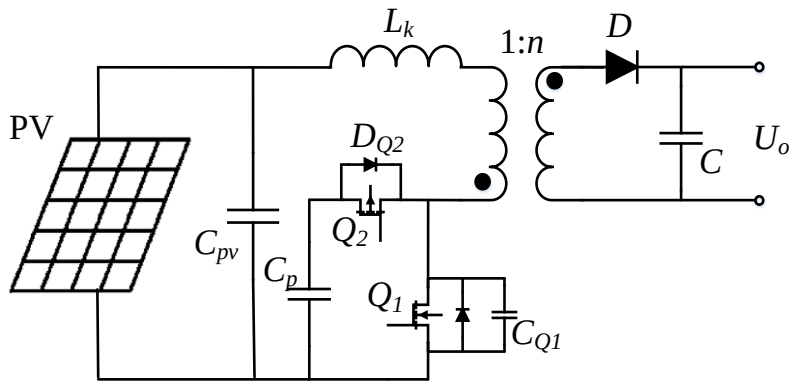
Active clamping circuits are classified into Negative Channel Metal Oxide Semiconductor (NMOS) active clamping circuits (Hsia et al., 2011; Ming et al., 2023) and Positive Channel Metal Oxide Semiconductor (PMOS) active clamping circuits (Han et al., 1999; Smith & Smedley, 1999; Huang et al., 2016) based on the position of the clamping capacitor. As shown in Figure 2.11, the clamping circuits consist of MOSFET Q_2 and clamping capacitor C_p . L_k is the leakage inductance of the flyback transformer.

Active clamping can achieve the recovery of leakage energy and suppress the turn-off voltage stress of the switch. Through proper control, soft switching of the main and

auxiliary switches can also be achieved (Dwari & Parsa, 2011). However, additional switch devices increase the cost, and the control algorithm is more complex than passive clamping, adding to the controller operational load, which is not widely used in engineering practice.



(a) Active Clamping Circuit with NMOS



(b) Active Clamping Circuits with PMOS

Figure 2.11: Active Clamping Circuit in Flyback Converters

ii. Passive clamping

Passive clamping circuits mainly include Resistor-Capacitor-Diode (RCD) clamping circuits (Huber et al., 2018), dual-transistor clamping circuits (Qin et al., 2024), and LCD

clamping circuits (Tao et al., 2008). Figure 2.12 shows a flyback microinverter with an RCD clamping circuit. When the main switch Q is turned off, its leakage source voltage is clamped by clamping capacitor C_p , and the leakage energy flows into the clamping circuit and is ultimately dissipated in clamping resistor R . This circuit has a simple topology and low cost; however, the leakage energy is consumed in the form of heat on resistor R , leading to a decrease in system efficiency (Li & He, 2007).

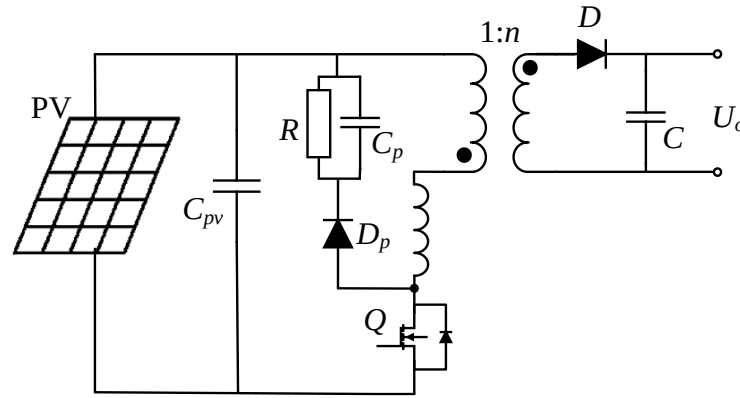


Figure 2.12: Passive Clamping Circuit with RCD

Figure 2.13 shows a flyback microinverter with a dual-transistor clamping circuit, which can reduce the voltage stress of the switch, ensuring that the voltage stress of each switch does not exceed U_{pv} , which is suitable for high-input voltage scenarios. At the same time, the energy of the transformer leakage is fed back into the grid without any leakage energy loss, resulting in higher system efficiency. However, this system requires a large number of devices, leading to higher costs (Zhao et al., 2022).

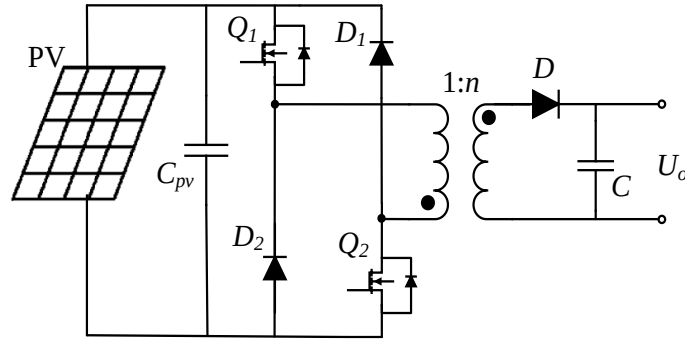


Figure 2.13: Passive Clamping Circuit with a Dual-Transistor

Figure 2.14 shows a flyback microinverter with an LCD clamping circuit, where no resistor is present, reducing the circuit losses (Wu & Wang, 2020). With the existence of the reset inductor L_b and snubber capacitor C_p , the circuit reabsorbs the leakage energy through LC resonance, thereby improving system efficiency (Watson et al., 1996; Moses & Banu, 2015).

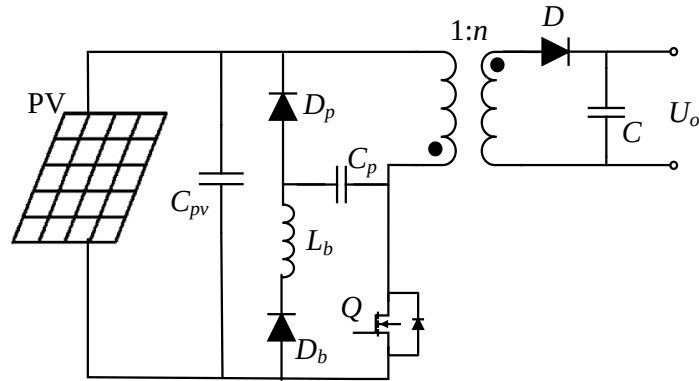


Figure 2.14: Passive Clamping Circuit with LCD

Table 2.6 summarizes the advantages and disadvantages of the five clamping techniques. The LCD passive clamping circuit can return the leakage energy of the transformer to the grid without any loss and requires fewer devices. Therefore, this research adopts this LCD passive clamping method.

Table 2.6: Comparison of Clamping Technologies

Clamp Forms	Clamping Methods	Author	Advantages	Disadvantages
Active Clamping	NMOS	Hsia et al. (2011) Ming et al. (2023)	It can achieve the recovery of leakage energy and suppress the turn-off voltage stress of the switch.	Due to the additional switch devices, it increases the cost and the control algorithm is more complex.
	PMOS	Huang et al. (2016)		
Passive Clamping	RCD	Li & He, (2007) Huber et al. (2018)	Simple topology and low cost.	The leakage energy is consumed on the resistor, leading to a decrease in system efficiency.
	Dual-transistor	Zhao et al. (2022) Qin et al. (2024)	It can return the leakage energy to the grid.	It requires a large number of devices, leading to higher costs.
	LCD	Tao et al. (2008) Wu & Wang (2020)	It can return the leakage energy to the grid, and requires fewer devices.	High switch conduction loss.

2.3 Flyback Topology Control Strategy

The key point of the control mode of the flyback inverter is the front-stage flyback circuit. The simplified circuit of the original circuit, omitting the grid frequency inverter bridge part, is shown in Figure 2.15 (Wu, 2020). Since the flyback circuit has a high-frequency switch, its frequency is much higher than the grid frequency, so the output voltage of the flyback circuit is a high-frequency DC sinusoidal waveform, and the flyback circuit can be analysed as a DC-DC circuit.

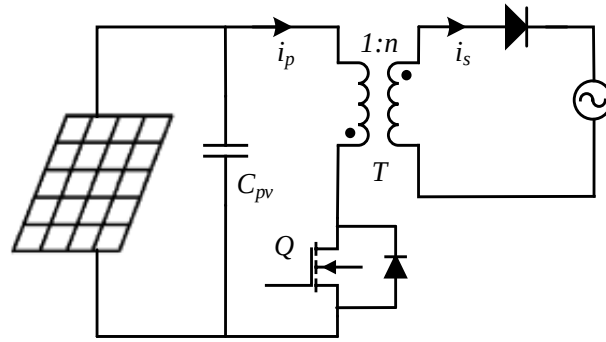


Figure 2.15: Simplified Diagram of the Flyback Conversion Topology

2.3.1 Classification of Operating Modes for Flyback inverters

Flyback inverters can operate in multiple different modes, and the rational selection of operating modes is an important step in inverter control strategy research. Flyback inverters can operate in three distinct modes: Discontinuous Conduction Mode (DCM), Boundary Conduction Mode (BCM), and Continuous Conduction Mode (CCM) (Chen et al., 2014; Gao et al., 2013; Pashaei et al., 2017).

As shown in Figure 2.15, the operation principle of the flyback inverter is to store energy in the primary inductance of the transformer during the uninterrupted on and off states of switch Q , and the energy in the inductance is released to maintain the normal operation of the inverter when the switch is turned off. Therefore, when the primary inductance of the transformer receives energy and generates a corresponding current on the secondary side, the degree of current decay can be used to determine the mode in which the inverter can operate. When the current decreases to zero precisely at the dead time of the switch, the inverter operates in DCM. When the current decreases to zero precisely at the beginning of the next switch cycle, the inverter operates in BCM mode. When the current does not decrease to zero and the next switch is triggered at the beginning, the flyback inverter operates in CCM (Lo et al., 2010; Shi & Mou, 2012).

2.3.1.1 Discontinuous Conduction Mode

The waveforms shown in Figure 2.16 depict the operation of the flyback inverter in the DCM (Wang et al., 2017; Gao, 2020). To better analyse the operating principle, the following assumptions are made:

- i. The switching frequency of the main transistor Q is much higher than the grid voltage frequency, and the grid voltage U_{gp} is constant within one switching cycle;
- ii. The decoupling capacitor C_{pv} on the DC side is sufficiently large, and the photovoltaic module output voltage U_{pv} is constant throughout the grid cycle;

iii. Energy losses within each switching cycle are ignored.

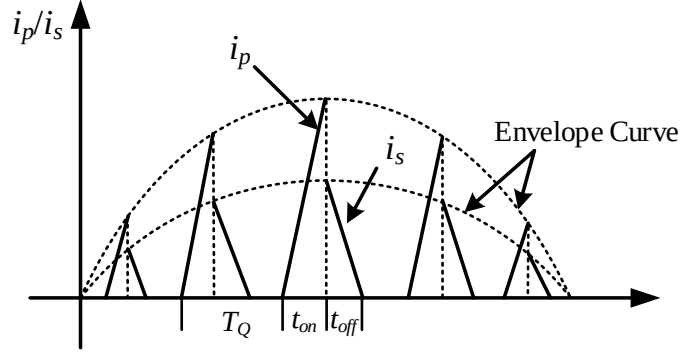


Figure 2.16: Primary and Secondary Current Waveforms in DCM

T_Q is the switch period of the main switch Q of the flyback inverter, t_{on} is the turn-on time, and t_{off} is the turn-off time. Therefore, in the DCM, $t_{on} + t_{off} < T_Q$. When the primary side switch Q is on, the primary current of the transformer starts to rise rapidly from zero until the end of the switch conduction time. At this time, the primary current reaches its peak value $i_{p.max}$, which is expressed by the following formula:

$$i_{p.max}(\theta_g) = \frac{U_{pv}}{L_p} t_{on}(\theta_g) \quad \text{Equation 2.1}$$

where θ_g is the phase angle of the grid voltage, U_{pv} is the input voltage of the photovoltaic module, and L_p is the primary inductance of the transformer.

After the main switch Q of the primary side turns off, the energy generated by the primary winding of the transformer quickly transfers to the secondary winding. At this point, the secondary current begins to decrease from its peak value $i_{s.max}$ until it reaches zero. Under ideal conditions, the grid voltage u_{gp} can be expressed as:

$$u_{gp}(\theta_g) = \sqrt{2}U_{rms}\sin(\theta_g) \quad \text{Equation 2.2}$$

where U_{rms} is the effective value of the grid voltage.

According to the volt-second balance theorem, the time required for the secondary side diode current to drop to zero can be represented as t_{off} :

$$t_{off}(\theta_g) = \frac{n \cdot U_{pv}}{u_{gp}(\theta_g)} t_{on}(\theta_g) = \frac{n \cdot U_{pv}}{\sqrt{2}U_{rms}\sin(\theta_g)} t_{on}(\theta_g) \quad \text{Equation 2.3}$$

where n is the turn ratio of the transformer secondary winding to the primary winding.

Based on Equation 2.1 and Equation 2.3, the average value of the secondary current in one switching cycle can be represented as:

$$i_{s.avg}(\theta_g) = \frac{1}{2} \frac{i_{p.max}(\theta_g)}{n} \frac{t_{off}(\theta_g)}{T_Q} = \frac{U_{pv}^2}{2\sqrt{2}L_p T_Q U_{rms}\sin(\theta_g)} t_{on}^2(\theta_g) \quad \text{Equation 2.4}$$

Equation 2.4 shows that to modulate the output current of the inverter sinusoidally, it is only necessary to control the conduction time t_{on} of the main switch Q to follow the sinusoidal variation in the grid voltage phase angle. Therefore, the duty cycle d_{DCM} of the main switch Q at this time can be represented as:

$$d_{DCM}(\theta_g) = \frac{t_{on}(\theta_g)}{T_Q} D_{max}\sin(\theta_g) \quad \text{Equation 2.5}$$

where D_{max} is the maximum duty cycle of the main Q within half a grid frequency cycle. By adjusting the value of D_{max} , the grid-connected current output by the inverter can be controlled. Substituting Equation 2.5 into Equation 2.4 yields:

$$i_{s.avg}(\theta_g) = \frac{T_Q U_{pv}^2 D_{max}^2}{2\sqrt{2} L_p U_{rms}} \sin(\theta_g) \quad \text{Equation 2.6}$$

From another perspective, if the peak function of the primary current is expressed in terms of the average value of the current transferred to the secondary side of the transformer, Equation 2.6 can be represented as:

$$i_{s.avg}(\theta_g) = \frac{1}{2} \frac{i_{p.max}(\theta_g)}{n} \frac{t_{off}(\theta_g)}{T_Q} = \frac{L_p}{2\sqrt{2} T_Q U_{rms} \sin(\theta_g)} [i_{p.max}(\theta_g)]^2 \quad \text{Equation 2.7}$$

According to the above equation, there is a close relationship between the peak current on the primary side of the transformer and the average current on the secondary side. By employing a Phase-Locked Loop (PLL) algorithm to generate a signal in phase and frequency with the grid voltage and then analysing it through DSP to produce Sinusoidal Pulse Width Modulation (SPWM) signals for the main switch, the transformer primary side can generate a DC half-envelope sinusoidal waveform and sinusoidal grid-connected currents. At this point, the peak current on the primary side of the transformer can be expressed as

$$i_{p.max}(\theta_g) = I_p \cdot \sin(\theta_g) \quad \text{Equation 2.8}$$

where I_p is the peak current of the primary side over half of the grid cycle. Substituting Equation 2.8 into Equation 2.7 yields:

$$i_{s.avg}(\theta_g) = \frac{1}{2} \frac{i_{p.max}(\theta_g)}{n} \frac{t_{off}(\theta_g)}{T_Q} = \frac{L_p I_p^2}{2\sqrt{2} T_Q U_{rms}} \sin(\theta_g) \quad \text{Equation 2.9}$$

According to the above equation, the grid-connected current can be controlled by controlling I_p . Therefore, if the inverter operates in the DCM, the control becomes much

simpler. In addition, the switches on the primary side can be opened again to store primary energy when the current stored in the secondary inductance of the transformer is completely depleted, allowing sufficient time for primary energy storage within the switching cycle, thus achieving complete demagnetization of the transformer within the switching cycle (Li & Wolfs, 2008). Because it operates in the DCM, the primary current generated by the primary winding starts from zero and increases in each switching cycle, thus avoiding excessive losses in the Q switch (Gorji et al., 2019).

2.3.1.2 Continuous Conduction Mode

Figure 2.17 shows the current waveforms of the primary and secondary sides when the flyback inverter operates in CCM (Hu et al., 2023).

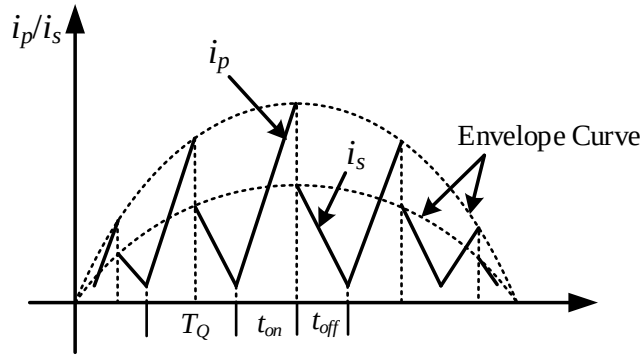


Figure 2.17: Primary and Secondary Current Waveforms in CCM

Within one switching cycle, when the switch is on, the primary excitation inductance starts to store energy, and the current gradually increases linearly. When the switch is turned off, the stored energy on the primary side is transferred to the secondary side, generating a continuously decreasing linear current. Since the switching cycle is short, the energy in the

primary winding is not fully consumed when the main switch is turned on again, causing the secondary side to store energy and generate current before the energy is completely discharged (Li & Oruganti, 2011; Neshaastegaran & Karshenas, 2013). Therefore, according to the volt-second balance theorem:

$$U_{pv}t_{on}(\theta_g) = \frac{\sqrt{2}U_{rms}\sin(\theta_g)}{n}t_{off}(\theta_g) \quad \text{Equation 2.10}$$

The duty cycle of switch Q in CCM can be derived as follows:

$$d_{CCM}(\theta_g) = \frac{t_{on}(\theta_g)}{t_{on}(\theta_g) + t_{off}(\theta_g)} = \frac{\sqrt{2}U_{rms}\sin(\theta_g)}{nU_{pv} + \sqrt{2}U_{rms}\sin(\theta_g)} \quad \text{Equation 2.11}$$

Assuming a unity power factor, the energy consumption of the inverter in the CCM is ignored; then, the output power of the inverter is equal to its input power. Thus:

$$i_{p.avg}(\theta_g)U_{pv} = u_{gp}(\theta_g) \cdot i_{gp}(\theta_g) = 2U_{rms}I_{rms}\sin^2(\theta_g) \quad \text{Equation 2.12}$$

where $i_{p.avg}(\theta_g)$ is the average value of the input current on the primary side, $u_{gp}(\theta_g)$ and $i_{gp}(\theta_g)$ represent the instantaneous values of the grid voltage and grid-connected current, respectively. The relationships between the various currents can be inferred from Figure 2.17:

$$\begin{cases} \frac{i_{p.max}(\theta_g) + i_{p.min}(\theta_g)}{2} \cdot \frac{t_{on}(\theta_g)}{T_Q} = i_{p.avg}(\theta_g) \\ i_{p.max}(\theta_g) - i_{p.min}(\theta_g) = \frac{U_{pv}t_{on}(\theta_g)}{L_p} \end{cases} \quad \text{Equation 2.13}$$

By substituting Equation 2.11 and Equation 2.10 into Equation 2.13, the peak current of the inverter primary inductance can be calculated:

$$i_{p.max}(\theta_g) = i_{s.avg}(\theta_g) \left[n + \frac{\sqrt{2}U_{rms}\sin(\theta_g)}{U_{pv}} \right] + \frac{U_{pv}T_Q}{L_p} \cdot \frac{\sqrt{2}U_{rms}\sin(\theta_g)}{nU_{pv} + \sqrt{2}U_{rms}\sin(\theta_g)}$$

Equation 2.14

According to the above equations, when the inverter operates in CCM, it cannot achieve the same consistency as in DCM in terms of achieving sinusoidal waveform output on the AC grid side through control of the switch duty cycle or the peak current of the primary side. In addition, when the output power injected into the grid is constant, the volume of the designed transformer will increase due to the increase in the excitation inductance, and issues such as reverse recovery of AC side diodes will arise, ultimately leading to significant losses during switch-off (Priewasser et al., 2013).

2.3.1.3 Boundary Conduction Mode

Figure 2.18 shows the current waveforms of the inverter operating in BCM (Lai et al., 2012). The difference between the BCM and DCM is that switch Q immediately turns on after energy is stored on the primary side of the transformer and released on the secondary side (Juang et al., 2012; Ansari et al., 2017).

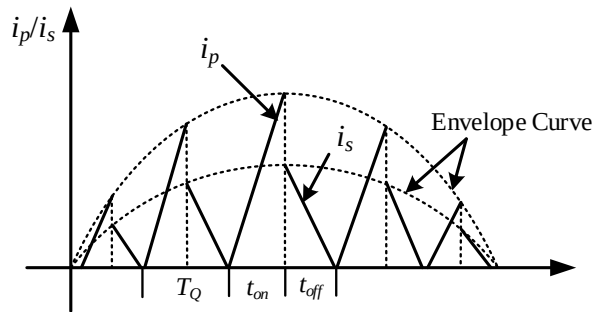


Figure 2.18: Primary and Secondary Current Waveforms in BCM

As the switch is continuously conducting at this time, the duty cycle in the BCM is the same as that in the CCM, namely:

$$d_{BCM}(\theta_g) = \frac{\sqrt{2}U_{rms}\sin(\theta_g)}{nU_{pv} + \sqrt{2}U_{rms}\sin(\theta_g)} \quad \text{Equation 2.15}$$

When operating in the BCM under ideal conditions, if the primary current of the transformer still exhibits a sinusoidal peak current, the average current of the secondary side within one switching cycle is:

$$i_{s.avg}(\theta_g) = \frac{1}{2} \frac{i_{p.max}(\theta_g)}{n} \cdot \frac{t_{off}}{T_Q} = \frac{I_p \sin(\theta_g)}{2 \left[n + \sqrt{2} \frac{U_{rms}}{U_{pv}} \sin(\theta_g) \right]} \quad \text{Equation 2.16}$$

where I_p is the peak current of the primary side over half a grid cycle.

There is a distortion factor in the equation for the average current on the secondary side. At this point, the grid-connected current output by the inverter is no longer a standard sinusoidal wave. Therefore, under the condition of constant input voltage, when the inverter operates in the BCM, compared with the DCM and CCM, the grid-connected current will have a higher THD, and injecting it to the grid will pollute the grid.

2.3.2 Comparison of the Operating Characteristics of the Three Modes

Through the operation analysis of the flyback inverter in the three modes mentioned above, the advantages and disadvantages of these three modes can be fully understood, as shown in Table 2.7.

- i. The DCM makes the control system algorithms easy to write, and there is no phenomenon of irreversible recovery in the rectifying diodes on the secondary side of the transformer. Additionally, it can also achieve high efficiency when the AC output load is small. However, its drawback lies in the lower utilization of power at full load operation;
- ii. When operating in CCM, the small change in the slope of the primary current leads to an increased demand for excitation inductance, thereby increasing the volume of the transformer, which does not meet the specifications of microinverters. Moreover, this mode also involves complex control strategies and involves reverse recovery of the rectifier diodes;
- iii. Compared with the above two modes, the BCM mode has the highest output current density and is more efficient in energy conversion. However, when the load is small, the switching frequency increases significantly, which can lead to increased consumption of switches and drivers in the long run.

Table 2.7: Comparison of the Operating Characteristics of the Three Modes

Operating Mode	Switching Frequency	Difficulty of Control	Power Density	Light Load Losses
DCM	Constant	Easy	Low	Low
CCM	Constant	Difficult	Medium	Medium
BCM	Variable	Medium	High	High

2.3.3 Comparison of the Control Strategies for Three Modes

The flyback inverter operates in different operating modes, which have various impacts on the inverter, such as the conversion efficiency, quality of the output current, complexity of the control algorithm, and service life. Therefore, an excellent control strategy plays an important role in inverters (Cichowski & Nieznanski, 2005; Gong et al., 2013; Cheng et al., 2021).

Zhang (2016) and Hu et al. (2023) analysed the situation of single-ended flyback microinverters operating in DCM, CCM and BCM and compared the voltage-current stress on the semiconductor devices in both modes, concluding that under the same power level conditions, the current stress of the single-ended flyback microinverter operating in DCM is greater, but the control strategy is relatively simpler and easier to implement compared with the CCM and BCM.

To address the demand for high efficiency in microinverters, some studies have proposed a BCM control strategy suitable for medium- and small-power-level inverters (Leuenberger & Biela, 2012; Zhang et al., 2014, 2016; Sabi & Costinett, 2019; Zhang et al., 2019; Yaqoob et al., 2021; Tang et al., 2023). By controlling the inductance current to operate in boundary current mode, Zero Voltage Switching (ZVS) of the switch tube can be achieved without adding any additional devices or auxiliary circuits. However, when the grid phase angle is small, the operating frequency of the inverter in boundary mode is relatively high (Trubitsyn et al., 2010). Although the switch tube achieves ZVS with negligible turn-

on losses, turn-off losses still exist, especially when the inverter operates at a light load, and the high switching frequency exacerbates turn-off losses, greatly reducing the conversion efficiency. Furthermore, because additional current is required to achieve soft switching, the effective value of the current does not decrease linearly with the load reduction under light load conditions, which also leads to lower efficiency of the inverter operating in boundary current mode under light load, making it difficult to achieve further efficiency optimization (Sharma & Ball, 2009; Blahník et al., 2012). Ma (2020) proposed and analysed a DCM strategy with a fixed turn-off time for inductance current, demonstrating through loss analysis that the inverter efficiency under DCM is significantly greater than that under CCM. However, when operating in a light-load DCM, the switching frequency still increases, leading to excessive switching losses. Fantino et al. (2022) proposed a bidirectional DCM constant on-time variable-frequency control strategy. The strategy enhances the converter efficiency under low-power conditions, providing fairly constant efficiency over the entire power range, by synchronously controlling both the bottom and top switches of the three boost phases. However, this method is more suitable for high-power applications and is not applicable to the single-phase microinverters studied in this thesis. Based on the fixed off-time control method, Zhang et al. (2018) proposed a variable off-time control method to modulate the preset fixed off-time to decrease the switching frequency during AC line zero-crossings and light load conditions, which is effective at improving the light load efficiency compared with the conventional fixed-frequency DCM control method. However, the issues of switch tube losses and harmonics are not mentioned. Christidis et al. (2021) proposed a

hybrid DBCM operation that inherits the merits of both the DCM and BCM and analysed a fully parameterized power loss model of the converter for DBCM modulation. Nevertheless, this model only incorporates component parameters and does not consider the parasitic parameters inherent in the components themselves.

In the conventional DCM, the turn-on of the switch is controlled by the on-time t_{on} calculated in the controller software. The on-time t_{on} is calculated based on the peak current I_{ref} on the primary side of the transformer. In theory, the peak current waveform remains constant after descending to zero until the beginning of the next cycle. However, in reality, due to the existence of parasitic parameters, after the primary current I_p of the transformer descends to 0, the parasitic capacitor C_Q will resonate with the primary inductances L_m and L_k . As a result, I_p does not remain at zero but rather continuously resonates, causing an initial value when I_p begins to rise at the start of the next switching cycle, as shown in Figure 2.19. Based on this initial value, if the transistor still conducts at the theoretically calculated on-time, the peak reference current I_{ref} on the primary side deviates from the theoretical value, affecting the quality of the output current. Lang et al. (2020) analysed the operating principle of DCM with a variable turn-off time and improved the quality of the grid-connected current by triggering the peak value of the inductance current through a hardware comparator, considering the influence of parasitic parameters on the inductance current.

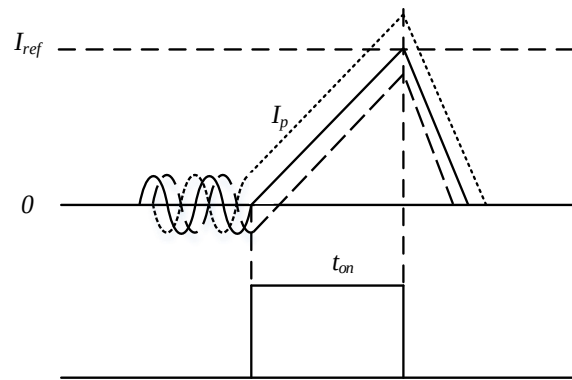


Figure 2.19: Actual Primary Current Curves under Different Initial Values

Table 2.8 summarizes the control strategies of microinverters in three operating modes, demonstrating that DCM is more suitable for low-power applications and has lower costs, aligning well with low-power, long-life, and cost-effective microinverters. Therefore, this research selected the flyback converter based on the DCM as the main circuit for the microinverter.

Table 2.8: Comparison of the Control Strategies for Three Modes

Author	Methods	Main findings	Drawbacks
Hu et al. (2023)	Comparison of DCM, BCM, and CCM	DCM is more suitable for low-power applications and has lower costs, aligning well with the microinverter.	/
Yaqoob et al. (2021)	BCM control strategy suitable for medium and small power-level inverters	It achieved Zero Voltage Switching (ZVS) of the switch tube.	When the inverter operates at light load, the high switching frequency exacerbates turn-off losses.

Table 2.8 continued

Ma (2020)	DCM with fixed turn-off time for inductance current	The inverter efficiency under DCM is significantly higher than that under CCM.	When operating in light-load discontinuous mode, the switching frequency still increases, leading to excessive switching losses.
Fantino et al. (2022)	Bidirectional DCM constant on-time variable-frequency control strategy	It enhanced the converter efficiency at low-power conditions.	This method is not applicable to the single-phase microinverters studied.
Zhang et al. (2018)	Variable turn-off time control method	It was effective in light load efficiency improvement.	It did not mention the issues of switch tube losses and harmonics.
Christidis et al. (2021)	Hybrid DBCM operation	It inherited the merits of both DCM and BCM.	It did not take into account the parasitic parameters.
Lang et al. (2020)	Variable turn-off time method in DCM	It improved the quality of light-load current.	It required additional comparator hardware to limit the peak inductance current.

2.4 Summary

This chapter provides a literature review on the topology structures and control strategies of inverters. The interleaved parallel flyback topology structure was chosen as the circuit for the microinverter studied in this thesis, and clamping technologies were discussed. It was found that the LCD clamping circuit can absorb leakage inductance at low cost. Additionally, a comparison of the three operating modes of the flyback topology was

conducted, which revealed that the DCM is more suitable for the low-power, long-life, and cost-effective microinverter studied in this research. During the literature review process, two gaps related to microinverters were identified.

- i. The use of a high-frequency transformer will inevitably increase the loss of the switch tube. How to reduce the switch loss and how to absorb the energy from the leakage inductance of the flyback transformer are the keys to improving the overall efficiency of the microinverter. Currently, much of the literature focuses on active clamping soft-switching technology. However, due to the increased number of switches, this leads to increased costs, and the control algorithm is more complex than passive clamping soft-switching, resulting in fewer applications in engineering practice. For passive clamping soft-switching, the conventional interleaved parallel flyback circuits are in an independent state, with each passive clamping circuit being responsible for a single flyback circuit, leading to duplicate component usage. Therefore, existing passive soft-switching technology still needs improvement. This research proposed a topology of an interleaved parallel passive clamping flyback microinverter with compensation capacitors to address issues such as high losses and repeated usage of components in existing passive soft-switching technology.
- ii. The flyback grid-connected inverter can achieve good results under ideal conditions. However, when considering parasitic parameters, the circuit may

experience resonance. During the resonance process, when controlling the switching of the switch, the uncertainty of the switching point can lead to energy spikes, causing device losses and heating and causing waveform oscillations, generating harmonics that affect the quality of the grid-connected current(Cichowski & Nieznanski, 2005; Gong et al., 2013; Cheng et al., 2021). Existing methods for determining peak current reference curves in the literature have not adequately considered parasitic parameters. This research proposed an optimized method for calculating peak current reference curves. The resonance multi-valley turn-on method reduces energy spikes during the switching process, effectively reducing device losses and harmonic content.

CHAPTER 3

RESEARCH METHODOLOGY

3.1 Introduction

This chapter discusses the steps followed to achieve the objectives set out in the research work. The procedures involved in the design of each module of the research are explained in detail. In Section 3.2, the methodology starts with the complete flowchart of the research procedure. The software required for the entire design process is introduced in Section 3.3. Following the flowchart, Section 3.4 introduces the structure of the conventional topology, as well as the structure, working principle, and parameter selection of the improved topology. Section 3.5 provides detailed explanations of the parameter extraction methods, the derivation process of the reference current curve, and the implementation process of the control strategy involved in the newly proposed novel Multi-Valley Turn-on (MVTO) control strategy. Section 3.6 constructs the experimental platform system framework, dividing the experimental prototype into the hardware parts of the main circuit, sampling circuits, and drive circuits and their corresponding software parts, detailing the design process and selection of these parts. Finally, a summary is given to conclude this chapter.

3.2 Research Methodology Flowchart

An extensive literature review on the subject matter was carried out, which provides the foundation and ideas in the field of photovoltaic grid-connected microinverters with

topology structures, control strategies and how to improve the existing research. This research consists of several phases: the design of the topology circuit, the proposal of a new control strategy, experimental platform development and experimental validation, as shown in Figure 3.1.

Firstly, improvements were made to the constructed conventional topology structure, functional circuits were added, and suitable component parameters were selected. In addition, the performance of the improved topology was simulated to verify the effectiveness and cost advantages of the proposed topology.

Next, the control strategy was developed, algorithms were selected to collect microinverter operating parameters, and the proposed multi-valley turn-on strategy was algorithmically programmed, simulated and compared with the fixed-frequency turn-on strategy mentioned in other literature. The objective of the comparative study was to observe the differences in their performance simultaneously. Therefore, researchers can exploit the benefits of using the proposed strategies.

Finally, a prototype and an experimental platform of a microinverter were constructed based on the designed topology and novel control strategy, and the correctness of the simulation results was verified through experiments, with an analysis and comparison of their performance.

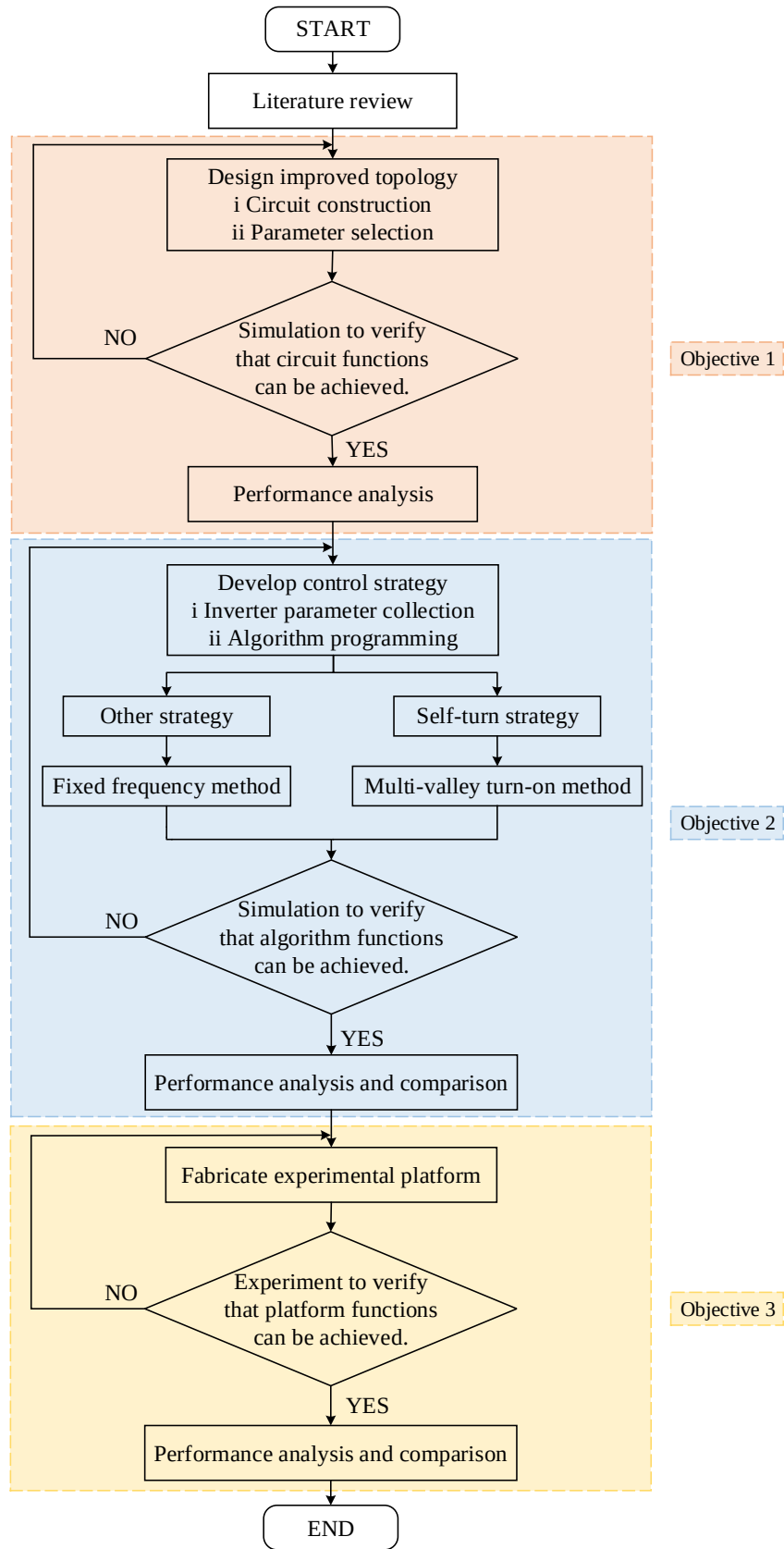


Figure 3.1: Flowchart of the Research

The three decision making boxes in Figure 3.1 assess whether the efficiency, THD, and corresponding waveforms of the topology structure, control strategy, and experimental platform meet international standards, in order to determine whether the corresponding function has been completed.

3.3 Simulation Software

This research uses Power Simulation software (PSIM) to simulate and program the entire circuit. This is a simulation application package software for the field of power electronics and motor control. It has several advantages, such as high-speed simulation, user-friendly interfaces, and waveform analysis, and effectively provides a powerful simulation environment for circuit analysis, control system design, and motor drive research. Compared with the commonly used simulation software MATLAB, the main advantages of PSIM are its high operating efficiency, greatly reduced simulation time, and accelerated circuit design and test process. The following algorithm and topology modelling also use psim.

Moreover, since PSIM lacks data processing and analysis capabilities, the plotting of algorithmic curves in the thesis was performed using MATLAB and Excel software.

3.4 Design of the Topology Structure

This research employed PSIM software for the design of the topology structure of the flyback microinverter, which mainly includes the following:

- i. Construction of the conventional topology model: Based on the topology overview in Section 2.2, the flyback inverter was selected as the basic

topology for this research. Once the improved topology has been constructed, the performance will be compared with that of the conventional flyback topology. The steps to construct the conventional topology are described in the following section.

- ii. Design of the improved topology: Improvements are made to the conventional topology model, including the addition of a compensation capacitor, the addition of passive clamping circuits, and the design of an interleaved parallel circuit. The principles and explanations of these three components are analysed and elaborated upon in the following sections.

3.4.1 Construction of the Conventional Topology

In this section, a conventional flyback topology model is constructed, appropriate parameters are selected, and the correctness of the constructed model is verified through simulation.

3.4.1.1 Construction of the Conventional Topology Model

This section builds a conventional flyback topology model, as shown in Figure 3.2, which is divided into the following three parts.

- i. The DC-DC conversion unit modulates a PWM wave with a certain duty cycle to control the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) Q , the DC waveform output by the photovoltaic module is converted into voltage U_p , and its envelope is a sinusoidal full wave with a

50 Hz frequency. Then, the voltage amplitude is changed through the transformer.

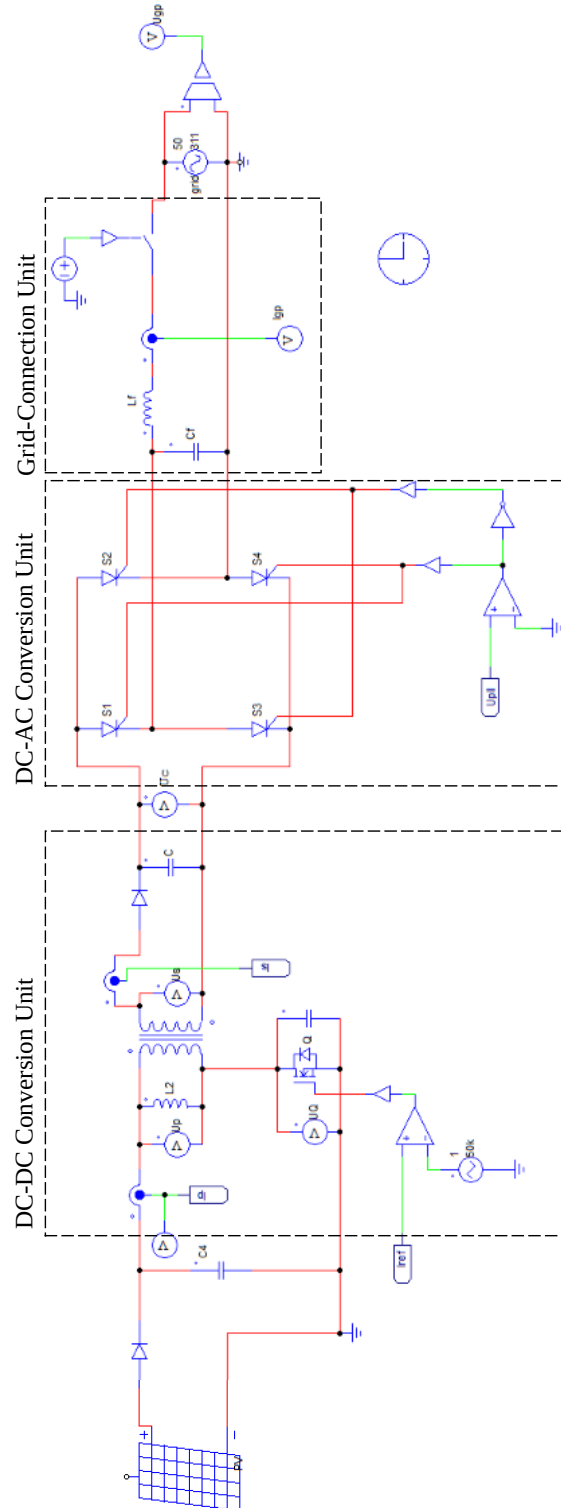


Figure 3.2: Simulation Model of the Conventional Flyback Topology Circuit

- ii. The DC-AC conversion unit modulates the PWM wave to control the transistors and converts the sinusoidal full wave into a sinusoidal AC waveform that can be grid connected.
- iii. The grid-connection unit consists of a CL filter circuit. The main function is to effectively filter out high-frequency harmonics above the switching frequency.

The key parameters of the conventional topology model are listed in Table 3.1.

Table 3.1: Key Parameters of the Conventional Topology Model

Parameter	Value	Unit
Open circuit voltage U_{oc}	40.49	V
Short circuit current I_{sc}	13.91	A
Maximum power point voltag U_{mp}	33.50	V
Maximum power point current I_{mp}	13.13	A
DC input voltage U_{pv}	25-55	V
Effective value of AC output voltage U_{gp}	220	V
Output voltage frequency f_{gp}	50	Hz
Rated output power P	200	W
Output filter capacitor C	10 n	F
Grid-side capacitor C_f	330 n	F
Grid-side inductor L_f	0.6 m	H
Maximum switching frequency f_{max}	300	kHz
Ratio of transformer n	2:12	-

In this model, it is assumed that all components are ideal switches, and switching losses are neglected, confirming the theoretical correctness of the basic topology.

The open circuit voltage U_{oc} , short circuit current I_{sc} , maximum power point voltage U_{mp} and maximum power point current I_{mp} are the electrical performance parameters of the photovoltaic module under a light intensity of 1000 W/m² and a temperature of 25°C.

3.4.1.2 Verification of the Conventional Topology Model

The key waveforms after the simulation of the conventional flyback topology model are shown in Figure 3.3.

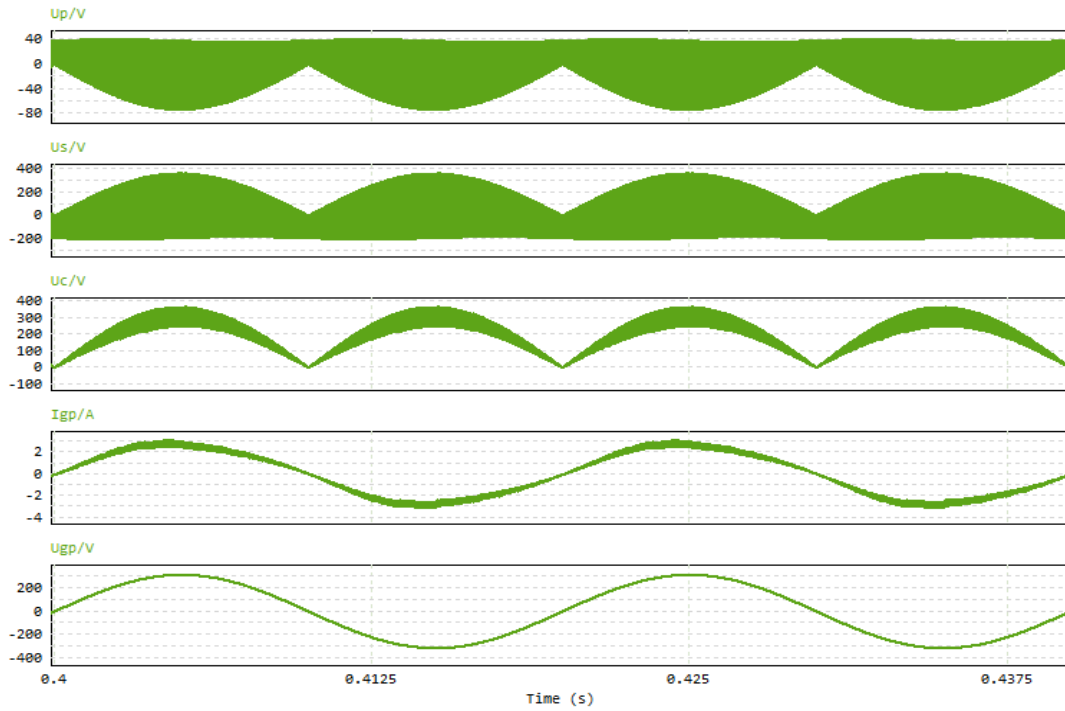


Figure 3.3: Key Waveforms of the Conventional Flyback Topology Model

From top to bottom, they represent the primary voltage U_p , secondary voltage U_s , output filter capacitor voltage U_C , grid-connected current I_{gp} , and grid voltage U_{gp} . The peak

value of U_p is -63.50 V, and the peak value of U_s is 319.48 V. After passing through the flyback transformer, the amplitude and direction of the voltage change. Following this, through the processing of the output filter capacitor and inverter circuit, a grid-connected current with the same frequency and phase as the grid voltage is obtained, facilitating grid connection.

After the above analysis, the conventional flyback inverter topology model can basically realize the functions of boosting, inverting and filtering. However, this inverter topology model only considers ideal conditions and does not account for any parasitic parameters, including leakage inductance, nor does it propose solutions to the various problems that arise due to the presence of parasitic parameters. If applied in practical engineering, challenges such as high peak voltage during switch tube turn-on, high switching frequency, low efficiency caused by high switching losses, and resonance affecting the primary current may occur, so further research is needed.

3.4.2 Design of the Improved Topology

After verifying the correctness of the conventional topology model, considering aspects such as increasing efficiency, reducing harmonics, and lowering costs, this research proposed an interleaved parallel passive clamping flyback grid-connected microinverter with compensation capacitors.

Since the two independent single-ended flyback circuits that constitute the interleaved flyback topology are identical, the improved topology can be divided into three

parts: the single-ended flyback topology with a compensation capacitor, the single-ended passive clamping flyback topology, and the interleaved parallel passive clamping flyback topology.

3.4.2.1 Single-Ended Flyback Topology with a Compensation Capacitor

i. Topology Structure

The main topology of the single-ended flyback grid-connected microinverter is shown in Figure 3.4. This research proposes a flyback microinverter topology structure with a compensation capacitor, which consists of a photovoltaic power absorption and conversion unit, a DC-DC conversion unit, a DC-AC conversion unit, and a grid-connected unit.

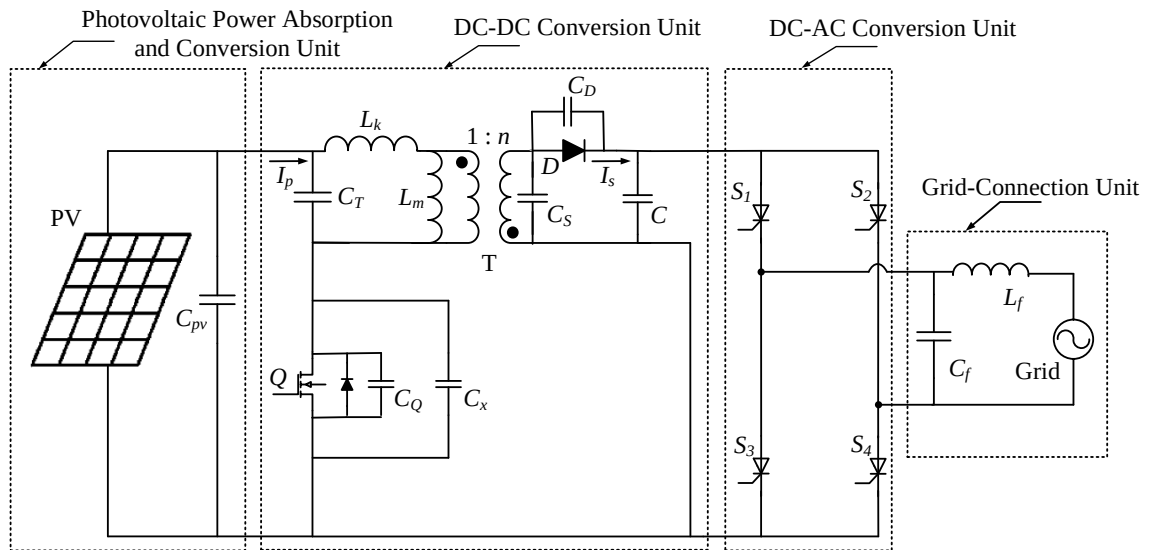


Figure 3.4: Single-Ended Flyback Topology with the Compensation Capacitor

The photovoltaic power absorption and conversion unit includes the photovoltaic module and the decoupling capacitor C_{pv} on the DC side.

The DC–DC conversion unit includes a compensation capacitor C_x for extending the resonance period, a switch tube Q operating at high frequency (where C_Q represents the parasitic capacitor of the transistor), and a high-frequency transformer T providing electrical isolation while transferring energy from the photovoltaic module to the grid. In this unit, L_m is the excitation inductance of the primary winding, L_k is the leakage inductance of the primary winding, and C_T is the distributed capacitor of the primary winding. Other components include the flyback rectifier diode D and its parasitic capacitor C_D , the absorption capacitor C_S for leakage energy, and the output filter capacitor C .

The DC–AC conversion unit includes thyristors S_1 , S_2 , S_3 , and S_4 , which are used to invert the half-wave signal output from the secondary winding of the transformer into a sinusoidal signal with the same frequency and phase as the grid.

The grid-connected unit includes the filter inductor L_f , filter capacitor C_f , and grid. The grid-connected current is injected into the grid through a low-pass filter formed by L_f and C_f .

ii. Operating Process in DCM

Section 2.3.1 introduces the operating principle of the flyback microinverter in the DCM within one grid cycle. The following section analyses the operation of the proposed topology within one switching cycle. The waveforms of the primary and secondary currents of the flyback converter under DCM are replotted in Figure 3.5, where I_p represents the primary current of the flyback transformer and I_s represents the secondary current.

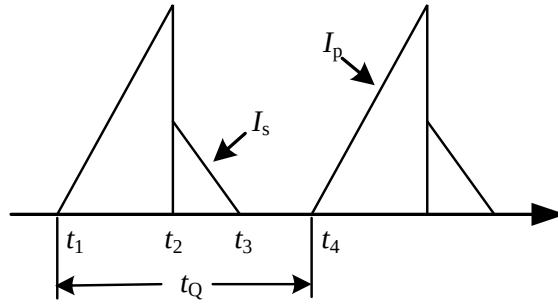


Figure 3.5: Primary and Secondary Current Waveforms of the Flyback Transformer in DCM

Due to the symmetry of the positive and negative half cycles, the positive half cycle is chosen for modal analysis. MOSFET Q operates at high frequency, and thyristors S_1 , S_2 , S_3 and S_4 operate at grid frequency. During the positive half cycle, the low-frequency bridge arms S_1 and S_4 are always conducting, while S_2 and S_3 remain off.

The operation process of the microinverter system in DCM can be divided into three modes:

Mode 1 (t_1 - t_2): As shown in Figure 3.6, Q is turned on, and the current I_p linearly increases under the action of the photovoltaic module, simultaneously flowing through the transformer primary side, causing an increase in the energy stored in the primary inductance L_m . At this point, due to the opposite polarities of the secondary side and primary side, the resonant rectifier diode D is in a reverse-biased cut-off state, storing energy in the primary winding. At this stage, no output current is supplied to the grid.

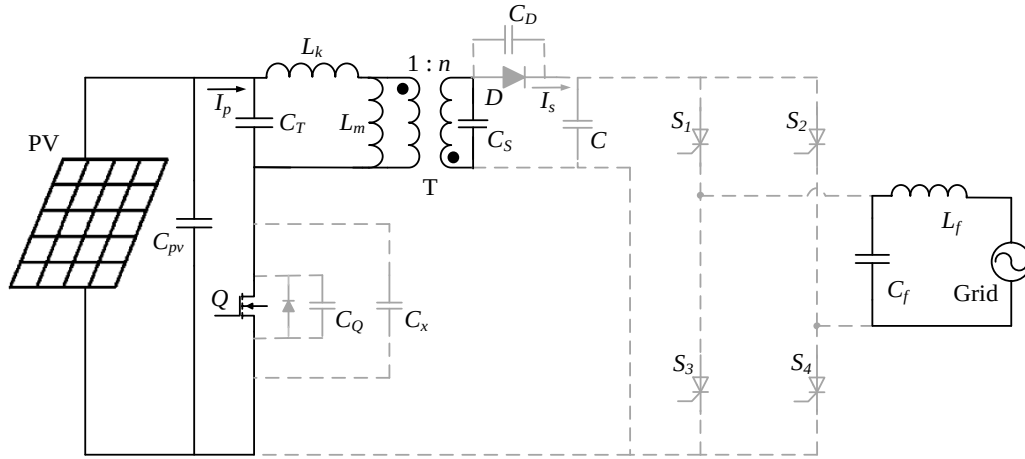


Figure 3.6: Mode 1 of the Single-Ended Flyback Topology

Mode 2 (t_2 - t_3): As shown in Figure 3.7, Q is turned off, and the current I_p decreases. Simultaneously, the primary current of the transformer T cannot change abruptly, and the energy is transferred to the secondary current through the induced electromotive force. At this moment, because the secondary side and primary side have opposite polarities, the resonant rectifier diode D conducts in the forward direction, delivering energy to the grid.

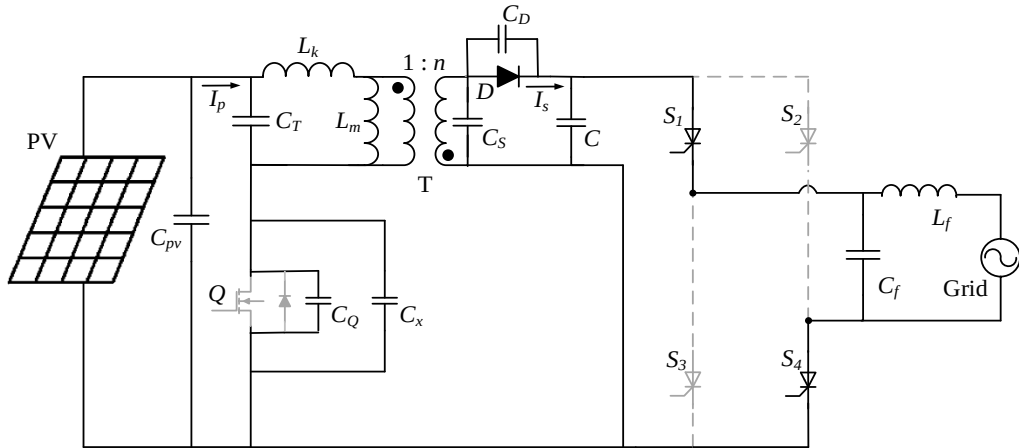


Figure 3.7: Mode 2 of the Single-Ended Flyback Topology

The leakage inductance L_k resonates with the three capacitors C_x , C_Q , and C_T , resulting in a small amplitude, with an oscillation period of

$$T_r = 2\pi\sqrt{L_k \cdot (C_x + C_Q + C_T)} \quad \text{Equation 3.1}$$

The excitation inductance L_m is clamped by the secondary voltage, so it does not participate in resonance.

Mode 3 (t_3 - t_4): As shown in Figure 3.8, Q is still disconnected, the secondary current I_s decreases to 0, and diode D is turned off. At this point, the clamping voltage exerted by the secondary side of the transformer on the primary side disappears, and there is a significant change in the voltage across C_x and C_Q . Resonance occurs among C_x , C_Q , C_T , C_s , L_k and L_m , causing fluctuations in the leakage-source voltage, with a relatively large resonant amplitude. The resonant period is

$$T_r = 2\pi\sqrt{(L_m + L_k)(C_x + C_Q + C_T + n^2 C_s)} \quad \text{Equation 3.2}$$

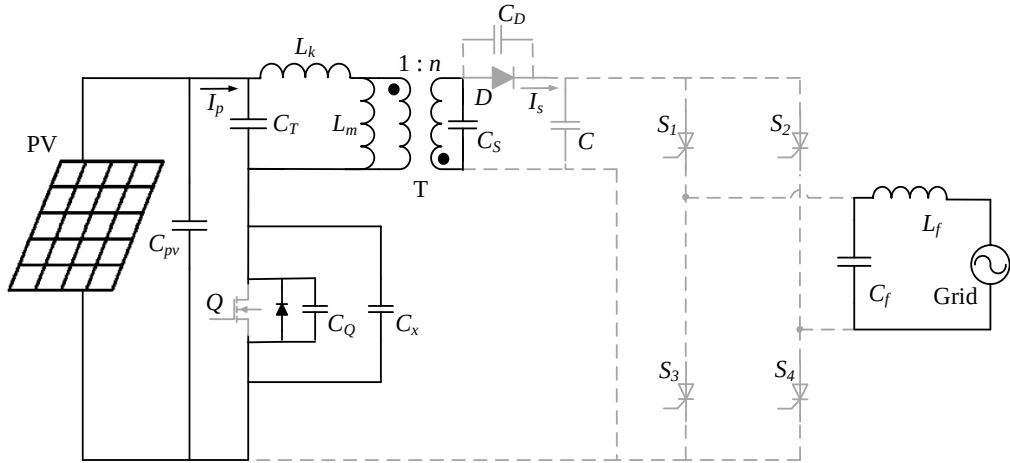


Figure 3.8: Mode 3 of the Single-Ended Flyback Topology

Based on Equation 3.1 and Equation 3.2, the addition of compensation capacitor C_x can extend the resonant period.

3.4.2.2 Single-Ended Flyback Topology with a Passive Clamping Circuit

The main topology of the single-ended passive clamping flyback microinverter is shown in Figure 3.9. The inverter is a two-stage structure, with a passive clamping flyback converter used for the front-stage DC-DC conversion and a thyristor full-bridge structure used for the rear-stage DC-AC conversion.

The topology includes a snubber capacitor C_p , a snubber diode D_p , a reset inductor L_b , and a reset diode D_b based on the single-ended flyback microinverter topology with a compensation capacitor described in Section 3.4.2.1. Additionally, due to the minimal impact of the distributed capacitor C_T and absorption capacitor C_s on the theoretical analysis below, these components are not labelled in the topology diagram in this chapter for the sake of simplicity.

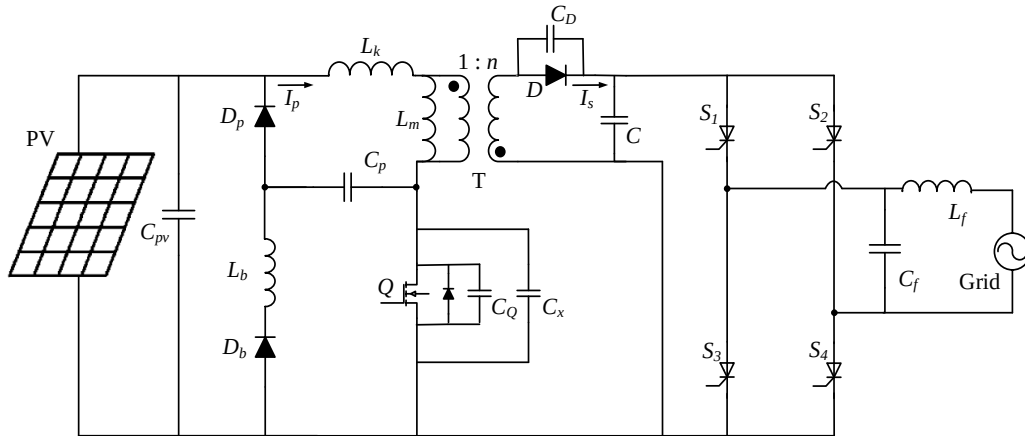


Figure 3.9: Single-Ended Passive Clamping Flyback Topology

The passive clamping operating process proposed in this research can be divided into a total of six modes, with waveforms shown in Figure 3.10.

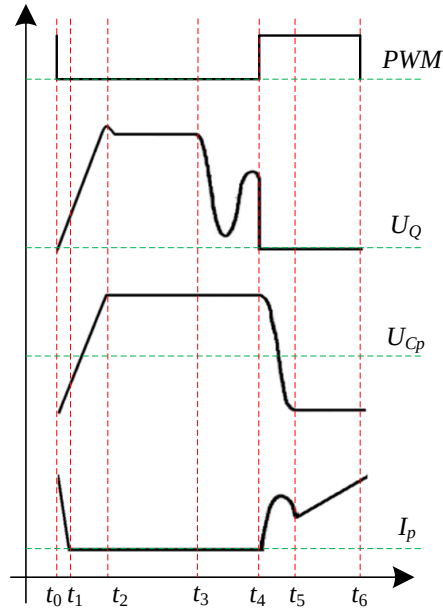


Figure 3.10: Operating Process Waveforms of Passive Clamping

Mode 1 (t_0 - t_1): As shown in Figure 3.11, at this time, the voltage direction across the snubber capacitor C_p is positive on the left and negative on the right. The driving signal PWM of the MOSFET Q is 0, and Q is turned off, entering the buffering period. The primary current I_p of the transformer is transferred to the parasitic capacitor C_Q and compensation capacitor C_x , generating resonance. When I_p decreases, the voltage U_Q across the parasitic capacitor of Q increases.

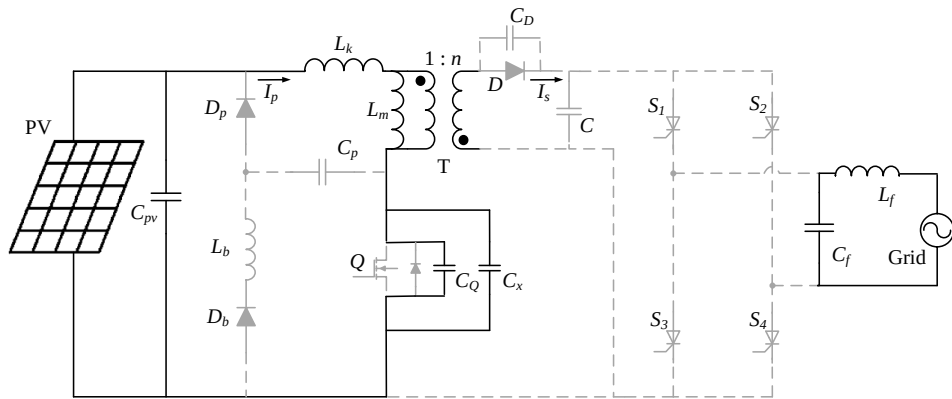


Figure 3.11: Mode 1 of the Passive Clamping Flyback Topology

voltage across the MOSFET Q undergoes significant changes, causing fluctuations in the drain-source voltage and leading to a large amplitude of resonance.

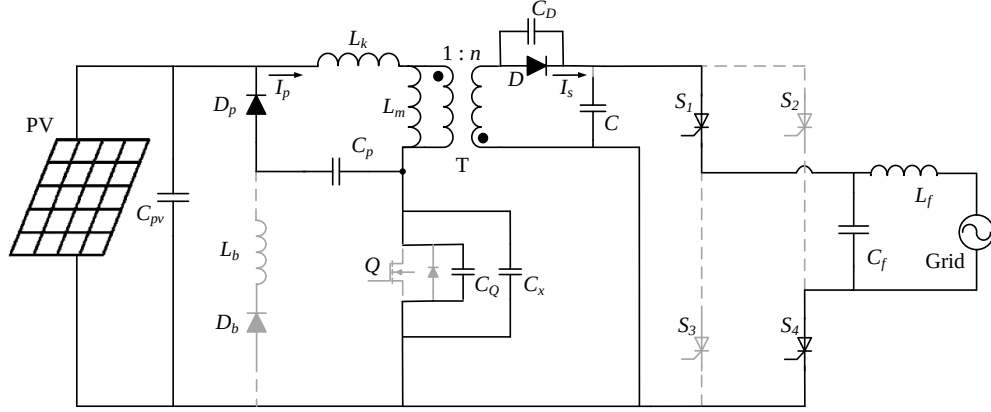


Figure 3.13: Mode 3 of the Passive Clamping Flyback Topology

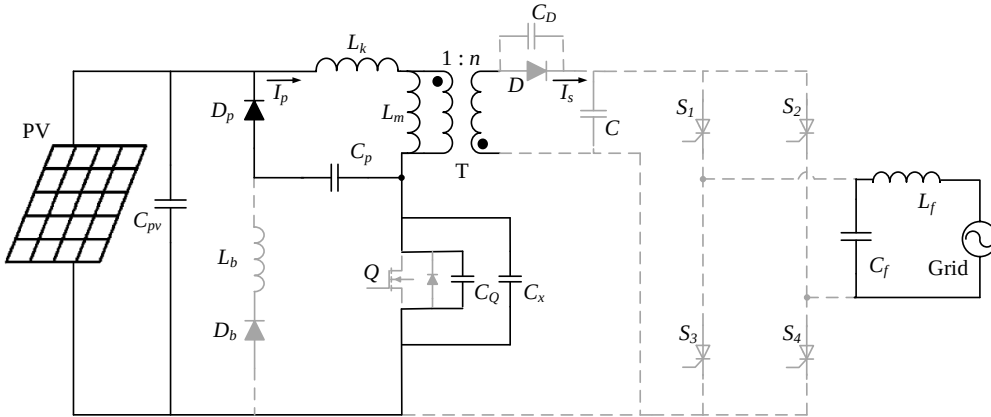


Figure 3.14: Mode 4 of the Passive Clamping Flyback Topology

Mode 5 (t_4 - t_5): As shown in Figure 3.15, to ensure that the snubber capacitor C_p functions in the next switching cycle, it needs to be completely discharged to reset. Upon the start of the reset, MOSFET Q conducts, and the snubber capacitor C_p discharges through MOSFET Q , reset inductor L_b , and reset diode D_b . Through energy exchange in the LC resonance, when the current flowing through the reset inductor L_b returns to zero, the voltage direction across the snubber capacitor C_p reverses, and the reset process ends.

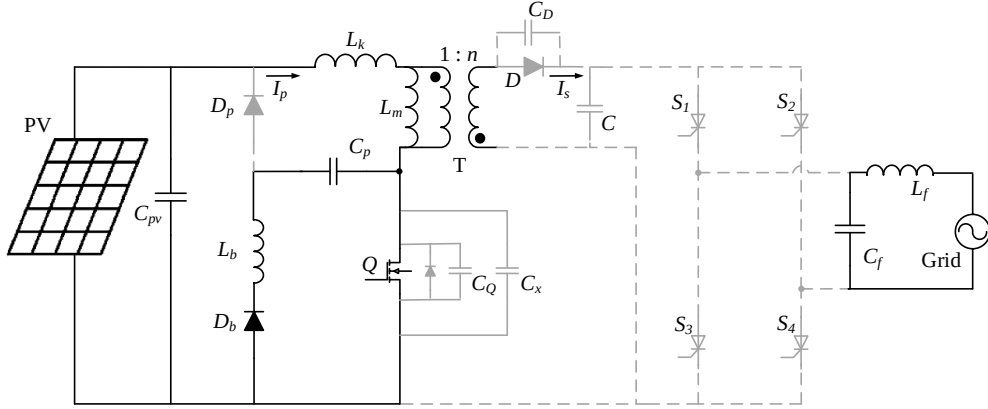


Figure 3.15: Mode 5 of the Passive Clamping Flyback Topology

Mode 6 (t_5 - t_6): As shown in Figure 3.16, the primary current I_p of the transformer increases, and the energy stored in the transformer increases until the MOSFET Q is turned off, completing one cycle.

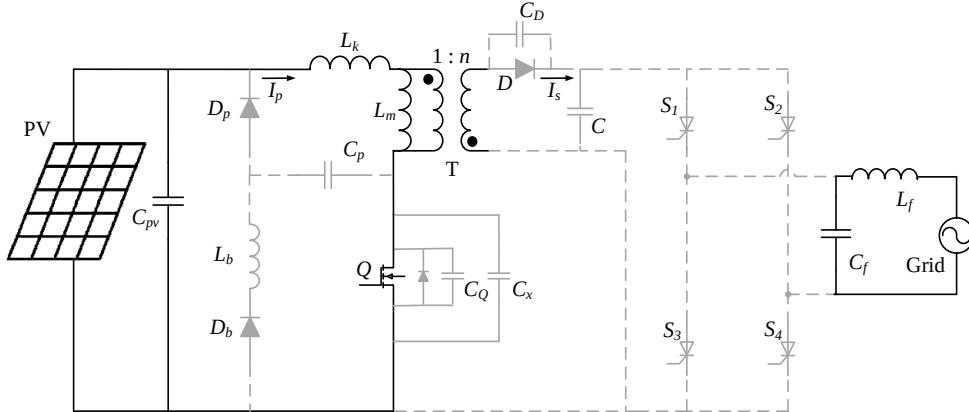


Figure 3.16: Mode 6 of the Passive Clamping Flyback Topology

3.4.2.3 Interleaved Parallel Passive Clamping Flyback Topology

Combining the compensation capacitor method proposed in Section 3.4.2.1 with the single-ended passive clamping flyback topology proposed in Section 3.4.2.2, the main topology of the interleaved parallel passive clamping flyback grid-connected microinverter

is shown in Figure 3.17. The two flyback circuits share a reset diode D_b , avoiding the redundant use of components.

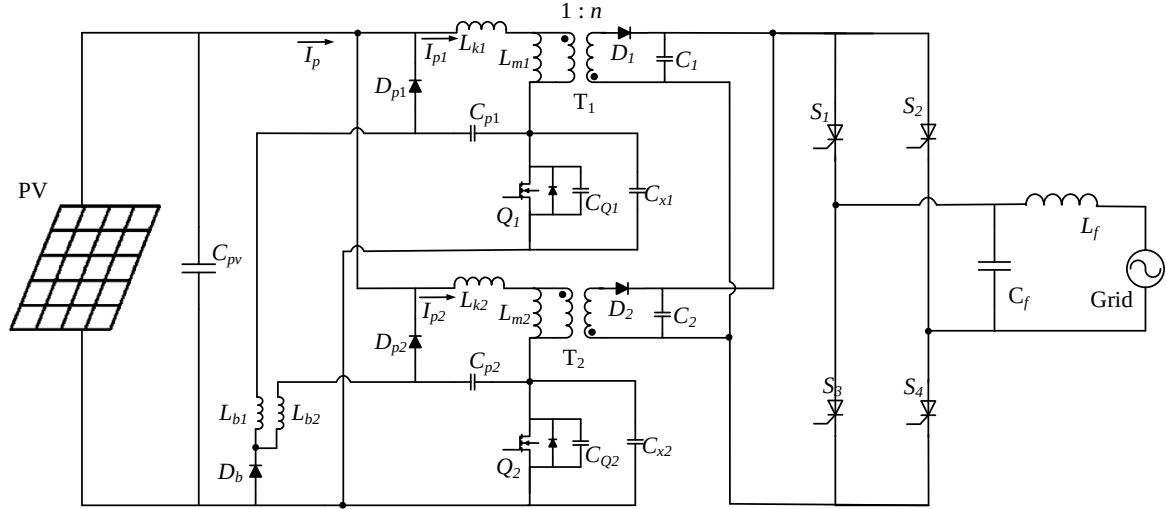


Figure 3.17: Main Circuit Topology of the Interleaved Flyback Grid-Connected Microinverter

i. Operating Process in DCM

The interleaved flyback microinverter topology is essentially an interleaved combination of two single-ended flyback converters. The operating principle and design parameters of each flyback converter circuit are the same as those of the single-ended flyback topology. The control algorithms for both are essentially the same, except that the control signal for one of them is delayed by half a switching cycle relative to the other. The current waveforms of the interleaved flyback microinverter in the DCM are shown in Figure 3.18, where I_{p1} is the primary current of the main flyback converter, I_{p2} is the primary current of the auxiliary flyback converter, I_{s1} is the secondary current of the main flyback converter, and I_{s2} is the secondary current of the auxiliary flyback converter.

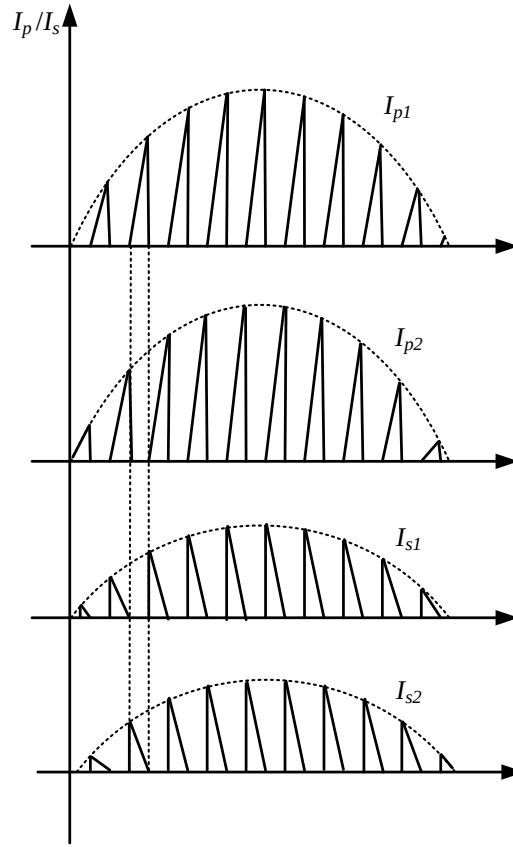


Figure 3.18: Current Waveforms of the Interleaved Flyback Topology in DCM

ii. Construction of the Improved Topology Model

The final constructed model is shown in Figure 3.19. Due to the complexity of the model, only the key improved part of the DC-DC flyback converter circuit is displayed here. The improvements include two snubber circuits, one reset circuit, two compensation capacitors, two absorption capacitors for energy dissipation, and the parasitic parameters of each component. The total simulation time for the model is 0.04 s, with a step size of 0.08 μs .

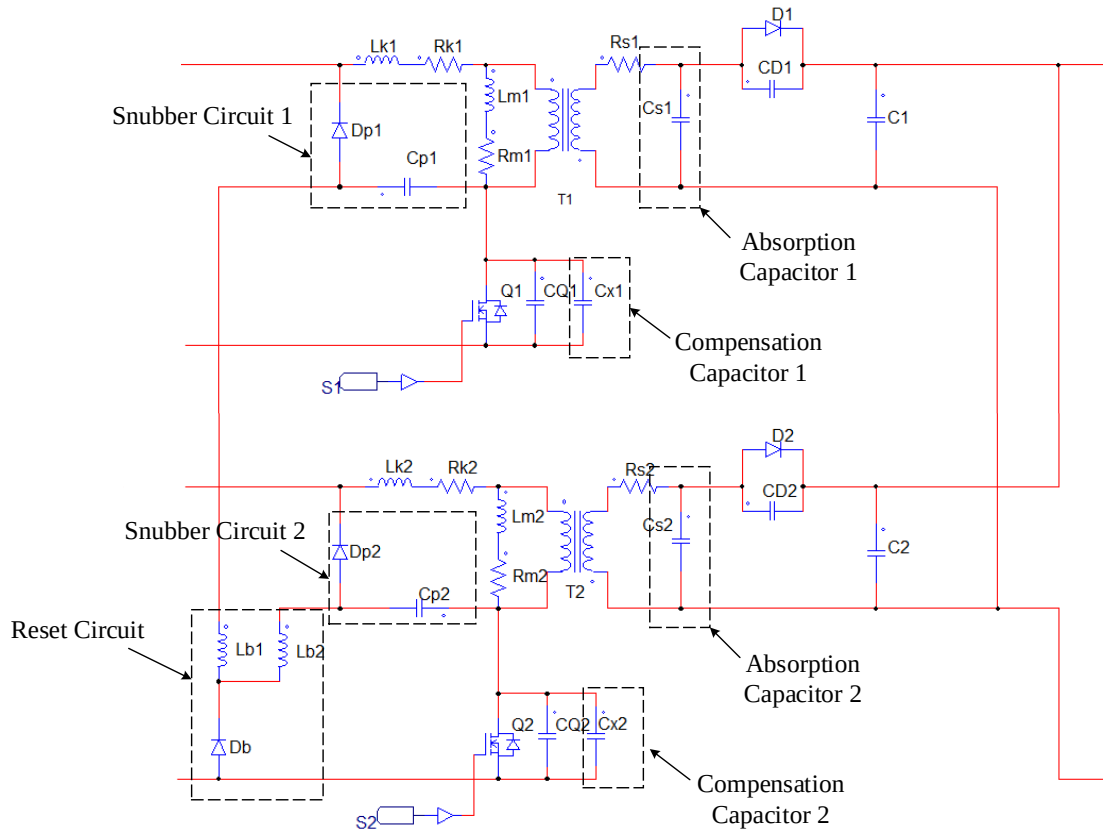


Figure 3.19: Flyback Converter Unit of the Improved Topology Model

The key parameters of the improved topology model are listed in Table 3.2. The selection of snubber capacitors C_{p1} , C_{p2} and reset inductors L_{b1} , L_{b2} is crucial. A parameter scanning method is used here, where the values of capacitors and inductors are individually adjusted to assess their impact on circuit performance, ultimately selecting the best component configuration. First, the values of the snubber capacitors are determined based on the transformer leakage inductance L_{k1} and L_{k2} . Then, the values of the reset inductors are individually adjusted to minimize the pulse in the MOSFET source-drain voltage waveform while ensuring that the inductors are appropriately sized. Besides, the parasitic parameters are obtained from measuring instruments.

Table 3.2: Key Parameters of the Improved Topology Model

Parameter	Value	Unit
DC input voltage U_{pv}	25-55	V
Effective value of AC output voltage U_{gp}	220	V
Output voltage frequency f_{gp}	50	Hz
Rated output power P	400	W
Maximum switching frequency $f_{\max}$	300	kHz
Ratio of transformer n_1, n_2	2:12	-
Output filter capacitors C_{l1}, C_{l2}	10 n	F
Snubber capacitors C_{p1}, C_{p2}	45 n	F
Reset inductor L_{b1}, L_{b2}	33 n	H
Absorption capacitors C_{s1}, C_{s2}	10 n	F
Compensation capacitors C_{x1}, C_{x2}	6.8 n	F
Parasitic parameters L_{k1}, L_{k2}	34.22 n	H
Parasitic parameters R_{k1}, R_{k2}	15.55 m	Ω
Parasitic parameters R_{m1}, R_{m2}	2.31 m	Ω
Parasitic parameters R_{s1}, R_{s2}	334 m	Ω
Parasitic parameters C_{Q1}, C_{Q2}	321.5 p	F
Parasitic parameters C_{D1}, C_{D2}	22 p	F

3.5 Developed Control Strategy

As analysed in Section 3.4.2.2, when MOSFET Q is turned on, there is a relatively high voltage due to the presence of the snubber capacitor C_p , resulting in power loss in the

MOSFET. Obviously, if the loss can be eliminated, the efficiency of the flyback converter can be further improved. The multi-valley turn-on control strategy proposed in this thesis can effectively reduce the turn-on loss of the MOSFET and harmonic content.

Because the control algorithms of the two flyback circuits in the interleaved parallel flyback topology are essentially the same, the multi-valley turn-on control strategy considering parasitic parameters in the DCM is developed based on the single-ended flyback topology, as illustrated in Figure 3.20. The main topology is shown in Figure 3.4.

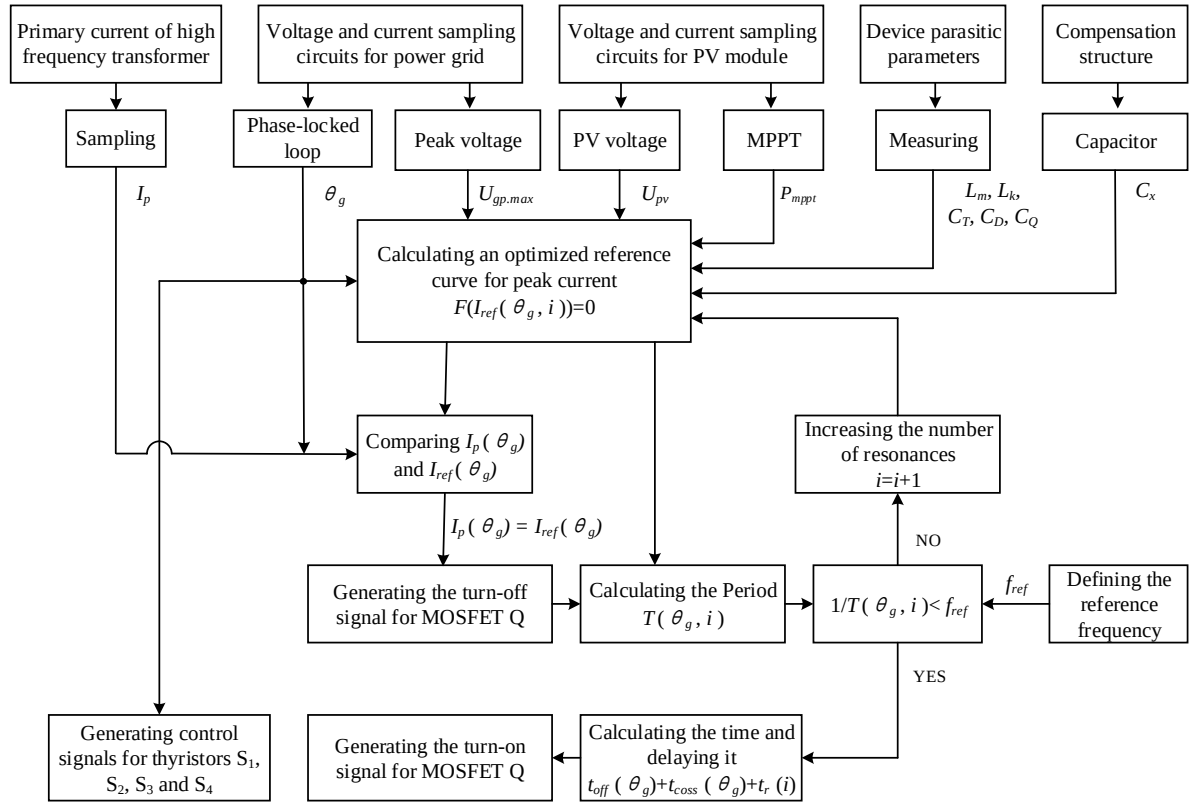


Figure 3.20: Control Strategy Diagram

Next, based on the aforementioned control strategy diagram, the parameter extraction methods, the derivation process of the reference current curve, and the implementation process of the control strategy are elucidated.

3.5.1 Parameter Extraction Method

The multi-valley turn-on control strategy designed in this thesis requires numerous parameters, including the peak grid voltage $U_{gp.max}$, photovoltaic module voltage U_{pv} , primary current I_p of the transformer, parasitic parameters of each component, maximum power P_{mppt} , and grid phase θ_g . Among these, the peak grid voltage, photovoltaic module voltage, and primary current of the transformer can be directly extracted in the simulation, and in actual equipment, they are obtained through sampling circuits (as detailed in Section 3.6.1.4). The parasitic parameters (listed in Table 3.2) of each component can be measured through measuring instruments. However, the maximum power and grid phase need to be obtained through the Maximum Power Point Tracking (MPPT) algorithm and Phase-Locked Loop (PLL) algorithm. Next, two algorithms used in this control strategy are introduced.

3.5.1.1 MPPT Algorithm

i. Operating Principle of the MPPT Algorithm

The MPPT is an important component of DC-DC control systems. DC-DC control systems mainly realize maximum power tracking of photovoltaic modules, thus improving the photoelectric conversion efficiency of photovoltaic modules. Its control block diagram is shown in Figure 3.21.

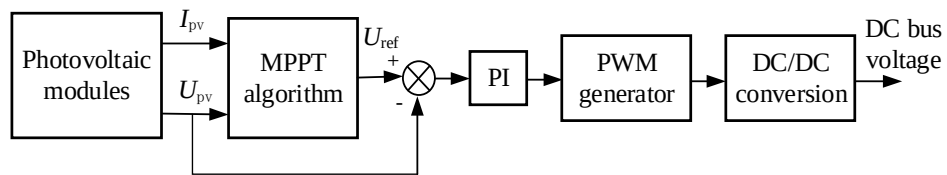


Figure 3.21: DC–DC Control System

The MPPT continuously adjusts the grid current reference through a corresponding algorithm, fine-tuning the inverter output power to regulate the output power of the photovoltaic modules and ensuring that the maximum power output is achieved. The Perturb and Observe (P&O) method, with its simple and easy-to-implement principles, is one of the most commonly used techniques in MPPT algorithms (Eltawil & Zhao, 2013; Bollipo et al., 2021). The algorithm principle involves comparing the current output power with the previous output power. Assuming $P(k+1) > P(k)$, the photovoltaic output voltage reference is perturbed in the same direction as this change; conversely, if the output power decreases, the perturbation direction changes in the next cycle. This perturbation and comparison process continues until the output power of the photovoltaic system reaches its maximum. The algorithm flow is illustrated in Figure 3.22.

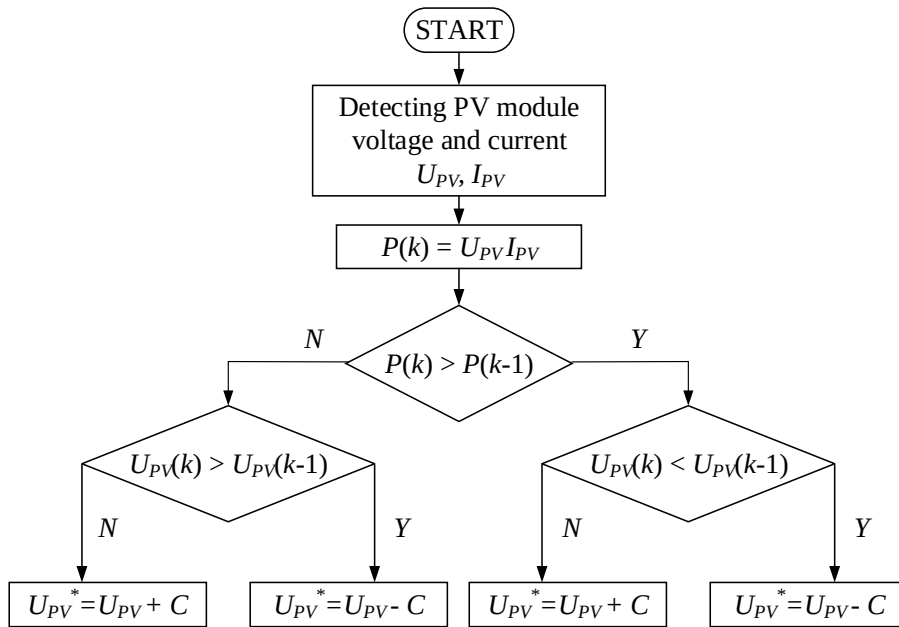


Figure 3.22: Flowchart of the P&O Method

ii. MPPT Algorithm Model

Based on the P&O method, this section establishes the MPPT simulation model, as shown in Figure 3.23. Module A is the P&O algorithm program. The value of C is set to 0.3 V. The maximum reference voltage U_{ref} is used as the feedback signal of the closed-loop control system, and U_{pv} is the output voltage of the photovoltaic module. The comparison between U_{ref} and U_{pv} obtains the maximum power current I_{mppt} through Module B of the feedforward control, PI adjustment and limiter.

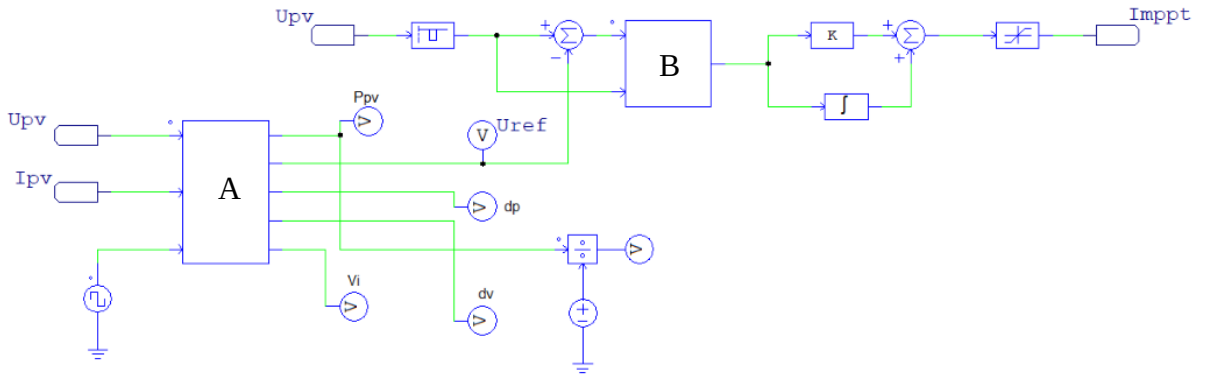


Figure 3.23: MPPT Algorithm Model

iii. Verification of the MPPT Algorithm Model

To verify the power tracking effect of the MPPT model, the maximum power voltage U_{mppt} of the photovoltaic module was set to 42 V by adjusting the light intensity and temperature, and the waveform was obtained from the simulation, as shown in Figure 3.24. The red waveform is the output voltage U_{pv} of the photovoltaic module, and the blue waveform is the reference voltage U_{ref} from the MPPT algorithm. After adjusting for 0.8 s,

the reference voltage tracked to the optimum position, achieving a maximum static MPPT efficiency of 99.64%. The tracking speed and accuracy were ensured.

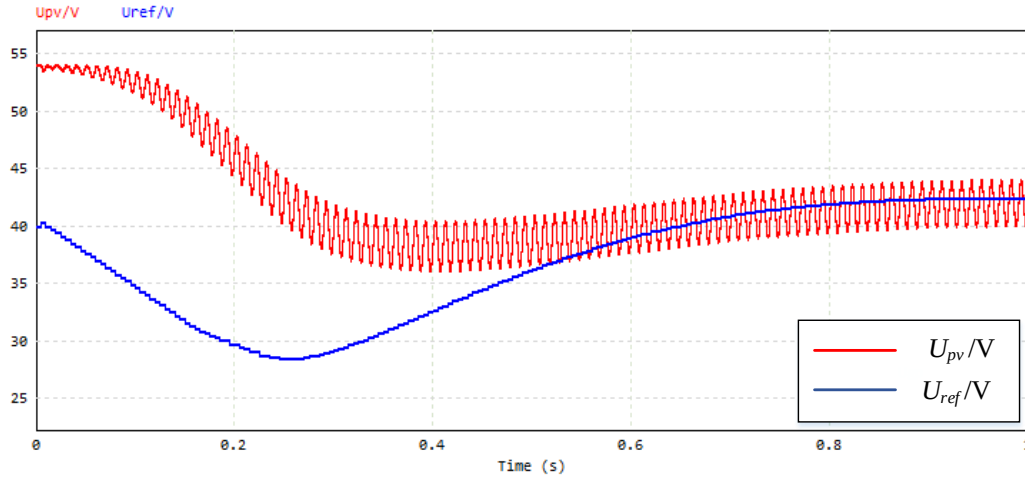


Figure 3.24: MPPT Model Simulation Result

3.5.1.2 PLL Algorithm

i. Operating Principle of the PLL Algorithm

The PLL is an important component of the DC–AC control system. A DC-AC control system generally adopts a dual-loop control system based on voltage and current. The outer voltage loop aims to stabilize the voltages across the output filter capacitors C_1 and C_2 at 350 V and provides a reference value for the inner current loop. The inner current loop mainly tracks the grid voltage by the grid-connected current to obtain a unity power factor. The overall control block diagram is shown in Figure 3.25.

In photovoltaic systems, maintaining phase synchronization between the grid voltage and grid-connected current is crucial for delivering as much high-quality electrical energy to the grid as possible.

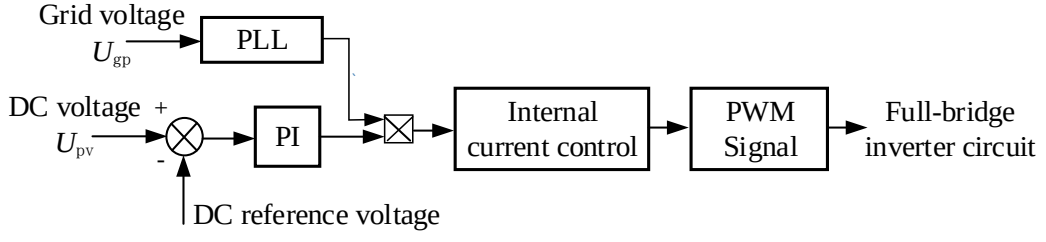


Figure 3.25: DC-AC Control System

A single-phase SOGI-PLL (Santos Filho et al., 2008; S. Wang et al., 2018; Qureshi & Potdar, 2021; Xu et al., 2021; Y. Huang et al., 2023) is employed to track the grid phase, and the control block diagram is shown in Figure 3.26, where the structure of the SOGI is enclosed within the dashed box.

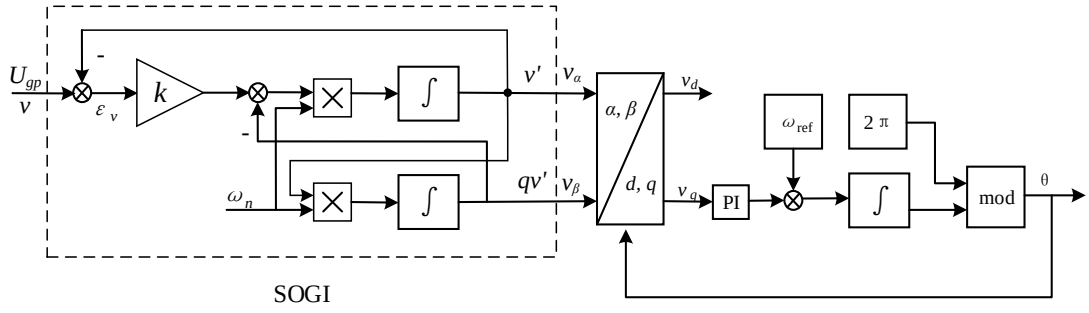


Figure 3.26: Control Block Diagram of SOGI-PLL

Firstly, the grid voltage U_{gp} is converted into virtual orthogonal signals v_α and v_β by the SOGI, which are then transformed into dq -axis DC signals through Park transformation. Then, the virtual-axis voltage signal v_d is adjusted to zero by a PI controller, combining feedforward control ω_{ref} and the integral loop, and the grid phase θ_g is ultimately obtained.

The closed-loop transfer function of the SOGI-PLL is:

$$\begin{aligned}
SOGI_v(s) &= \frac{v'}{v}(s) = \frac{k\omega_n s}{s^2 + k\omega_n s + \omega_n^2} \\
SOGI_{qv}(s) &= \frac{qv'}{v}(s) = \frac{k\omega_n^2}{s^2 + k\omega_n s + \omega_n^2}
\end{aligned}
\tag{Equation 3.3}$$

where the value of k is taken as 1.414

ii. PLL Algorithm Model

Based on the aforementioned SOGI-PLL algorithm, a grid-connected simulation model was built, as shown in Figure 3.27.

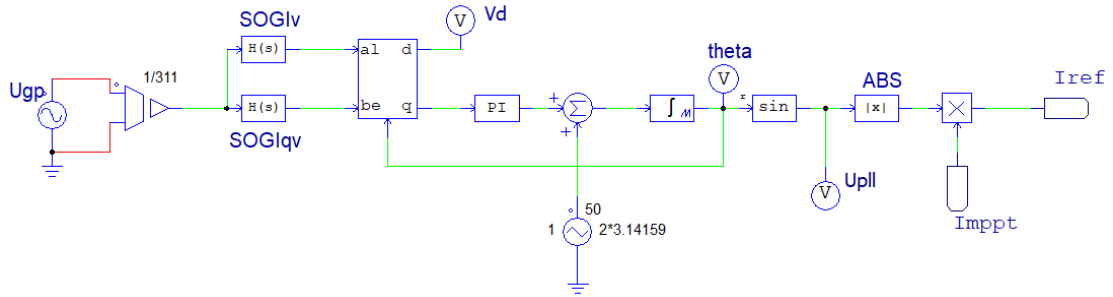


Figure 3.27: PLL Algorithm Model

After SOGI-PLL, the grid phase θ and the unit sinusoidal AC voltage U_{pll} in phase with the grid voltage are obtained. The reference current I_{ref} is obtained by multiplying the absolute value of U_{pll} by the maximum power current I_{mppt} output from the MPPT model.

iii. Verification of the PLL Algorithm Model

The correctness and effectiveness of the built PLL simulation model were verified through simulation, and the simulation waveforms are shown in Figure 3.28.

The red waveform represents the grid voltage U_{gp} after unitization, and the blue waveform is the voltage U_{pll} tracked by the PLL algorithm. After 25 ms, the tracking voltage

began to maintain a frequency and phase synchronous with the grid voltage. The SOGI-PLL algorithm can rapidly track the phase and frequency of the grid voltage, exhibiting good dynamic performance and phase-locking accuracy.

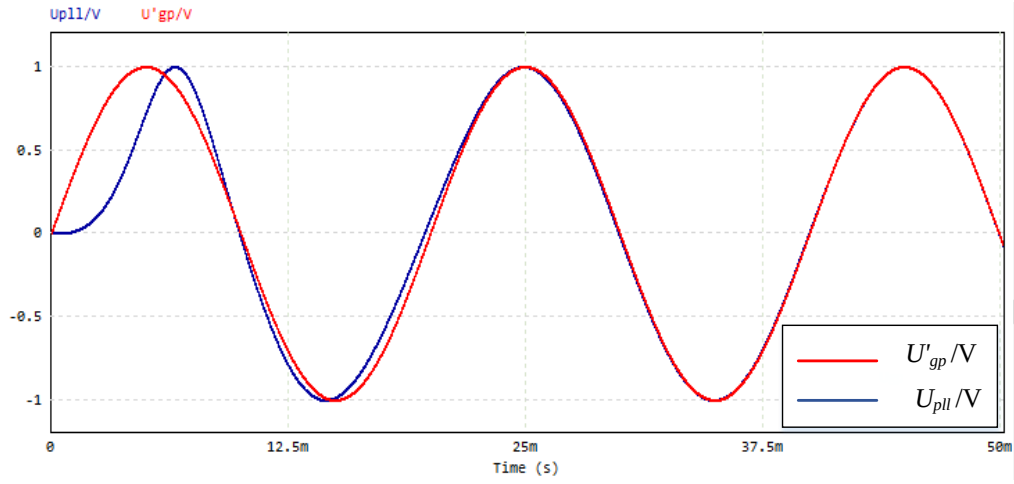


Figure 3.28: PLL Model Simulation Result

3.5.2 Derivation Process of the Reference Current Curve

The peak current reference curve is defined as $I_{ref}(\theta_g)$. When the MOSFET is turned on, the transformer primary current increases linearly. When the peak current reference curve $I_{ref}(\theta_g)$ is reached, the transistor is turned off. The rising time of the current in this stage is

$$t_{on}(\theta_g) = \frac{L_1}{U_{pv}} \cdot I_{ref}(\theta_g) \quad \text{Equation 3.4}$$

where θ_g represents the grid phase angle, U_{pv} is the output voltage of the photovoltaic module, L_1 is the primary inductance of the high-frequency transformer, and $L_1 = L_m + L_k$.

After the MOSFET is turned off, due to the influence of the transformer inductance and various parasitic capacitors, the primary current cannot immediately drop to zero, and the excitation energy cannot be directly transferred to the secondary side of the high-frequency transformer. There is a buffering time in this scenario, from the moment of turn-off until the primary current drops to zero. In this stage, at the moment of turn-off, the MOSFET voltage is zero. When the primary current drops to zero, the MOSFET voltage is clamped at $U_{pv} + U_{gp.max} \sin(\theta_g)/n$. Therefore, the buffering time during this stage is:

$$t_{coss}(\theta_g) = \frac{C_p}{I_{ref}(\theta_g)} \left(U_{pv} + \frac{U_{gp.max} \cdot \sin(\theta_g)}{n} \right) \quad \text{Equation 3.5}$$

where $U_{gp.max}$ is the peak voltage of the grid, n is the turn ratio of the secondary winding to the primary winding of the high-frequency transformer, and C_p is the resonance capacitor of the circuit, consisting of the parasitic capacitor C_Q of the MOSFET Q , the distributed capacitor C_T of the high-frequency transformer winding, the parasitic capacitor C_D of the rectifier diode, and the compensation capacitor C_x . It is expressed as:

$$C_p = C_Q + C_T + C_x + n^2 C_D \quad \text{Equation 3.6}$$

After the completion of buffering, the energy in the excitation inductance is transferred to the secondary side through the high-frequency transformer, causing a linear decline in the excitation inductance current. The time required for the secondary diode current to drop to zero can be represented as:

$$t_{off}(\theta_g) = \frac{n \cdot L_1}{U_{gp.max} \cdot \sin(\theta_g)} \cdot I_{ref}(\theta_g) \quad \text{Equation 3.7}$$

Once the secondary side diode current decreases to zero, the primary side of the high-frequency transformer will enter the resonance process due to the presence of the inductance and parasitic capacitors. The resonance period is

$$T_r = 2\pi\sqrt{L_1 \cdot C_p} \quad \text{Equation 3.8}$$

To ensure low output harmonics, it is necessary to turn on at the valley of the resonant waveform. The time for turning on at the i -th valley can be calculated as

$$t_r(i) = (2 \cdot i - 1) \cdot \pi\sqrt{L_1 \cdot C_p} \quad \text{Equation 3.9}$$

The time for one cycle can be calculated as

$$T(\theta_g, i) = t_{on}(\theta_g) + t_{cos s}(\theta_g) + t_{off}(\theta_g) + t_r(i) \quad \text{Equation 3.10}$$

As the grid-connected current is directly related to the average value of the high-frequency transformer secondary current, ensuring that the average value of the secondary current is sinusoidal can guarantee that the grid-connected current is sinusoidal.

The average value of the secondary side current is

$$I_{s.avg}(\theta_g) = \frac{1}{2} \cdot \frac{I_{ref}(\theta_g)}{n} \cdot \frac{t_{off}(\theta_g)}{T(\theta_g, i)} \quad \text{Equation 3.11}$$

To ensure that the average secondary current is sinusoidal, it is necessary to

$$I_{s.avg}(\theta_g) = I_{gp.max} \cdot \sin(\theta_g) \quad \text{Equation 3.12}$$

where $I_{gp.max}$ is the peak current of the grid.

Through the equation, it can be derived that:

$$\frac{1}{2} \cdot \frac{I_{ref}(\theta_g)}{n} \cdot \frac{t_{off}(\theta_g)}{T(\theta_g, i)} = I_{gp.max} \cdot \sin(\theta_g) \quad \text{Equation 3.13}$$

Through joint calculation, $I_{ref}(\theta_g)$ is a cubic equation for U_{pv} , $U_{gp.max}$, $I_{gp.max}$, L_1 , C_p , n and θ_g . The steady-state output power of the circuit is defined as P :

$$P = \frac{U_{gp.max} \cdot I_{gp.max}}{2} \quad \text{Equation 3.14}$$

The relevant parameters are defined as follows:

$$\begin{cases} A_0 = 4 \cdot P \cdot \sin^2(\theta_g) \\ B_0 = \frac{1}{U_{pv}} + \frac{n}{U_{gp.max} \cdot \sin(\theta_g)} \\ C_0 = (2 \cdot i - 1) \cdot \pi \cdot \sqrt{\frac{C_p}{L_1}} \\ D_0 = \frac{C_p}{L_1} \cdot (U_{pv} + \frac{U_{gp.max} \cdot \sin(\theta_g)}{n}) \end{cases} \quad \text{Equation 3.15}$$

The following can be obtained:

$$F(I_{ref}(\theta_g, i)) = (I_{ref}(\theta_g))^3 - A_0 B_0 \cdot (I_{ref}(\theta_g))^2 - A_0 C_0 \cdot (I_{ref}(\theta_g)) - A_0 D_0 = 0$$

$$\quad \text{Equation 3.16}$$

By solving the equation, the curve of $I_{ref}(\theta_g)$ can be obtained and used for the reference curve of peak current control.

3.5.3 Implementation Process of the Control Strategy

Considering parasitic parameters, the strategy calculates an accurate peak current reference curve and ensures the accuracy of the turn-off signal. By employing a multi-valley

turn-on approach based on the resonant waveform, the switching loss is reduced, the efficiency is improved, and the harmonic content of the grid current is decreased.

The specific implementation of this control strategy is as follows:

i. Detection and calculation of relevant parameters

Through the parameter extraction methods in Section 3.5.1, the peak grid voltage $U_{gp,max}$, photovoltaic module voltage U_{pv} , primary current I_p of the transformer, parasitic parameters of each component, maximum power P_{mppt} , and grid phase θ_g are extracted. The parasitic parameters are obtained through measuring instruments, including the excitation inductance L_m of the primary side of the high-frequency transformer, leakage inductance L_k of the primary side, distributed capacitor C_T of the primary side, parasitic capacitor C_D of the flyback rectifier diode, and parasitic capacitor C_Q of MOSFET Q . Additionally, control signals for thyristors S_1 , S_2 , S_3 and S_4 can be generated based on the detected phase angle θ_g .

ii. The optimized reference current curve for peak current control is calculated through mathematical derivation. The specific derivation process can be found in section 3.5.2.

iii. Generation of the turn-off signal for MOSFET Q

The control system detects the primary current $I_p(\theta_g)$ of the high-frequency transformer at different phase angles and compares it with the optimized reference current curve $I_{ref}(\theta_g)$. The turn-off signal for MOSFET Q is generated when $I_p(\theta_g)$ reaches the value

of $I_{ref}(\theta_g)$. Subsequently, the system calculates the linear rise time $t_{on}(\theta_g)$ of the transformer primary current, the current buffering time $t_{coss}(\theta_g)$, the time $t_{off}(\theta_g)$ required for the secondary diode current to reach 0, and the time $t_r(i)$ for the i -th harmonic valley. Finally, the switching period $T(\theta_g, i)$ and the switching frequency are computed.

iv. Generation of the turn-on signal for MOSFET Q

The system defines a reference frequency f_{ref} as a frequency limit to prevent problems caused by excessive frequency and compares the switching frequency $1/T(\theta_g, i)$ of the transistor with the reference frequency f_{ref} .

If $1/T(\theta_g, i) < f_{ref}$, the system calculates the time and introduces a delay of $t_{off}(\theta_g) + t_{coss}(\theta_g) + t_r(i)$, subsequently generating the turn-on signal for MOSFET Q.

If $1/T(\theta_g, i) \geq f_{ref}$, the system increases the harmonic number by setting $i=i+1$ and returns to compute the optimized reference current curve for peak current control. This process is repeated until $1/T(\theta_g, i) < f_{ref}$ and the turn-on signal for MOSFET Q is generated.

3.6 Fabrication of the Experimental Platform

The system functional block diagram of the experimental platform is shown in Figure 3.29. A Digital Signal Processor (DSP) collects the voltage and current signals of the photovoltaic module, MOSFET current and flyback output signals, grid voltage and zero-crossing signals, and grid-connected current signals. These signals are processed by the software programs of the Central Processing Unit (CPU) to control the drive circuits that

output PWM signals to the main circuit, thereby achieving flyback, inversion, and grid-connection functions.

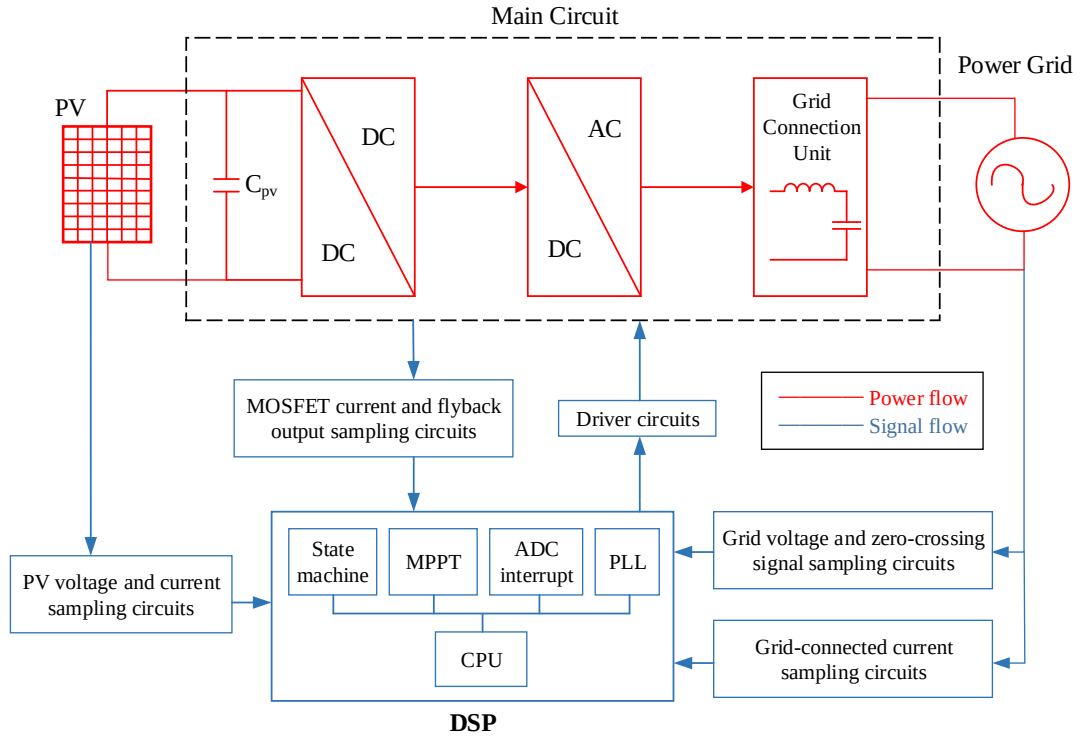


Figure 3.29: System Functional Block Diagram of the Experimental Platform

Based on the system functional block diagram, the hardware circuits of the microinverter were designed firstly, including the main circuit, sampling circuits, and drive circuits. Then, an overall plan was made for the software process, and a flowchart of the main functional modules was provided. This laid the theoretical foundation for the construction of the experimental prototype and platform in Chapter 4.

3.6.1 Design of Hardware Circuits

According to the division of the topology structure, the hardware circuit is also divided into three parts: the DC–DC conversion unit, the DC–AC conversion unit, and the

Grid-connected unit. Among them, the DC–DC conversion unit is the focus of this research, which includes the coupling capacitor, the flyback transformer, MOSFETs, and the flyback output diode. In addition, sampling circuits for voltage and current of each part of the main circuit, as well as the driving circuits for MOSFETs and thyristors, are also indispensable. The following will detail the design of these components.

3.6.1.1 Design of the DC–DC Conversion Unit

i. Design of the Decoupling Capacitor C_{pv}

In a single-phase photovoltaic grid-connected power generation system, there is an instantaneous imbalance between the input power and output power, so it is necessary to design a decoupling capacitor to balance the difference between the input and output instantaneous power (Zengin et al., 2013). During the stable operation of the power generation system, it is assumed that the output power of the photovoltaic module remains at the MPP; that is, the input power of the photovoltaic power generation system is a constant value:

$$P_i(t) = U_{pv.mpp} \times I_{pv.mpp} \quad \text{Equation 3.17}$$

where $U_{pv.mpp}$ and $I_{pv.mpp}$ are the voltage and current at the MPP of the photovoltaic module, respectively, and $P_i(t)$ is the instantaneous input power of the photovoltaic power generation system.

Assuming a unity power factor, the output power of the grid-connected system is:

$$P_o(t) = U_{gp} \sin(\omega t) \times I_{gp} \sin(\omega t) = \frac{1}{2} U_{gp} I_{gp} (1 + \cos(2\omega t)) \quad \text{Equation 3.18}$$

Equation 3.17 and Equation 3.18 show that the difference between the instantaneous input power and the instantaneous output power of the photovoltaic system is an AC quantity twice the frequency of the grid, i.e., $\frac{1}{2} U_{gp} I_{gp} \cos(2\omega t)$. This difference needs to be balanced by a decoupling capacitor:

$$\frac{1}{2} C_{pv} U_{pv.max}^2 - \frac{1}{2} C_{pv} U_{pv.min}^2 = \int_{-\frac{\pi}{4\omega}}^{\frac{\pi}{4\omega}} (P_i(t) - P_o(t)) dt \quad \text{Equation 3.19}$$

Therefore,

$$C_{pv} = \frac{P_{mppt}}{2\omega \times U_{pv.mppt} \times U_{ripple}} \quad \text{Equation 3.20}$$

where C_{pv} is the decoupling capacitor; P_{mppt} is the maximum power output of the photovoltaic module, taken as 250 W; ω is the angular frequency of the grid voltage; and U_{ripple} is the ripple of the photovoltaic module output voltage.

To achieve a 98% utilization rate of photovoltaic output, the output voltage fluctuation of the photovoltaic module should be less than 8.5% of its MPP voltage (Kjaer et al., 2005). To further increase the utilization rate of the photovoltaic output, it is taken as

$$U_{ripple} \leq 5\% \times U_{pv.mppt} \quad \text{Equation 3.21}$$

From Equation 3.20 and Equation 3.21, $C_{pv} > 2.63$ mF can be obtained ($U_{pv.mppt}=55$ V). For this platform, four 2700 μ F electrolytic capacitors were connected in parallel.

ii. Design of the flyback transformer

As a crucial component in power conversion, the design of a flyback converter is

naturally of utmost importance, and its reliable operation relies on a well-performing flyback transformer. The basic parameters of the flyback transformer in the DCM are shown in Table 3.3.

Table 3.3: Design parameters of the Flyback Transformer

No	Parameters	Value	Unit
1	Input voltage U_{pv}	25~55	V
2	Output voltage U_{gp}	$220\sqrt{2}(1+7\%)$	V
3	Rated output power P_o	400	W
4	Maximum switching frequency f_{Q_max}	300	kHz
5	Maximum duty cycle D_{max}	0.55	-
6	Maximum operating magnetic flux coefficient B_m	0.41	T
7	Converter efficiency η	95%	-

In addition, the primary side inductance of the transformer is calculated as (W. Gao, 2012):

$$L_m \leq \frac{U_{pv.min}^2 T_Q D_{max}^2}{2P_o/\eta} \quad \text{Equation 3.22}$$

where $U_{pv.min}$ is the minimum input voltage of the system (i.e., the minimum output voltage of the photovoltaic module) and T_Q is the switching period of the MOSFET.

By using Equation 3.22, $L_m \leq 3.89 \mu\text{H}$ is calculated, and the actual value of L_m is $3.55 \mu\text{H}$.

The turns ratio of the transformer is:

$$n \leq \frac{220\sqrt{2}(1+7\%) \times D_{max}}{U_{pv,max}(1-D_{max})} = 6.7 \quad \text{Equation 3.23}$$

Taking $n=6$.

Next, the appropriate core is selected. The output power P_0 at this point is 400 W, corresponding to a system rated power of 400 W for the interleaved flyback converter. Therefore, the respective rated power for the two interleaved forward converters is $P_{01} = P_{02} = 200$ W. Based on the power, relevant design parameters of magnetic cores are investigated, and the PQ3415 magnetic core is selected, with a cross-sectional area with a cross-sectional area A_e of 154 mm².

The primary winding turns N_p are calculated as:

$$N_p = \frac{L_m \cdot I_p}{B_m \cdot A_e} = \frac{L_m}{B_m \cdot A_e} \cdot \frac{2P_o}{\eta \cdot U_{pv,min} \cdot D_{max}} \approx 1.72 \quad \text{Equation 3.24}$$

Taking $N_p=2$.

The number of secondary winding turns N_s is calculated as:

$$N_s = n \cdot N_p = 12 \quad \text{Equation 3.25}$$

iii. Selection of the MOSFET

In the process of system operation, the voltage stress of MOSFETs Q_1 and Q_2 is the maximum voltage they endure when turned off. When Q_1 and Q_2 are turned off, the voltage is the sum of the input voltage and the voltage reflected from the secondary side of the transformer to the primary side. Therefore, the voltage stress of the MOSFETs is:

$$U_{Q1.max} = U_{Q2.max} = U_{pv} + \frac{\sqrt{2} \times 220}{n} = 86.85V \quad \text{Equation 3.26}$$

The current stress of the MOSFET is the maximum current flowing through the transistor during system operation. When the MOSFETs are conducting, the current is the operating current. The current stress of the MOSFET is (Z. Zhang, 2016):

$$I_{Q.max} = 2 \sqrt{\frac{I_{pv} U_{pv}}{L_m f_Q}} = 15.87A \quad \text{Equation 3.27}$$

According to the voltage and current stress, considering a safety margin of one to two times, the HGN099N15S produced by Hunteck Company in China, with a voltage rating of 150 V and a current rating of 60 A, was selected.

iv. Selection of the flyback output diode

When the MOSFET is conducting, the flyback output diodes D_1 and D_2 endure the maximum reverse voltage. Therefore, their voltage stress is:

$$U_{D1.max} = U_{D2.max} = nU_{pv} + \sqrt{2} \times 220 = 521.13V \quad \text{Equation 3.28}$$

Furthermore, according to the relationship between the primary and secondary currents of the transformer, the current stress on the flyback output diodes D_1 and D_2 is:

$$I_{D1.max} = I_{D2.max} = \frac{I_{Q.max}}{n} = 2.645A \quad \text{Equation 3.29}$$

Considering the ringing issue caused by the reverse recovery of the diode (Yuan et al., 2014), the silicon carbide diode MSD02120G1 produced by Msemitex Company in China, with a reverse voltage rating of 1200 V and a current rating of 10 A, was selected.

3.6.1.2 Design of the DC–AC Conversion Unit

Thysistors S_1 - S_4 endure a voltage stress equal to the peak value of the grid voltage. Considering the permissible fluctuation of 7% in the single-phase grid voltage specified in the grid-connected standard, the voltage stress is approximately 332.9 V. Simultaneously, considering the current stress, which is the same as that of the flyback output diode, the HSB80R240K2 produced by Hunteck Company in China, with a voltage rating of 800 V and a current rating of 20 A, was selected.

3.6.1.3 Design of the Grid-Connected Unit

The design of the grid-connected unit is essentially the design of the filter, aiming to create a filter capable of effectively attenuating high-frequency harmonics. Since the flyback converter in this thesis operates in DCM, behaving like a current source, a CL filter is used for the output. Generally, the design of a CL filter needs to consider two factors: the cut-off frequency of the filtering network and the magnitude of the reactive power produced by the filtering capacitors.

The cut-off frequency of the filtering network is calculated as:

$$f_c = \frac{1}{2\pi\sqrt{L_f \times C_f}} \quad \text{Equation 3.30}$$

The cut-off frequency f_c must be much higher than the fundamental frequency f_{gp} of the grid current and much lower than the switching frequency f_Q , setting the range as

$$10f_{gp} < f_c < \frac{f_Q}{10} \quad \text{Equation 3.31}$$

The known fundamental frequency f_{gp} of the grid current is 50 Hz, and the maximum switching frequency $f_{Q,max}$ is 300 kHz. Therefore, the range of the cut-off frequency of the filtering network is

$$500\text{Hz} < f_c < 30000\text{Hz} \quad \text{Equation 3.32}$$

According to Equation 3.30 and Equation 3.32,

$$\frac{10^{-8}}{\pi^2} < L_f \times C_f < \frac{10^{-6}}{\pi^2} \quad \text{Equation 3.33}$$

In addition, the relevant regulations for grid-connected photovoltaic systems state that when the output of the inverter in the photovoltaic system exceeds 50% of its rated output, the average power factor should not be less than 0.9 (leading or lagging). Firstly, the DC-DC conversion unit and DC-AC conversion unit are equivalently treated as a current source, and the grid-connected unit is redrawn, as shown in Figure 3.30 (Z. Zhang, 2016).

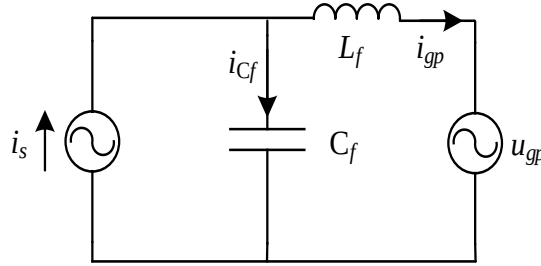


Figure 3.30: Grid-Connected Unit Equivalent Circuit

Assuming that the system operates normally, the grid-connected current and the grid voltage are in phase and frequency, indicating a grid power factor of 1. Therefore, the grid-connected current can be expressed as:

$$i_{gp} = \frac{\sqrt{2}P_0}{220} \sin \omega t \quad \text{Equation 3.34}$$

As shown in the Figure 3.30, the current flowing through the inductor L_f is i_{gp} . According to the self-inductance equation, substituting into Equation 3.34, the voltage across the filtering inductor L_f is

$$u_{L_f} = L_f \frac{di_{gp}}{dt} = \frac{2\omega L_f P_0}{220\sqrt{2}} \cos\omega t \quad \text{Equation 3.35}$$

The voltage u_{C_f} across the filtering capacitor C_f consists of the voltage u_{L_f} across the inductor L_f and the grid voltage u_{gp} , substituting into Equation 3.35, the voltage u_{C_f} is

$$u_{C_f} = u_{L_f} + u_{gp} = \frac{2\omega L_f P_0}{220\sqrt{2}} + 220\sqrt{2} \sin\omega t \quad \text{Equation 3.36}$$

Given the voltage across the capacitor C_f , according to the differential equation for the capacitor current, the current flowing through the filtering capacitor C_f is:

$$i_{C_f} = C_f \frac{du_{C_f}}{dt} = (220\sqrt{2}\omega C_f) \cos\omega t - \left(\frac{2\omega^2 L_f C_f P_0}{220\sqrt{2}}\right) \sin\omega t \quad \text{Equation 3.37}$$

From Equation 3.34 and Equation 3.37, the output current of the equivalent current source can be expressed as:

$$i_s = (220\sqrt{2}\omega C_f) \cos\omega t + \left(\frac{2P_0(1-\omega^2 L_f C_f)}{220\sqrt{2}}\right) \sin\omega t \quad \text{Equation 3.38}$$

From Equation 3.38, the phase angle between the grid-connected current and the grid voltage is:

$$\varphi_{gp} = \arctan \left[\frac{220^2 \omega C_f}{P_0(1-\omega^2 L_f C_f)} \right] \quad \text{Equation 3.39}$$

When the cut-off frequency of the output filtering network is $500 \text{ Hz} < f_c < 30000 \text{ Hz}$, $1 - \omega^2 L_f C_f \approx 1$:

$$\varphi_{gp} = \arctan \left[\frac{220^2 \omega C_f}{P_0} \right] \quad \text{Equation 3.40}$$

Equation 3.40 indicates that the power factor is related to the output filtering capacitor and the output power. When the filtering capacitor is constant, φ_{gp} decreases with increasing power factor. When the output power P_o is constant, φ_{gp} increases with increasing filtering capacitor. To ensure that the power factor of the microinverter is $\cos\varphi_{gp} \geq 0.9$ at 50% of the rated power, the following condition needs to be met:

$$\cos\varphi_{gp} = \cos\left(\arctan\left[\frac{220^2\omega C_f}{0.5P_o}\right]\right) \geq 0.9 \quad \text{Equation 3.41}$$

Considering the above factors, the filtering network parameters can be taken as $L_f = 0.6$ mH and $C_f = 330$ nF.

3.6.1.4 Design of the Sampling Circuits

i. Voltage sampling of the photovoltaic modules

The output voltage sampling circuit of the photovoltaic modules is shown in Figure 3.31. An operational amplifier (GS8592) was used here. The designed microinverter for this research has two parallel-connected photovoltaic modules; hence, the amplifier has two pairs of input and output interfaces.

The relationship between the output voltage of the photovoltaic modules and its sampling signal is expressed as:

$$U_{pv1.dsp} = U_{pv1} \frac{R_{112}}{R_{112} + R_{25}} \quad \text{Equation 3.42}$$

$$U_{pv2.dsp} = U_{pv2} \frac{R_{113}}{R_{113} + R_{30}} \quad \text{Equation 3.43}$$

where $U_{pv1.dsp}$ and $U_{pv2.dsp}$ are the sampling signals of the output voltage from the photovoltaic modules sent to the DSP and U_{pv1} and U_{pv2} are the actual output voltage signals of the PV modules.

By adjusting the resistance value in Equation 3.42 and Equation 3.43, the output voltages of the photovoltaic modules are sampled and conditioned to obtain sampling signals ranging from 0 to 3.3 V, which are then sent to the DSP for further processing.

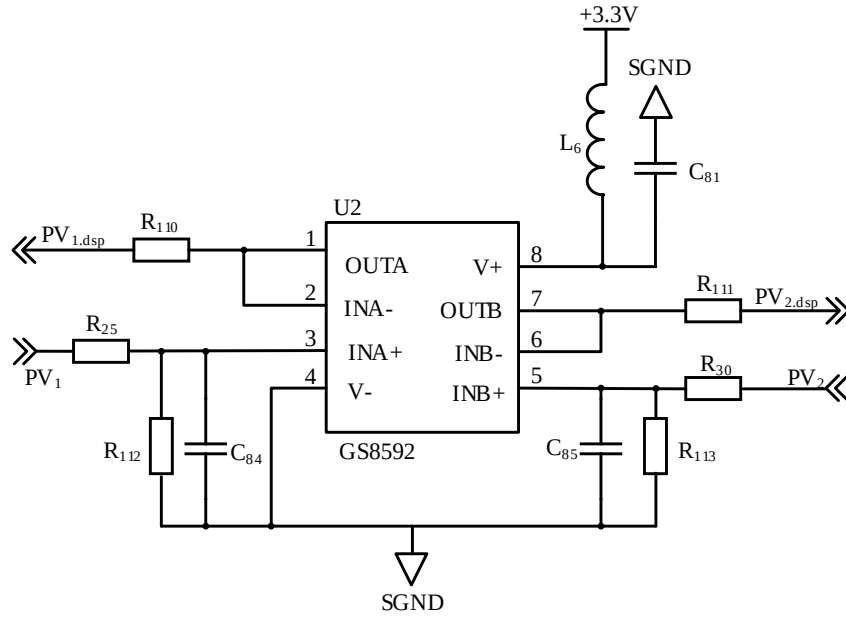


Figure 3.31: Voltage Sampling Circuit of the Photovoltaic Modules

ii. Current sampling of the photovoltaic modules

The output current sampling circuit of the photovoltaic modules, taking PV_1 as an example, is shown in Figure 3.32. The output current sampling circuit for PV_2 has the same structure and therefore is not listed separately, where R_{220} , R_{221} , and C_{41} form an RC filtering circuit, R_{49} is the sampling resistor with a value of 3 m Ω connected in series to the negative

terminal of PV_1 , and the current flowing through the sampling resistor is the photovoltaic module output current I_{pv1} . The voltage $U(I_{pv1})$ across the sampling resistor serves as the input signal to the operational amplifier, similar to the operation amplifier GS8592.

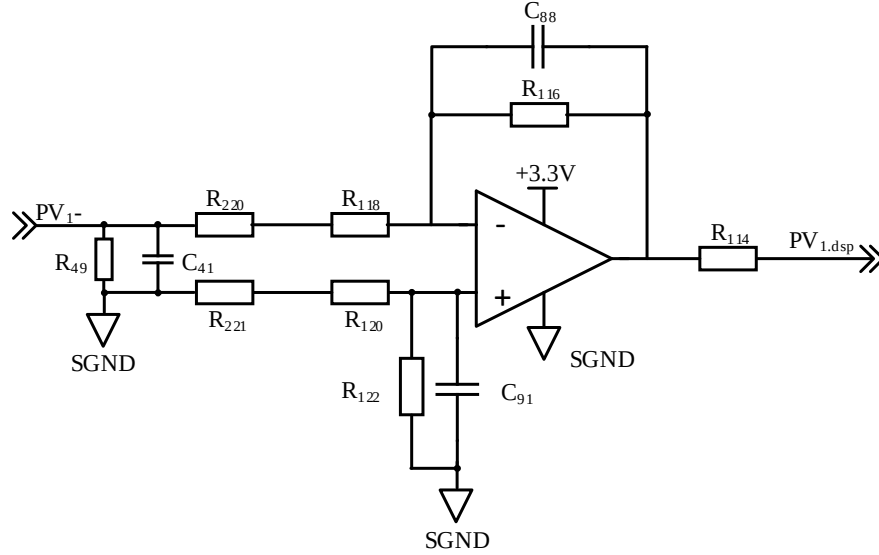


Figure 3.32: Current Sampling Circuit of the Photovoltaic Module

The relationship between the actual output current I_{pv1} of photovoltaic module PV_1 and the sampling signal $I_{pv1.dsp}$ is expressed as:

$$U(I_{pv1.dsp}) = U(I_{pv1}) \frac{R_{122}}{R_{120} + R_{122}} \times \frac{R_{118} + R_{116}}{R_{118}} = (I_{pv1} \times R_{49}) \frac{R_{122}}{R_{120} + R_{122}} \times \frac{R_{118} + R_{116}}{R_{118}}$$

Equation 3.44

iii. Current sampling of the MOSFET

The MOSFET current sampling circuit is shown in Figure 3.33. The two flyback circuits of the interleaved microinverter are completely identical, and similarly, the current sampling circuits of the MOSFET are also identical. The output terminals CT1+ and CT1- (or CT2+ and CT2-) in Figure 3.33 are the two output terminals of the Current sense

Transformer (CT) connected in series with the MOSFET. The selected CT model is FC-SCT5.0. According to the application manual of this CT, its output current is 1/100 of the current flowing through its input side (i.e., the MOSFET current, I_{Q1} or I_{Q2}). Combined with this sampling circuit, the relationship between the MOSFET current I_{Q1} (or I_{Q2}) and its corresponding sampling signal sent to the DSP is as follows:

$$U(I_{Q1.dsp}) = I_{Q1} \times \frac{1}{100} \times (R_{79} // (R_{76} + R_{78})) \times \frac{R_{78}}{R_{76} + R_{78}} \times \frac{R_{71} + R_{73}}{R_{73}} + U(0.5V) \times \frac{R_{76}}{R_{76} + R_{78}} \times \frac{R_{71} + R_{73}}{R_{73}} \quad \text{Equation 3.45}$$

$U(I_{Q1.dsp})$ is the voltage signal corresponding to the MOSFET current sent to the DSP, where I_{Q1} is the current flowing through the MOSFET, and $U(0.5)$ is the actual voltage corresponding to the auxiliary power output voltage of 0.5 V (due to the possible error between the actual and designed values of the auxiliary power supply voltage, the actual value should be used here).

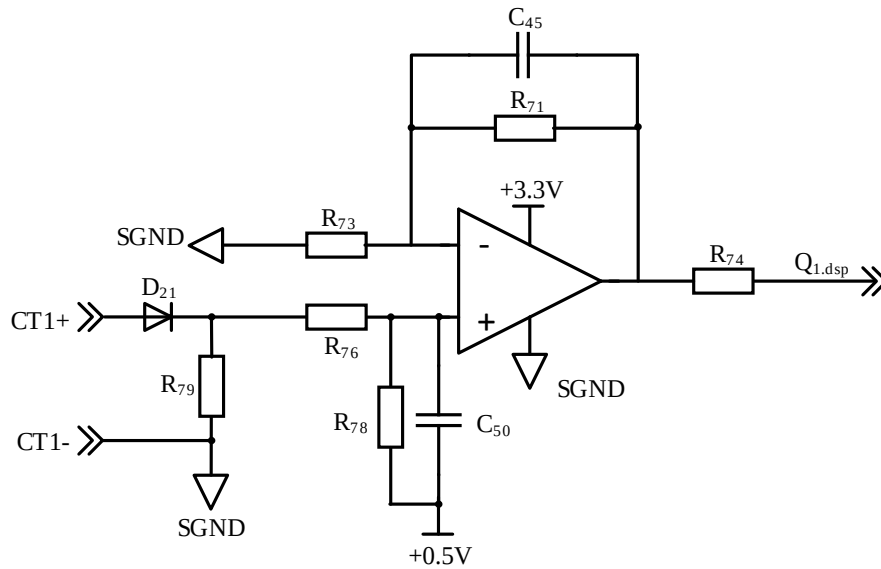


Figure 3.33: Current Sampling Circuit of the MOSFET

iv. Voltage sampling of the flyback output

The voltage sampling circuit on the flyback output side is shown in Figure 3.34. The relationship between the flyback output voltage $U_{flyback}$ and its corresponding sampling signal $U_{flyback.dsp}$ sent to the DSP is as follows:

$$U_{flyback.dsp} = U_{flyback} \times \frac{R_{163}}{R_{72} + R_{83} + R_{163}} \times \frac{R_{70} + R_{68} + R_{158}}{R_{70} + R_{68}} + U(1.65V) \times \frac{R_{72} + R_{83}}{R_{72} + R_{83} + R_{163}} \times \frac{R_{70} + R_{68} + R_{158}}{R_{70} + R_{68}} \quad \text{Equation 3.46}$$

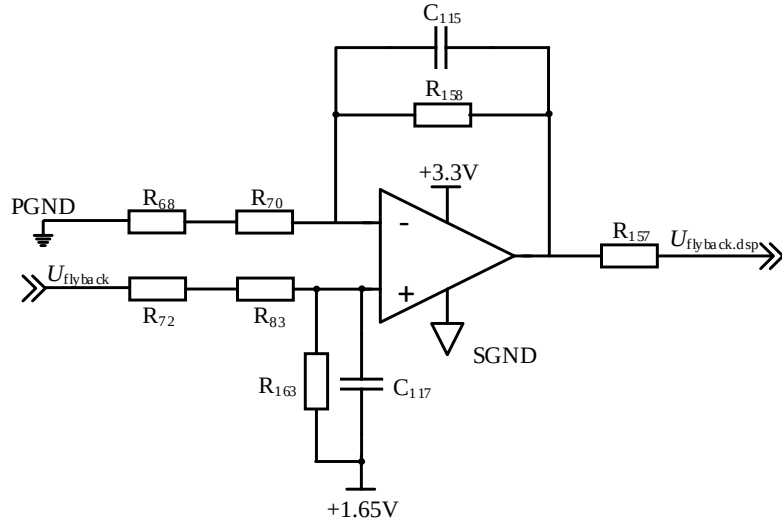


Figure 3.34: Voltage Sampling Circuit of Flyback Output

v. Grid voltage and zero-crossing signal sampling

The grid voltage sampling circuit and the grid voltage zero-crossing signal detection circuit are shown in Figure 3.35 and Figure 3.36, respectively. Since the forms of the grid voltage sampling circuit and the flyback output voltage sampling circuit are completely identical, the equation relationships of the two are also completely identical, as follows:

$$U_{gp.dsp} = U_{gp} \times \frac{R_{195}}{R_{93} + R_{94} + R_{195}} \times \frac{R_{86} + R_{87} + R_{183}}{R_{86} + R_{87}} + U(1.65V) \times \frac{R_{93} + R_{94}}{R_{93} + R_{94} + R_{195}} \times \frac{R_{86} + R_{87} + R_{183}}{R_{86} + R_{87}} \quad \text{Equation 3.47}$$

where U_{gp} is the grid voltage and $U_{gp,dsp}$ is the sampling signal of the grid voltage corresponding to the input to the DSP.

The output signal processed by the sampling circuit of the grid voltage in Figure 3.35 is directly sent to the DSP on one hand, and on the other hand, it is sent to the zero-crossing signal detection circuit (Figure 3.36) to obtain the zero-crossing signal of the grid voltage.

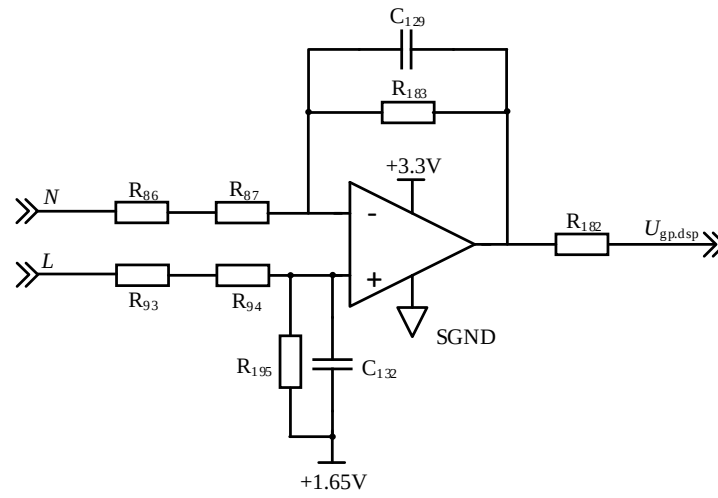


Figure 3.35: Grid Voltage Sampling Circuit

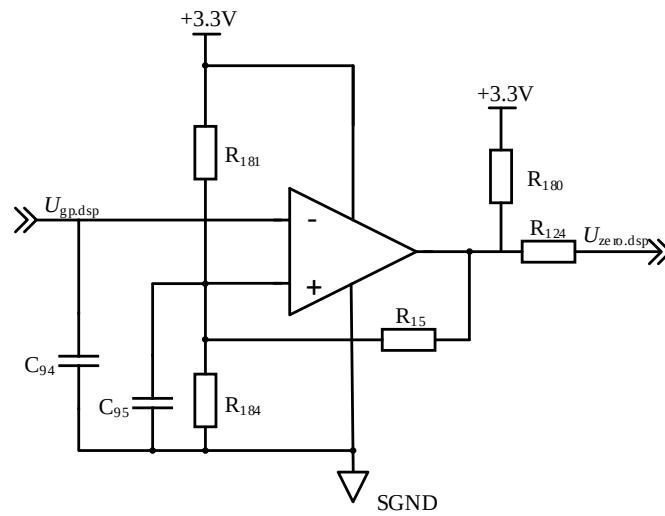


Figure 3.36: Zero-Crossing Signal Detector Circuit

Since there may be oscillating ripples near the zero-crossing point of the grid voltage, to accurately detect the zero-crossing signal, the influence of ripples on the accuracy of zero-crossing detection can be reduced by adding the hysteresis loop action. The size of the hysteresis can be adjusted by changing the resistance values of R_{181} , R_{184} and R_{15} . The hysteresis width Δ can be represented by the following equation:

$$\Delta = U(+3.3V) \times \left(\frac{R_{184}}{R_{181} // R_{15} + R_{184}} - \frac{R_{184} // R_{15}}{R_{181} + R_{184} // R_{15}} \right) \quad \text{Equation 3.48}$$

where $U(+3.3V)$ is the actual voltage corresponding to the auxiliary power output voltage of +3.3 V (due to the possible error between the actual and designed values of the auxiliary power supply voltage, the actual value should be used here).

vi. Grid-Connected Current Sampling

The grid-connected current sampling circuit is shown in Figure 3.37.

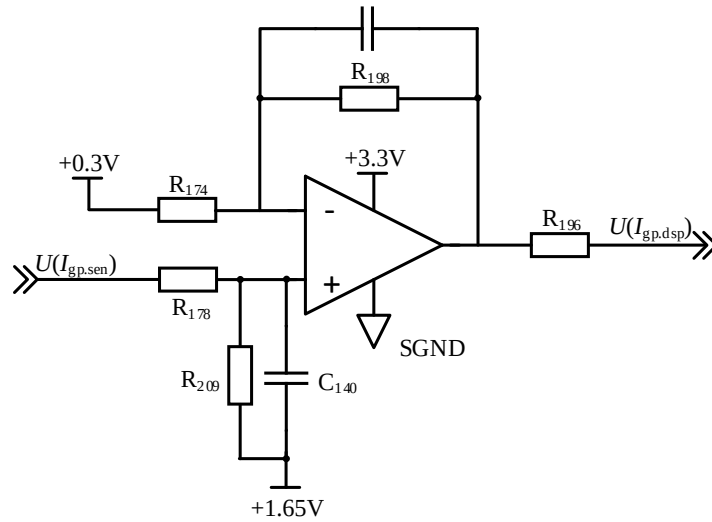


Figure 3.37: Sampling Circuit of Grid-Connected Current

The input signal $U(I_{gp.sen})$ of the grid-connected current sampling circuit is the voltage signal of the actual grid current I_{gp} after being processed by the Hall circuit sensor STK-03HD/S. According to the manual of the STK-03HD/S chip, the relationship between the sampling input current I_{gp} of the chip and the output voltage signal $U(I_{gp.sen})$ of the chip can be represented as follows:

$$U(I_{gp.sen}) = 0.18I_{gp} + 2.6 \quad \text{Equation 3.49}$$

The relationship between the output voltage signal $U(I_{gp.sen})$ of STK-03HD/S and its sampling signal $I_{gp.dsp}$ is as follows:

$$U(I_{gp.dsp}) = U(I_{gp.sen}) \times \frac{R_{209}}{R_{178}+R_{209}} \times \frac{R_{198}+R_{174}}{R_{174}} + U(0.3V) \times \frac{R_{198}}{R_{174}} \quad \text{Equation 3.50}$$

where $U(I_{gp.dsp})$ is the voltage signal corresponding to the grid-connected current sampling signal $I_{gp.dsp}$ sent to the DSP.

In Equation 3.49 and Equation 3.50, the relationship between the grid-connected current and its corresponding sampling signal input to the DSP is given as follows.

$$U(I_{gp.dsp}) = (0.18I_{gp} + 2.6) \times \frac{R_{209}}{R_{178}+R_{209}} \times \frac{R_{198}+R_{174}}{R_{174}} + U(0.3V) \times \frac{R_{198}}{R_{174}} \quad \text{Equation 3.51}$$

3.6.1.5 Design of the Driver Circuits

i. MOSFET driver circuit of the DC–DC conversion unit

The MOSFET driver in the flyback circuit can be implemented using a chip with low-side driver functionality. In this research, the NSD1025-DSPR produced by the Novosns Company in China was used, and its driving circuit is shown in Figure 3.38.

PWM1A and PWM1B are the signals generated by the DSP chip and passed through a high-speed four-channel digital isolator. MOS1A and MOS1B are the driving signals connected to the gate terminals of the MOSFETs in the main and auxiliary circuits.

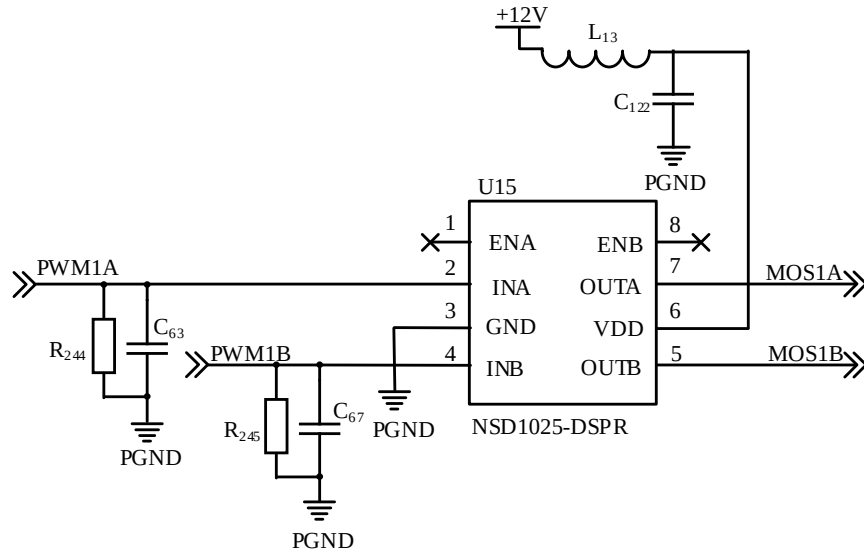


Figure 3.38: MOSFET Driver Circuit of the DC-DC Conversion Unit

ii. Thyristor driver circuit of the DC–AC conversion unit

The thyristor is a kind of semicontrolled device for current control, and the triggering pulse generated by the trigger circuit should have sufficient amplitude and width to ensure reliable conduction of the thyristor (Shu et al., 2020). This thesis selected the optically coupled bidirectional thyristor drive chip OR-M3053, and its driver circuit diagram is shown in Figure 3.39.

The circuits for the other three thyristors are the same. The signal PWM_s is the corresponding thyristor driving signal sent out by the DSP, and the M and N terminals are the anode and cathode of the corresponding thyristor, respectively.

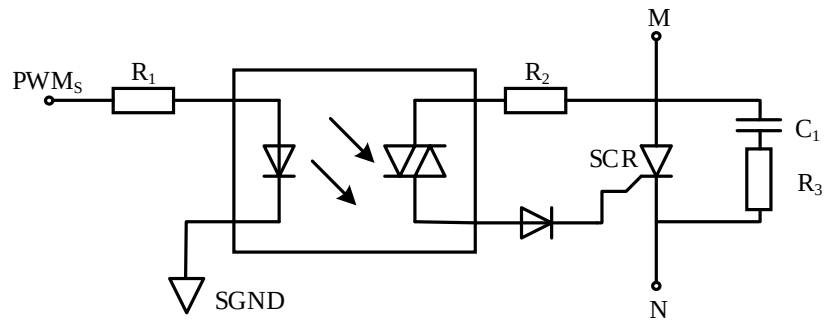


Figure 3.39: Thyristor Driver Circuit

3.6.2 Design of Software Processes

The overall function of the software includes the MPPT program for photovoltaic module output, the PLL program, fault detection, and protection. The PLL algorithm and MPPT algorithm are introduced in Section 3.5. In this section, based on flowcharts of program submodules, the implementation processes of other functions are sequentially introduced.

3.6.2.1 Main Program and State Machine

The software flowchart for the main program is shown in Figure 3.40. To control the system, it is necessary to firstly initialize the DSP chip, configure the functional modules into the corresponding operating mode, and then judge the system state based on the sampled data to determine the system operating state. This involves executing the state machine loop subprogram and ADC interruption subprogram, while also determining whether the conditions for executing MPPT algorithm are met and updating the reference current or reference voltage. The condition for executing MPPT algorithm is a 100 ms loop, meaning MPPT algorithm is executed once every 100 ms.

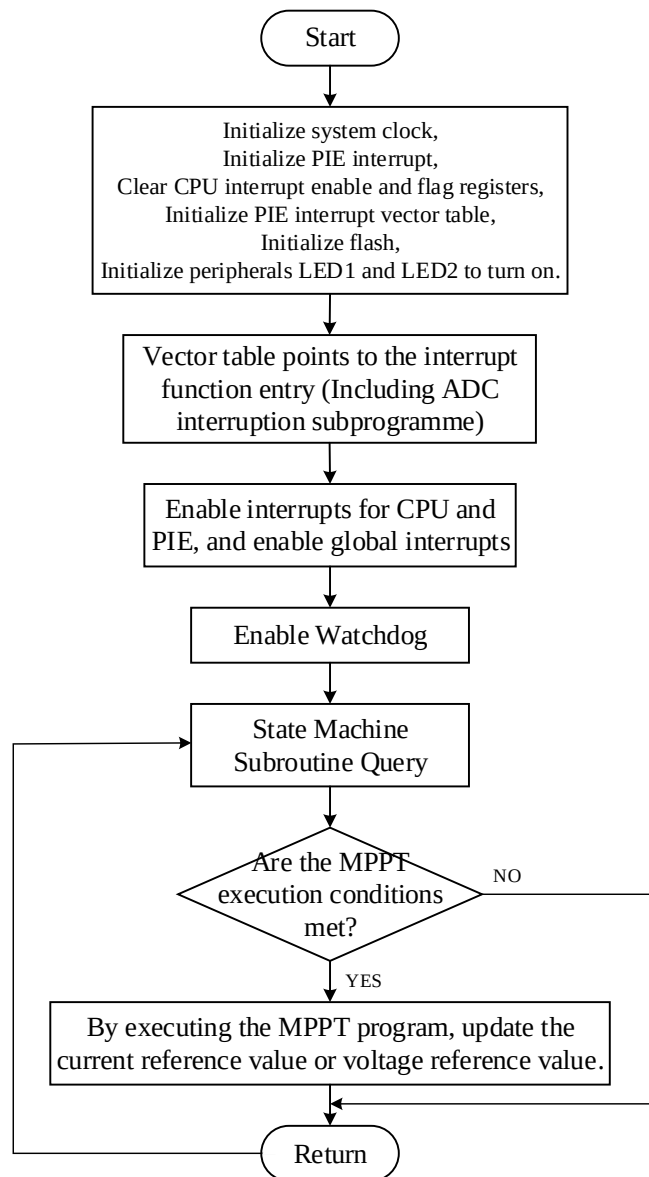


Figure 3.40: Software Fowchart of the Main Program

The software flowchart for the state machine loop subprogram is shown in Figure 3.41. The system states are divided into "Startup", "Error", and "Normal", each corresponding to LED displays and work descriptions, as shown in Table 3.4.

Once the system is powered up and initialized successfully, the system state is set to "startup." Then, depending on whether the system detects the corresponding fault and

whether the preset switch time has been reached, the system switches between these three states.

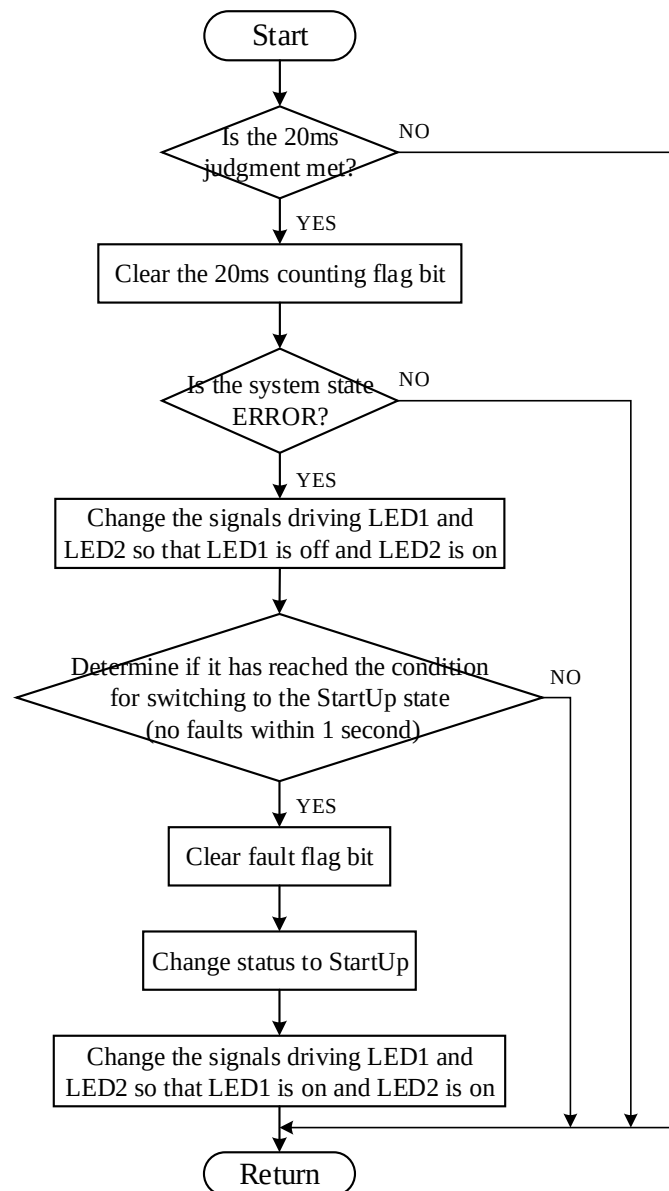


Figure 3.41: Software Flowchart for the State Machine Loop Subprogram

Due to the different requirements for the speed of state switching in different system states, the transition from the "Fault" state to the "Normal" state can be slower, while the transition from the "Normal" state to the "Fault" state must be executed immediately.

Therefore, in the slow-execution state machine loop program, only the function of the transition from the "Fault" state to the "Normal" state is executed, while the implementation of the function of the transition from the "Normal" state to the "Fault" state is placed in the fast-execution ADC interrupt fault diagnosis subroutine.

The decision making box "Is the 20 ms judgment met" Figure 3.41 means that the system scans the state machine every 20 ms to determine whether the conditions for switching from the "Error" state to the "Normal" state are met. During this process, if the ADC interruption subprogram detects a fault, it will immediately take protective measures.

Table 3.4: Three States of the State Machine

State Machine	LED Display	Description of Work Status
Startup	LED1 on, LED2 on.	Entering after initialization is complete.
Normal	LED1 blinking, LED2 off.	All functions are running normally, LED1 blinks once in the ADC program.
Error	LED1 off, LED2 on.	Entering this state when a fault occurs.

3.6.2.2 ADC Interruption Subprogram

The software flowchart of the ADC interrupt subprogram is shown in Figure 3.42. The ADC interrupt subprogram is executed once every two flyback PWM cycles, mainly to realize the reading and processing of sampled data results, fault detection and handling, updating the PWM module compare register for updating the duty cycle, and so on.

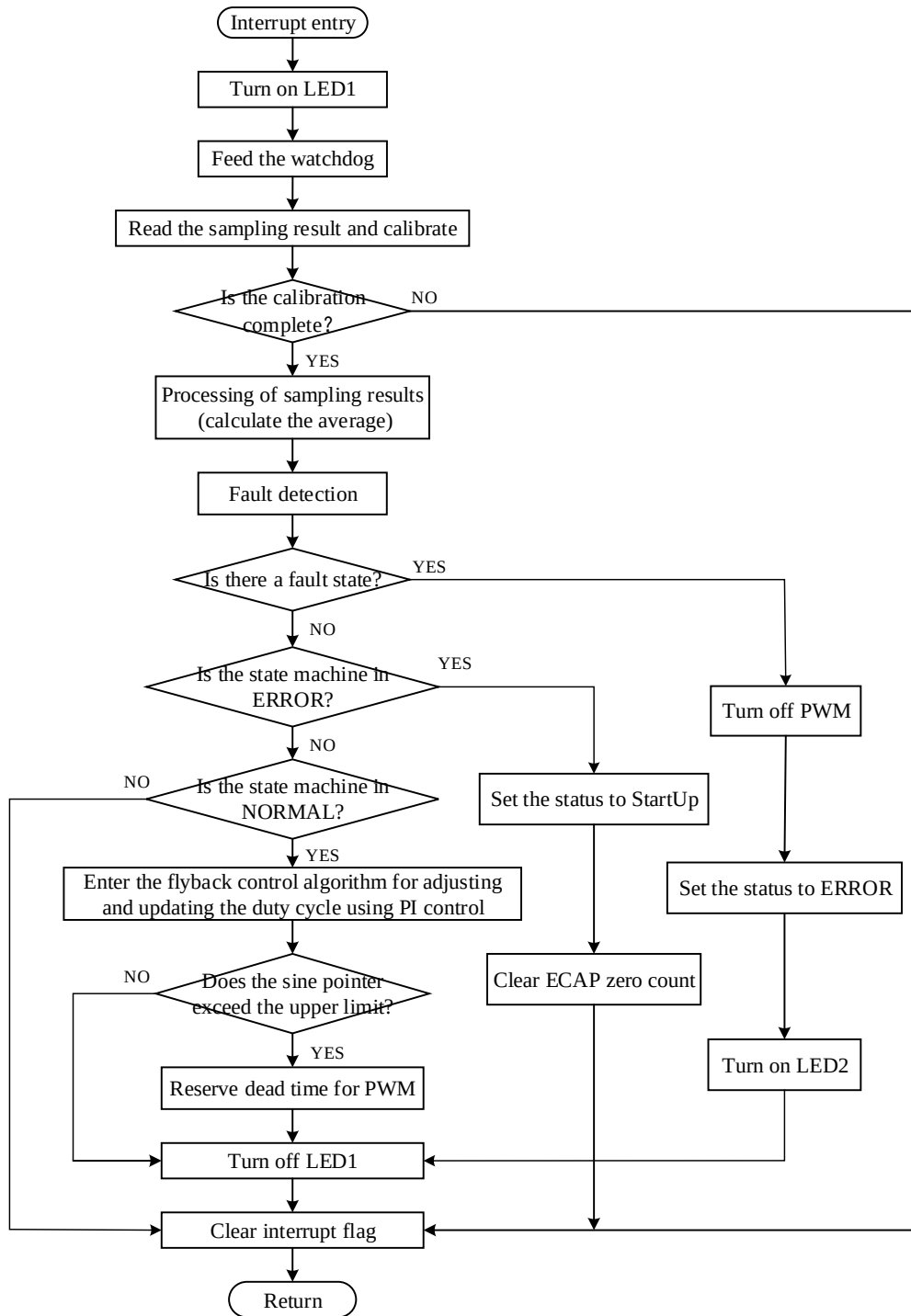


Figure 3.42: Software Flowchart of the ADC Interrupt Subprogram

3.7 Summary

The construction and development process of the model and experimental platform for photovoltaic grid-connected microinverters is presented in this chapter, which is mainly

composed of the topology structure and control strategy. For topology structure, this chapter established a conventional topology model and completed parameter selection. Through simulation analysis and verification, the correctness of the topology has been validated. Then, improvements were made by adding compensation capacitors and introducing passive clamping technology to obtain the final interleaved passive clamping flyback topology structure. Various parameters were determined, and the working principles were detailed, providing a model basis for subsequent simulation result analysis. Furthermore, a novel multi-valley turn-on control strategy was proposed that introduces parameter extraction methods, including the MPPT and PLL algorithms. The feasibility of the algorithms was verified through simulation. Additionally, an accurate equation for the reference current curve was derived in detail, and the implementation process of the control strategy was elucidated based on the curve equation. Finally, the entire experimental control platform of the microinverter was constructed. The design and selection of various hardware and software modules within the microinverter were described in detail, providing theoretical support for building the final experimental prototype and conducting experimental verification.

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Introduction

In Chapter 3, improvements to the topology structure, development of the control strategy, and establishment of the experimental framework were discussed to enhance the performance of the microinverter. This chapter provides a detailed analysis of the simulation waveforms and experimental results. Firstly, Section 4.2 divides the topology structure into three parts—a single-ended flyback topology with a compensation capacitor, a single-ended passive clamping flyback topology, and an interleaved parallel passive clamping flyback topology—and analyses the simulation performance of the three topologies in a progressive manner. Then, based on the MPPT algorithm and SOGI-PLL algorithm designed in Chapter 3, Section 4.3 details the simulation results for the novel multi-valley turn-on control strategy and compares its efficiency and harmonic content with those of the fixed-frequency control strategy. Finally, Section 4.4 implements the system framework designed in Chapter 3, introduces the prototype of the microinverter and the experimental platform, and experimentally validates the correctness of the simulation.

4.2 Topology Structure

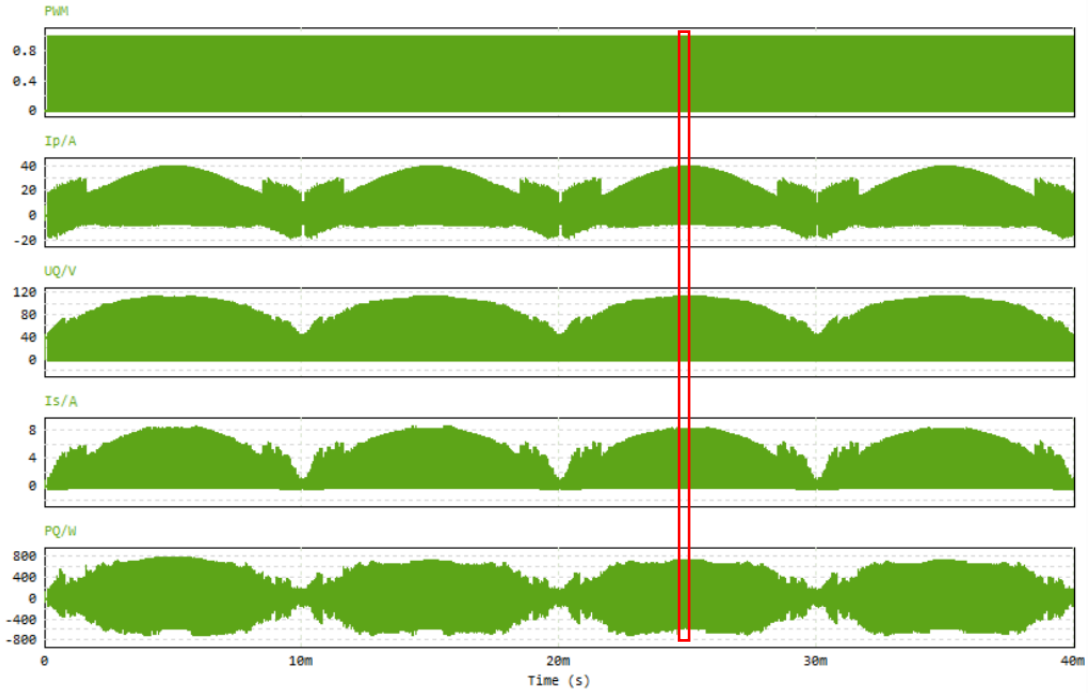
Based on the theoretical analysis results in Section 3.4.2, an improved topology model was constructed in PSIM software to simulate a microinverter operating in DCM, validating the correctness of the theoretical analysis and design. Next, the model is divided

into three parts: a single-ended flyback topology with compensation capacitors, a single-ended passive clamping flyback topology, and an interleaved parallel passive clamping flyback topology. The simulation results are analysed and compared.

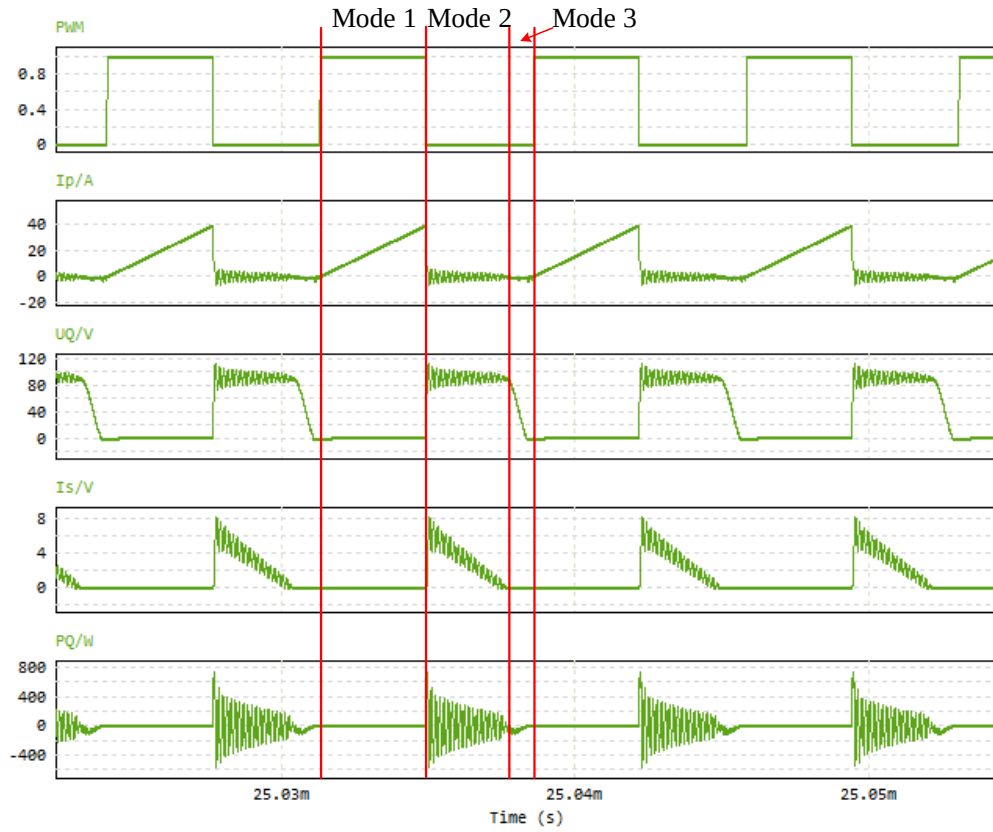
4.2.1 Single-Ended Flyback Topology with a Compensation Capacitor

i. Waveform Analysis of the Three Modes

Figure 4.1 presents several key waveforms of the single-ended flyback topology based on the multi-valley turn-on control strategy in DCM. Figure 4.1 (a) shows the overall waveforms, while Figure 4.1 (b) provides a detailed view within the red box in the overall waveforms. I_P represents the primary current of the transformer, U_Q is the drain-source voltage of the MOSFET Q , and I_s is the secondary side current of the transformer. P_Q is the instantaneous power loss of MOSFET Q .



(a) Overall Waveforms



(b) Detailed Waveforms

Figure 4.1: Key Waveforms of Single-Ended Flyback Topology

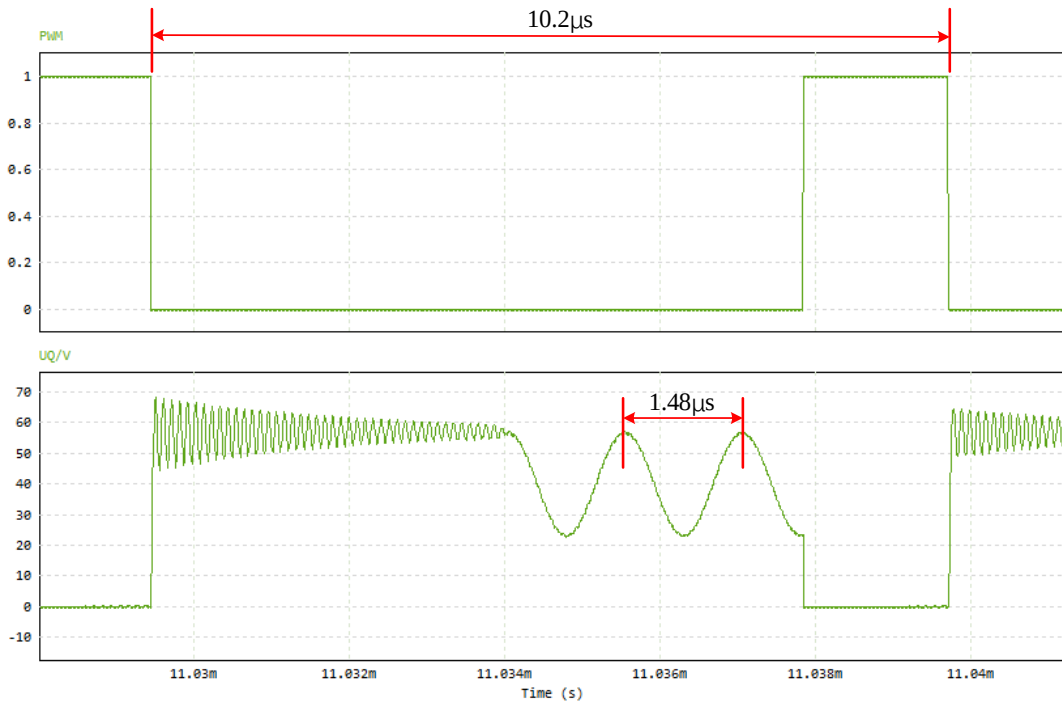
The detailed view revealed three modes within one period. In mode 1, MOSFET Q is turned on, and the primary current rises linearly from 0A to about 40 A, at this time, the source-drain voltage U_Q of MOSFET Q , the power loss P_Q and the secondary current I_s are all 0. In mode 2, MOSFET Q is turned off, and the source-drain voltage U_Q oscillates and stabilises around 92V. Due to the existence of parasitic capacitance of the MOSFET Q , there is a power loss at this time. Meanwhile, due to the flyback transformer, the energy is transferred from the primary side to the secondary side until it is all transferred to the grid. In mode 3, the disappearance of the clamp voltage causes fluctuations in the drain-source

voltage and leads to a large amplitude of resonance. But due to the existence of the parasitic diode, the source-drain voltage will not be less than 0 V.

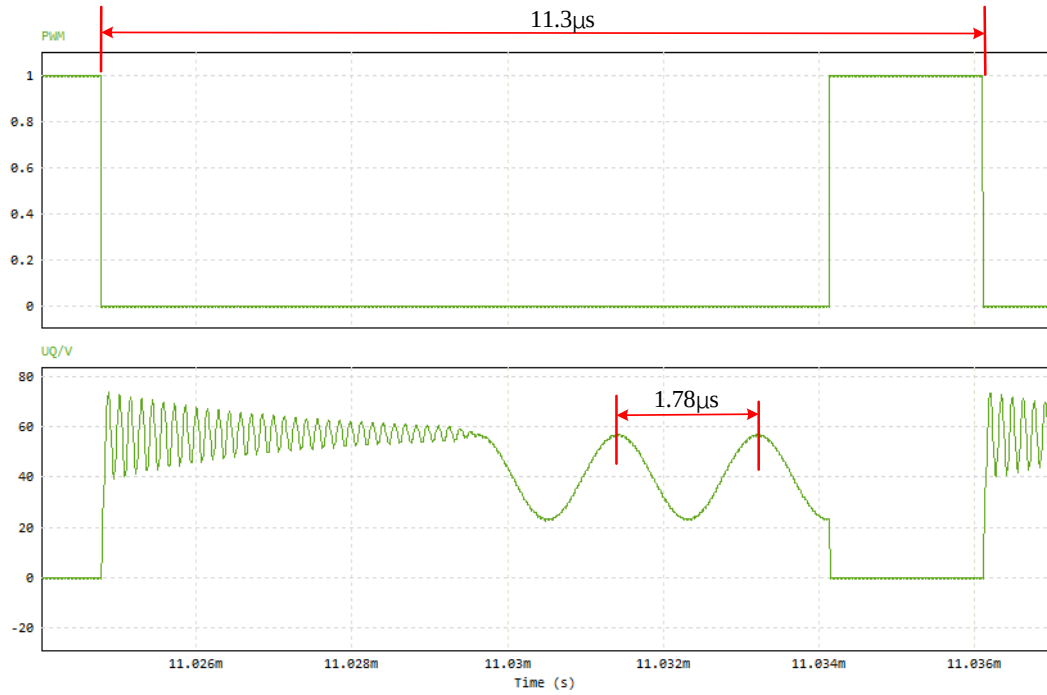
From the waveforms, it can be observed that the simulation results align with the theoretical mode analysis.

ii. Comparison of Resonance Periods

Figure 4.2 (a) and Figure 4.2 (b) present the relevant waveforms of MOSFET Q in two topologies, without and with the compensation capacitor, respectively, at a certain approximate moment when the grid phase angle is small. The *PWM* is the drive signal of MOSFET Q, and U_Q is the drain-source voltage of MOSFET Q.



(a) Voltage across MOSFET Q without a Compensation Capacitor



(b) Voltage across MOSFET Q with a Compensation Capacitor

Figure 4.2: Voltage across the Switch before and after Adding Compensation Capacitor

The resonant periods of Mode 3 are different. The resonant period without the compensation capacitor is measured as $2.96 \mu\text{s}$, with a switching period of $10.2 \mu\text{s}$. Moreover, with the compensation capacitor, the resonant period extends by 20.27% to $3.56 \mu\text{s}$, and the switching period increases to $11.3 \mu\text{s}$, an extension of 10.78%. It can be concluded that the addition of compensation capacitor effectively increases the resonance period, reduces the switching frequency, and resolves the issues of high switching frequency and high loss.

iii. Optimal Value of the Compensation Capacitor

Figure 4.3 lists the average power loss of MOSFET Q within the grid cycle during the simulation process, with an absorption capacitor C_s of 220 pF and different values of

compensation capacitor C_x . When C_x is 15 nF, the power loss of the transistor Q is the lowest at 0.2753 W. This parameter is used for the construction of the experimental platform.

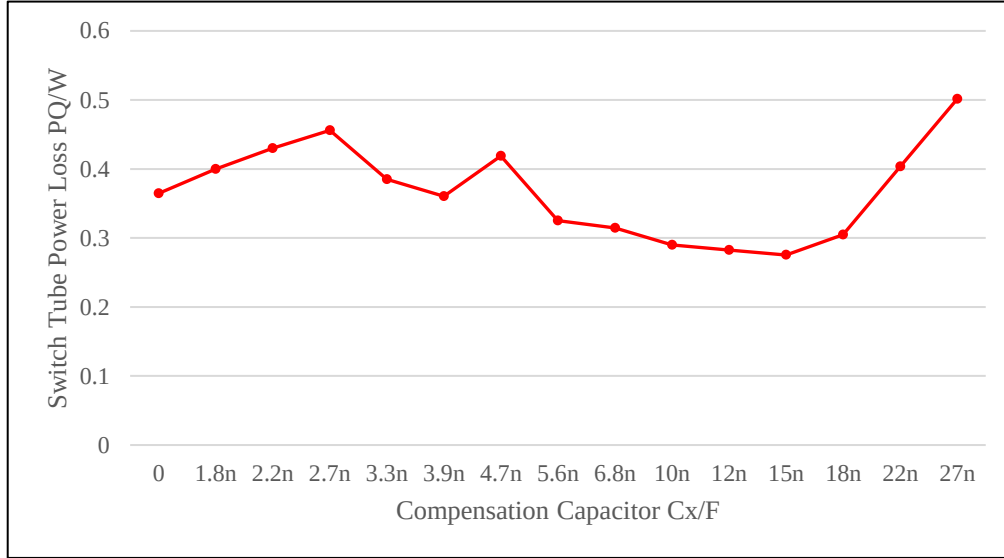


Figure 4.3: Transistor Power Loss with Different C_x

4.2.2 Single-Ended Passive Clamping Flyback Topology

i. Waveform Analysis of the Six Modes

Figure 4.4 presents several key waveforms of the single-ended passive clamping flyback topology. PWM is the driving signal of MOSFET Q , U_Q is the drain-source voltage of Q , U_{Cp} is the voltage of the snubber capacitor C_p , and I_P is the primary current of the transformer.

In mode 1 and mode 2, the MOSFET Q turns off, the drain-source voltage U_Q of Q and the voltage U_{Cp} of the snubber capacitor C_p increase linearly because of the leakage inductance, and the clamp circuit conducts. While the transformer energy is transferred from the primary side to the secondary side. In mode 3, U_Q oscillates at 64V, U_{Cp} stabilises at

about 13V, the clamp circuit remains stable. At this time, the flyback output side supplies energy to the grid. In mode 4, the clamp circuit continues to work, but due to the disappearance of the clamp voltage from the secondary side, it will cause a larger oscillation across the MOSFET Q . In mode 5, the MOSFET Q turns on, the reset circuit operates, the snubber capacitor C_p discharges, and U_{Cp} drops to -8 V. In mode 6, the reset circuit stops operating, and the primary-side current rises, waiting for the next cycle.

Figure 4.4 annotates six modes within one period, and the simulation results align with the theoretical mode analysis.

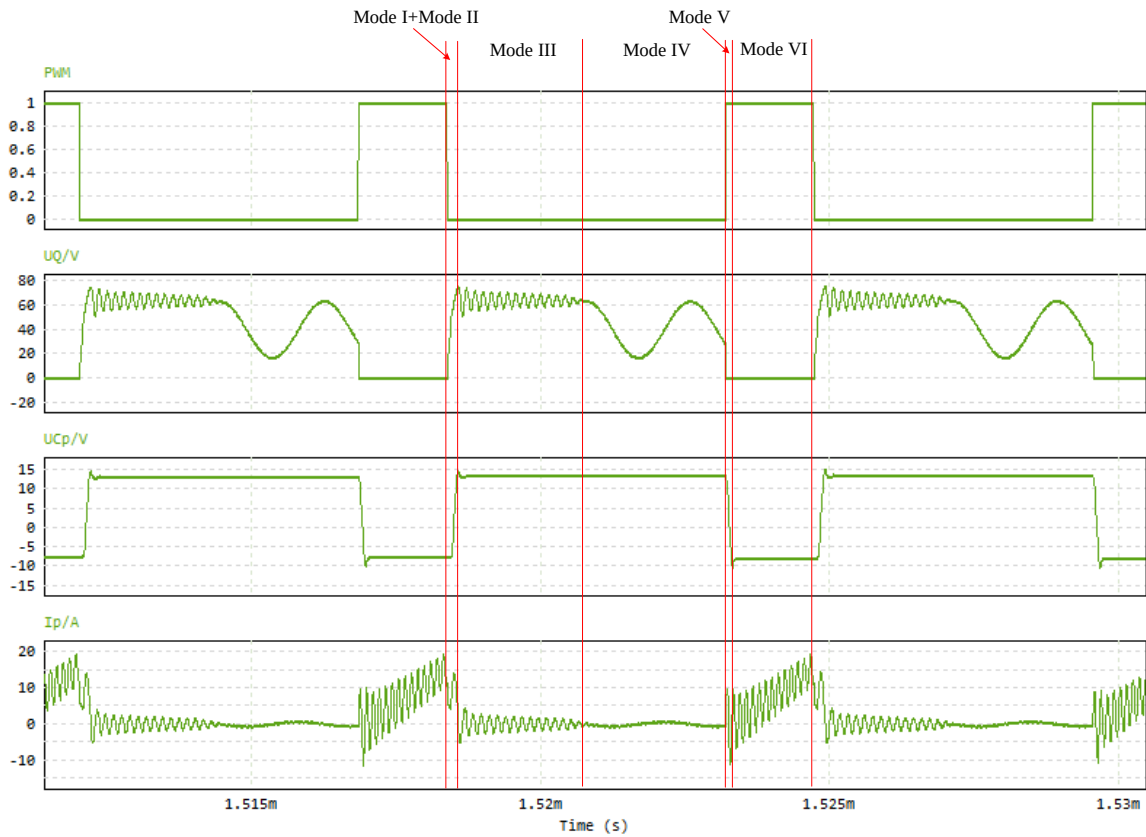
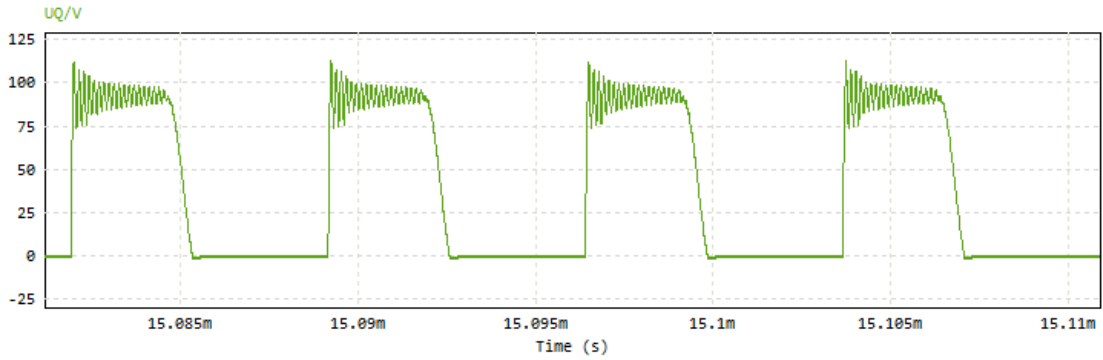


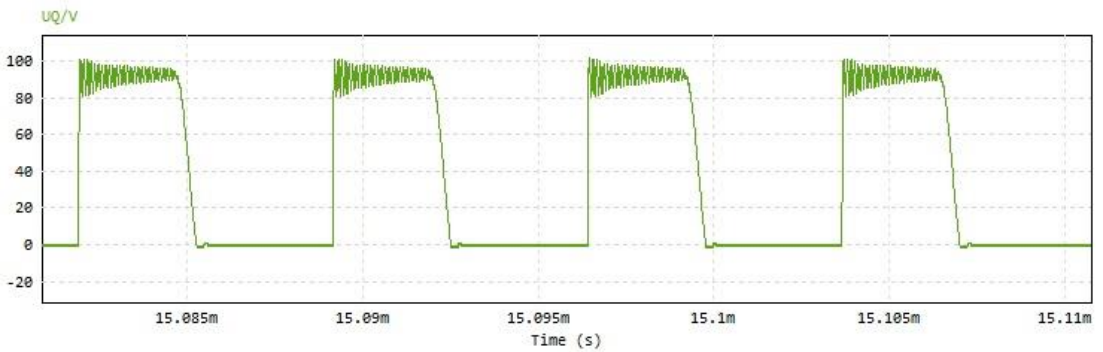
Figure 4.4: Key Waveforms of Single-Ended Passive Clamping Flyback Topology

ii. Comparison of the Voltage Spikes

The effectiveness of the passive clamping circuit was verified. The drain-source voltage waveforms of MOSFET Q before and after the addition of the passive clamping circuit in the same phase of the power grid are compared. As shown in Figure 4.5, when Q is off, the drain-source voltage of both topologies fluctuates by approximately 90 V. Without the passive clamping circuit, the voltage spike of Q reaches 112 V. After adding the passive clamping circuit, at the same power and voltage level, due to the resonant effect of the clamping circuit, there is absorption and feedback of leakage inductance, reducing the voltage spike of MOSFET Q to 101 V, a decrease of 9.8%.



(a) Drain-Source Voltage Waveform of MOSFET Q without the Clamping Circuit



(b) Drain-Source Voltage Waveform of MOSFET Q with the Clamping Circuit

Figure 4.5: Comparison of the Drain-Source Voltage Waveforms with and without the Clamping Circuit.

iii. Waveform Analysis of the Grid-Connection Unit

Figure 4.6 shows the grid voltage and grid-connected current waveforms of the single-ended passive clamping microinverter with a power of 200 W. The peak grid voltage is 311 V, and the peak grid-connected current is 1.18 A. For comparison with the grid voltage, the current signal is amplified by 50 times. The THD of the grid-connected current is 3.02%, which meets the grid-connected standard. There is distortion in the grid current near the zero-crossing point. Zhang et al. (2021) suggested that this is caused by the filtering capacitor leading the current ahead of the voltage, while Miao et al. (2019) attributed this to the turn-off delay of the switch device. Therefore, considering the specific causes of distortion is one of the future research directions.

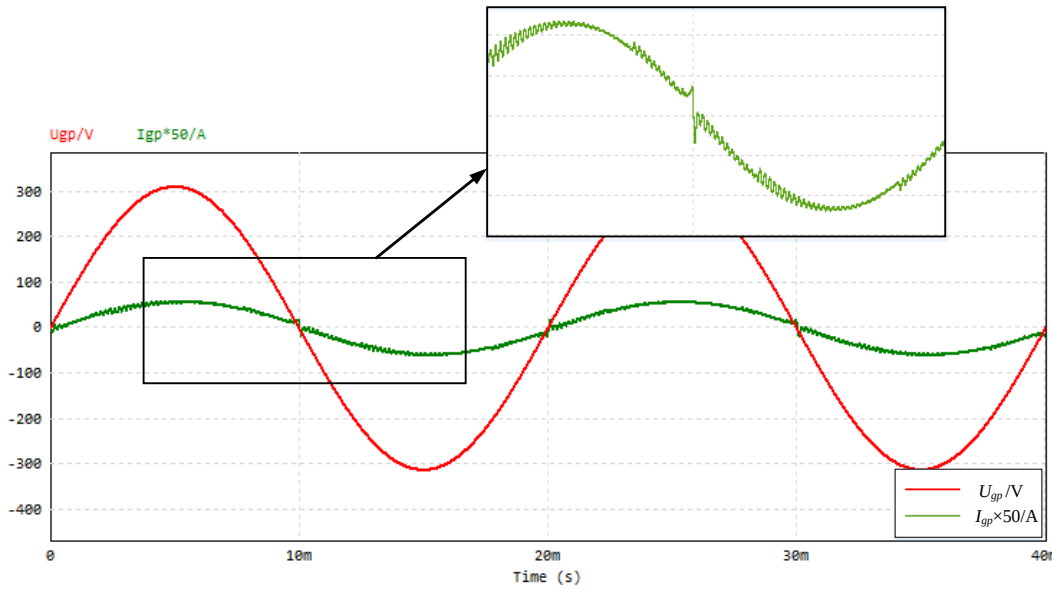


Figure 4.6: Grid Voltage and Grid-Connected Current Waveforms of the Single-Ended Passive Clamping Flyback Microinverter

4.2.3 Interleaved Parallel Flyback Topology

i. Waveform Analysis of the Grid-Connection Unit

Figure 4.7 shows the grid voltage and grid-connected current waveforms of the interleaved flyback topology. Similarly, the current signal is amplified by 50 times.

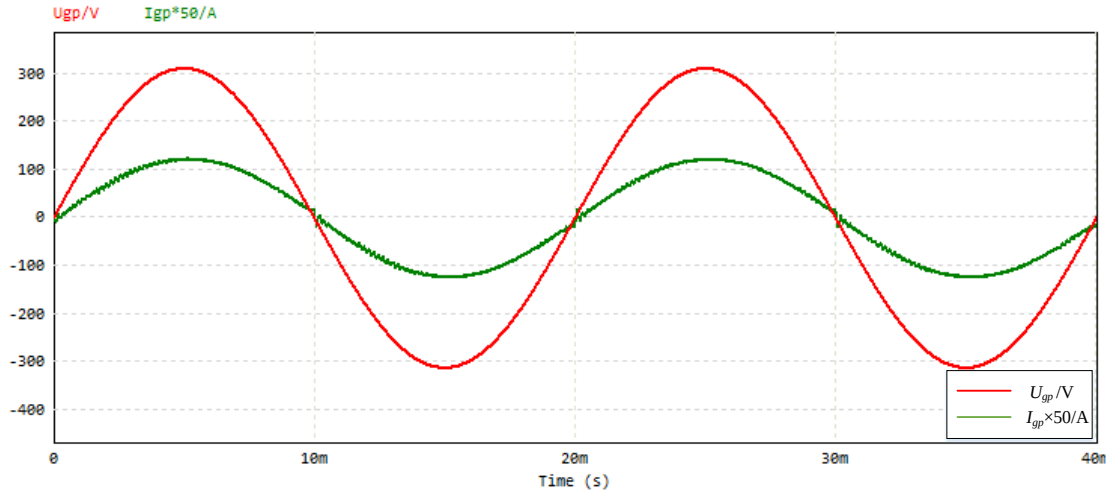


Figure 4.7: Waveforms of the Grid Voltage and Grid-Connected Current of the Interleaved Flyback Topology

The peak value of the grid-connected current is 2.46 A, approximately twice that of the single-ended flyback topology. After FFT analysis, the THD was found to be 2.11%, which is smoother than that of the single-ended flyback topology, resulting in a reduction of 0.91% in the harmonic content.

ii. Waveform Analysis of the DC–DC Conversion Unit

Figure 4.8 shows the primary current and total current for each flyback converter. From top to bottom, they are the primary side current I_{p1} of the main flyback converter, the

primary side current I_{p2} of the auxiliary flyback converter, and the total primary side current I_p . The currents of the two flyback converters do not affect each other and are independent.

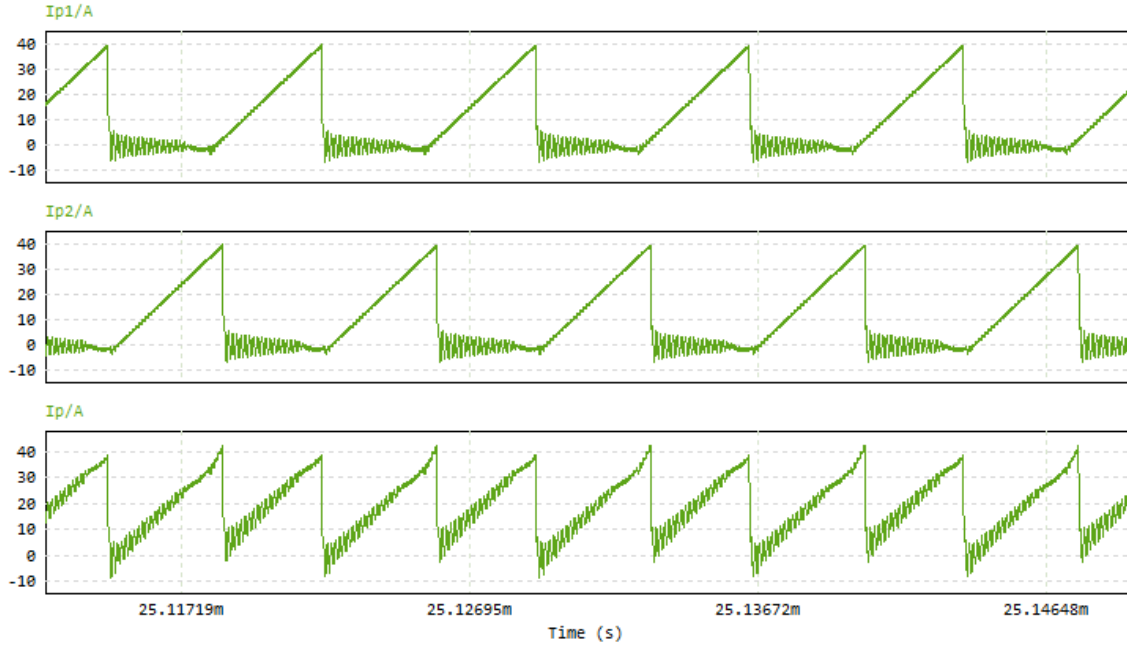


Figure 4.8: Primary Currents of Interleaved Flyback Topology

Figure 4.9 and Figure 4.10 present several key waveforms of the interleaved flyback topology. Figure 4.9 shows the overall waveforms, while Figure 4.10 provides a detailed view within the red box in the overall waveforms, including the driving signals $PWM1$ and $PWM2$ of the main and auxiliary circuits, the drain-source voltages U_{Q1} and U_{Q2} of the main MOSFET Q_1 and the auxiliary MOSFET Q_2 , the currents I_{Q1} and I_{Q2} through the main MOSFET Q_1 and the auxiliary MOSFET Q_2 , and the secondary currents I_{s1} and I_{s2} through the main circuit and the auxiliary circuit.

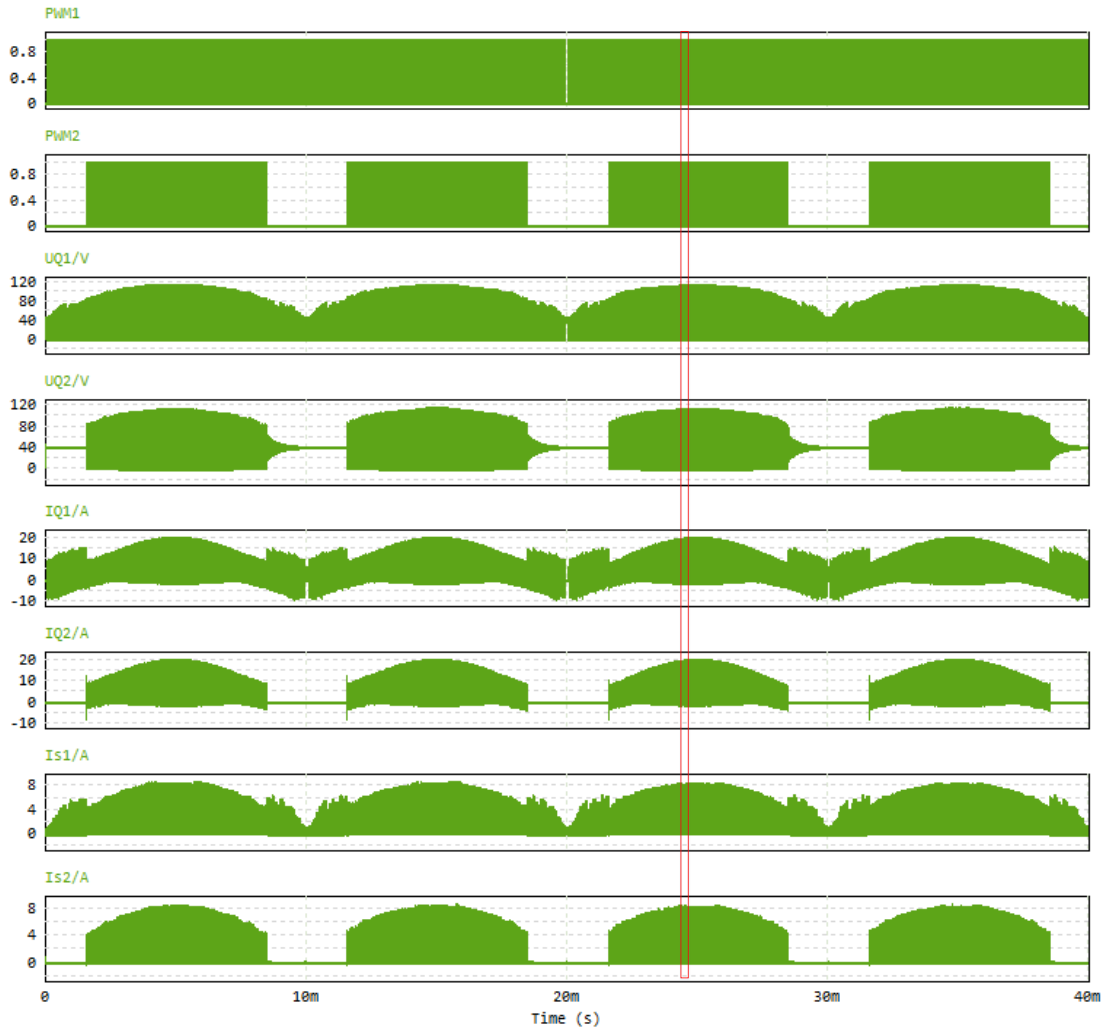


Figure 4.9: Overall Key Waveforms of the Interleaved Passive Clamping Flyback Topology

When the grid phase is relatively low, only the main circuit operates for flyback. When the output power reaches 90 W, as set by the program, the auxiliary circuit also starts operating. The MOSFETs Q_1 and Q_2 of the main and auxiliary circuits alternate on and off, with a switching frequency twice that of the single-ended flyback topology, effectively expanding the power level of the flyback circuit and enhancing its capacity.

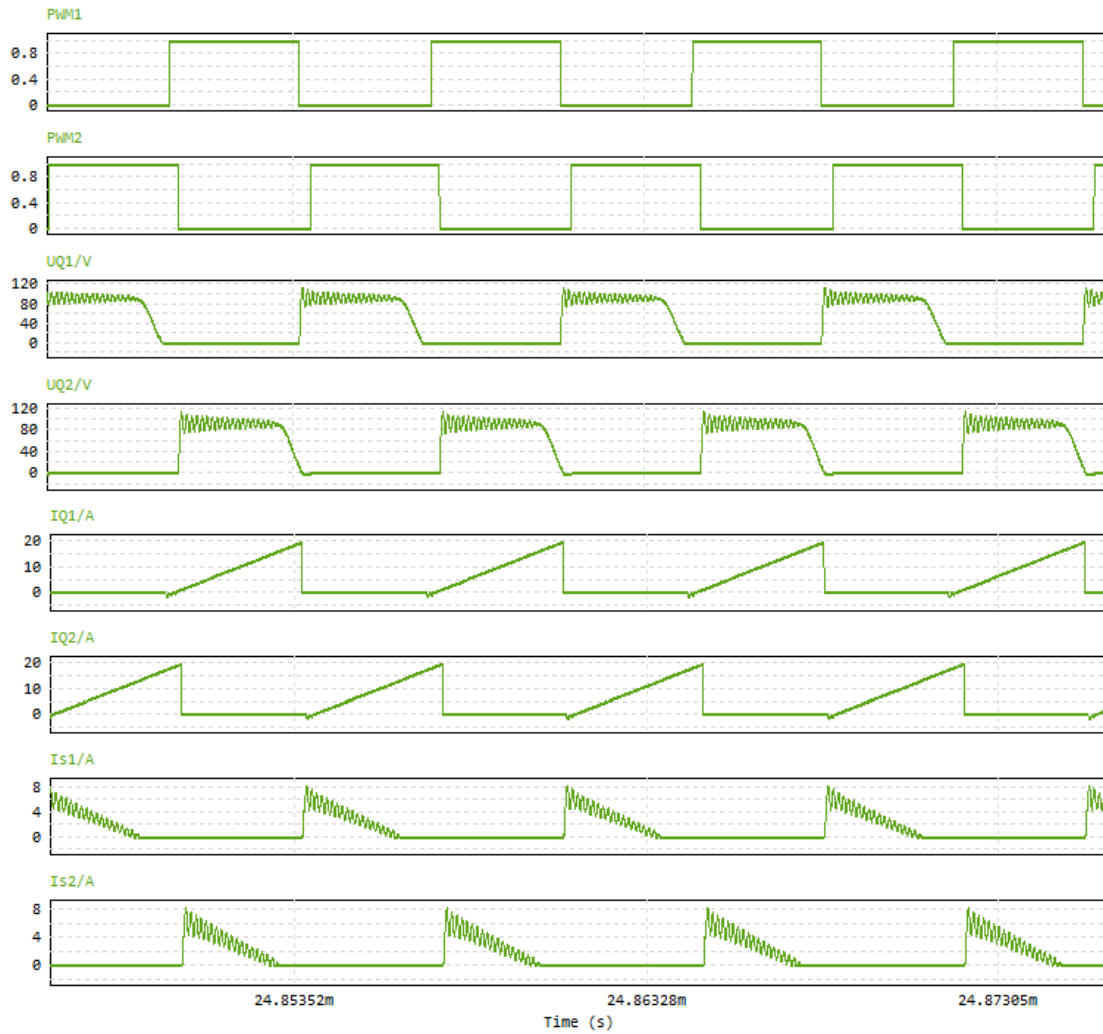


Figure 4.10: Detailed Key Waveforms of the Interleaved Passive Clamping Flyback Topology

iii. Cost Comparison

Table 4.1 lists the numbers of components used in the DC–DC flyback unit with different clamping technologies for interleaved flyback topologies. The diode, capacitor, inductor, and resistor used in the flyback unit have similar prices, while the price of the MOSFET is several times greater than that of these four components.

By comparison, the improved LCD passive clamping circuit proposed in this research has the lowest component cost, with the PCB costing approximately 150 MYR. Compared with active clamping, RCD passive clamping, and dual-transistor passive clamping topologies, it reduces two switching transistors, saving about 4 MYR. Compared with the traditional LDC passive clamping circuit, it reduces one high-voltage diode, saving approximately 1 MYR, resulting in a cost reduction of up to 2.67%.

Table 4.1: ElementNum Comparison of Different Clamping Topologies

Clamping Technology	Author	ElementNum				
		Transistor	Diode	Capacitor	Inductor	Resistor
LCD Passive Clamping	This Research	2	3	2	2	0
PMOS Active Clamping	Kim et al. (2012)	4	0	2	0	0
NMOS Active Clamping	Chen et al. (2023)	4	0	2	2	0
RCD Passive Clamping	Huber et al. (2018)	4	2	2	0	2
LCD Passive Clamping	Wu&Wang (2020)	2	4	2	2	0
Dual-Transistor Passive Clamping	Mo (2012)	4	2	0	0	0

4.3 Multi-Valley Turn-on Control Strategy

According to the analysis of the control strategy in Section 3.5, this section plots the peak current reference curve based on the accurate equation of the peak current and analyses the simulation results of the multi-valley turn-on control strategy to verify the effectiveness of improving the operational efficiency and reducing the harmonic content.

4.3.1 Simulation Results of the Peak Current Reference Curve

As shown in Figure 4.11, the peak current reference curve $I_{\text{ref}}(\theta_g)$ is plotted using MATLAB. The component parameters involved in the derivation process are shown in Table 4.2.

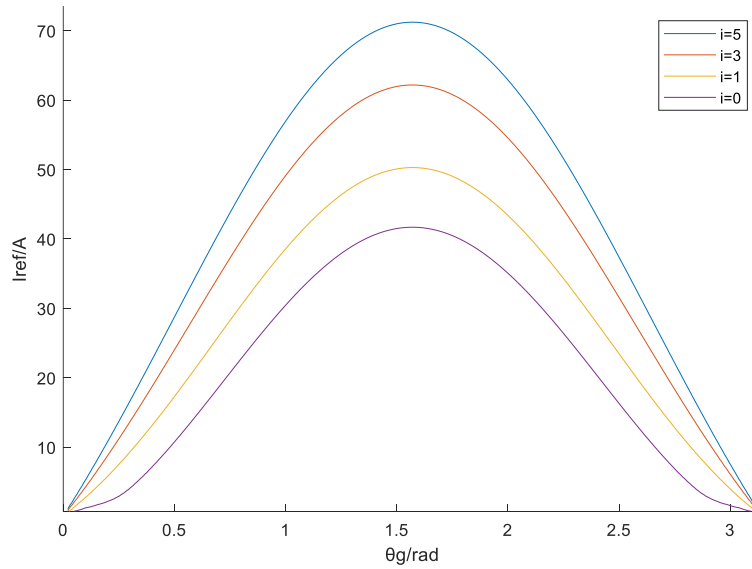


Figure 4.11: Peak Current Reference Curves for Different Numbers of Resonances

In Figure 4.11, the curves of different colours represent the peak curves when the number of resonances is 0, 1, 3, or 5. The introduction of different numbers of resonances has a significant impact on the peak reference curve of the transformer. The more resonances

there are, the larger the peak reference current. When the phase of the grid is $\pi/2$, under normal circumstances, the primary side current I_p is approximately 40 A. The situation with a resonance number of 0 in Figure 4.11 is more consistent with this result. Therefore, it can be inferred that at this point, according to the multi-valley turn-on control strategy proposed in this research, the controller will not increase the number of resonances.

Table 4.2: Component Parameters Required for the Control Strategy

Parameter	Value	Unit
DC input voltage V_{pv}	30	V
AC output voltage peak value $V_{gp,max}$	311	V
Rated output power P	200	W
Ratio of transformer n	2:12	-
Excitation inductance L_m	3.4 u	H
Leakage inductance L_k	34.2 n	H
Distributed capacitor C_T	321.5 p	F
Parasitic capacitor of MOSFET Q C_Q	321.5 p	F
Parasitic capacitor of diode D C_D	22 p	F

4.3.2 Simulation Results of the Control Strategy

i. Implementation of Valley Turn-on

Figure 4.12 shows the waveforms of the *PWM* drive signals, drain-source voltage U_Q of MOSFET Q , transformer primary current I_p , and secondary current I_s at a certain moment. It annotates the four time variables t_{cross} , t_{off} , t_r and t_{on} mentioned in section 3.5.2.

At this time, the transformer primary current oscillates and generates a turn-on signal for MOSFET Q at the third valley bottom, achieving valley turn-on. The switching period of Q is 10.78 μs .

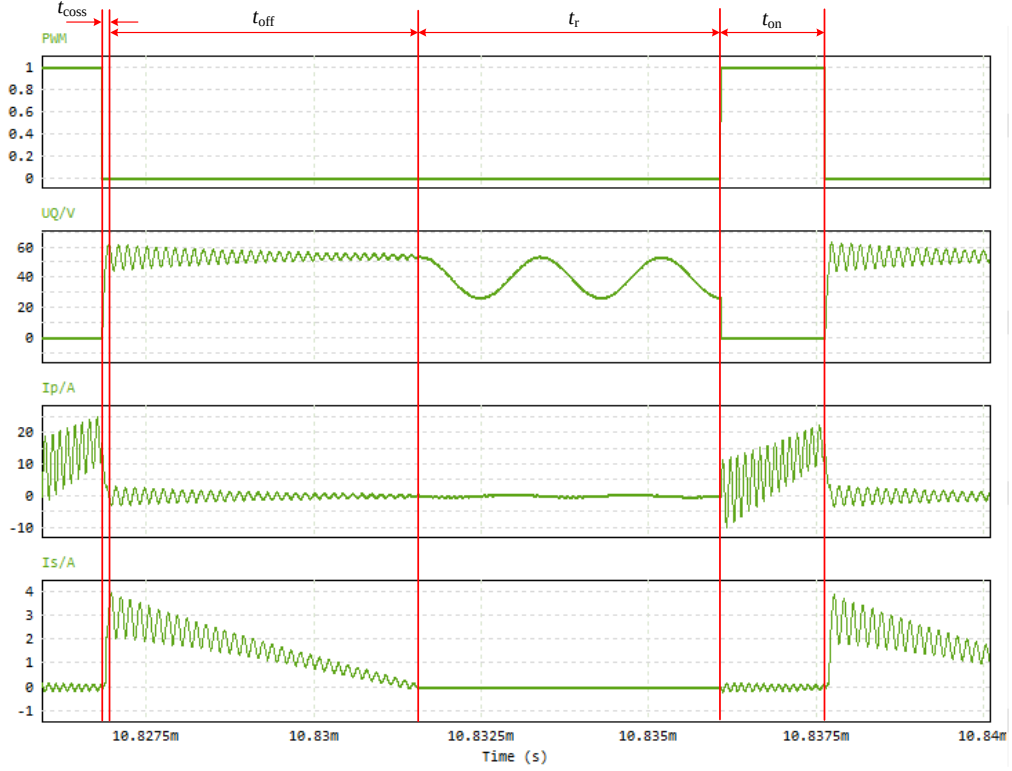
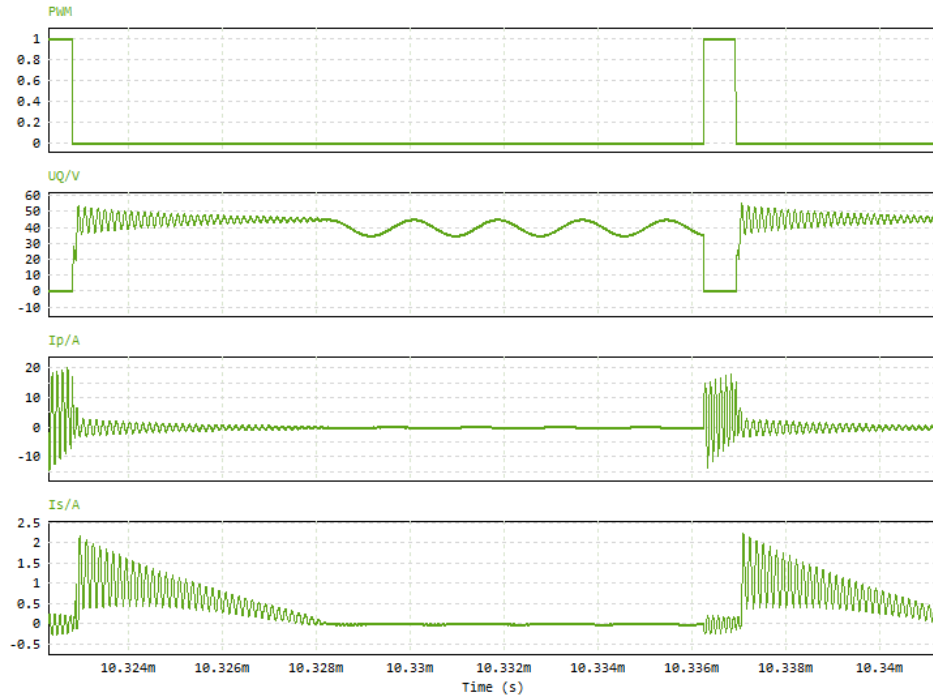


Figure 4.12: Waveforms of the Transistor Voltage and Transformer Current

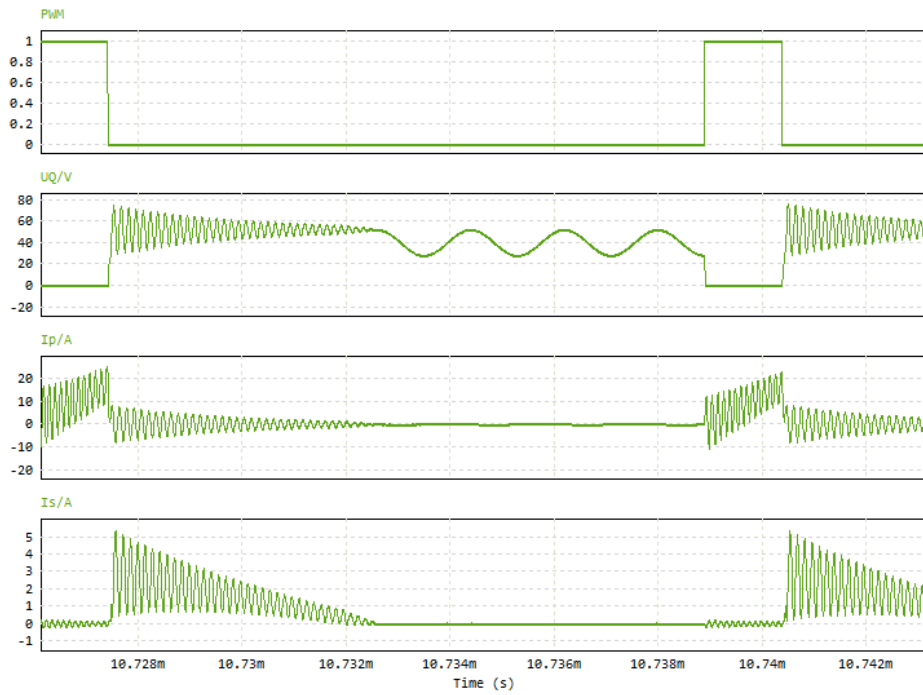
Figure 4.13 provides waveforms of the MOSFET Q voltage and transformer current under four different phase conditions. The multi-valley turn-on control strategy achieves valley turn-on in all cases.

With increasing phase angle, Figure 4.13 (a), (b), (c), and (d) represent the transistor turn-on signals generated at the fifth, fourth, second, and first valleys of the oscillation, with switch periods of 14.72 μs , 13.01 μs , 8.95 μs , and 6.67 μs , respectively. Where, the turn-on

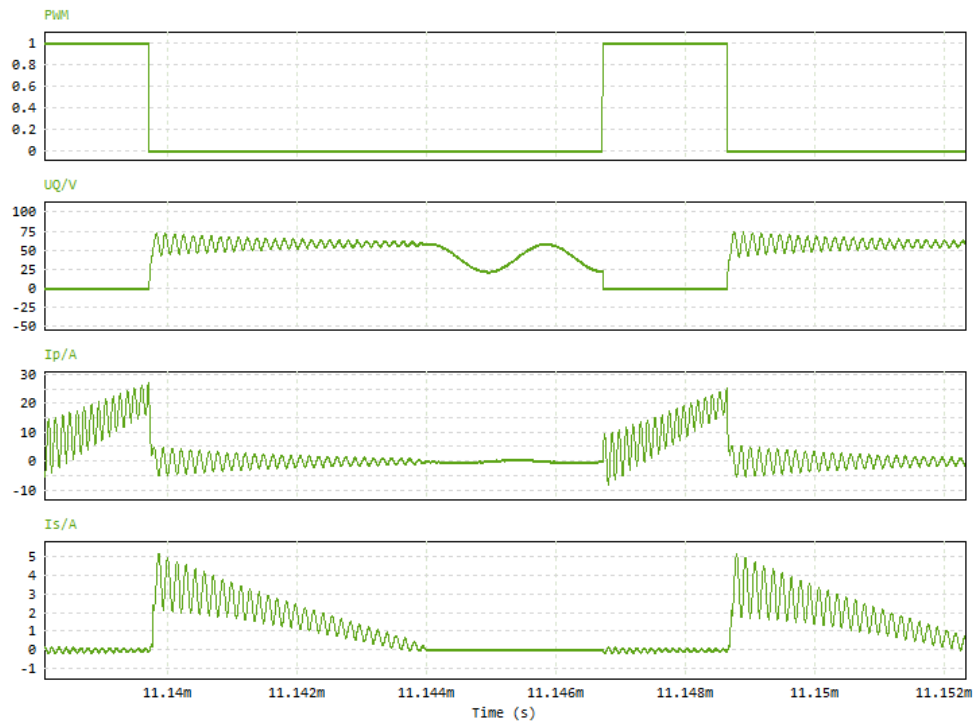
time of MOSFET is $0.76\mu\text{s}$, $1.53\mu\text{s}$, $1.97\mu\text{s}$, $2.07\mu\text{s}$, respectively. The peak current changes with the variation in the phase angle.



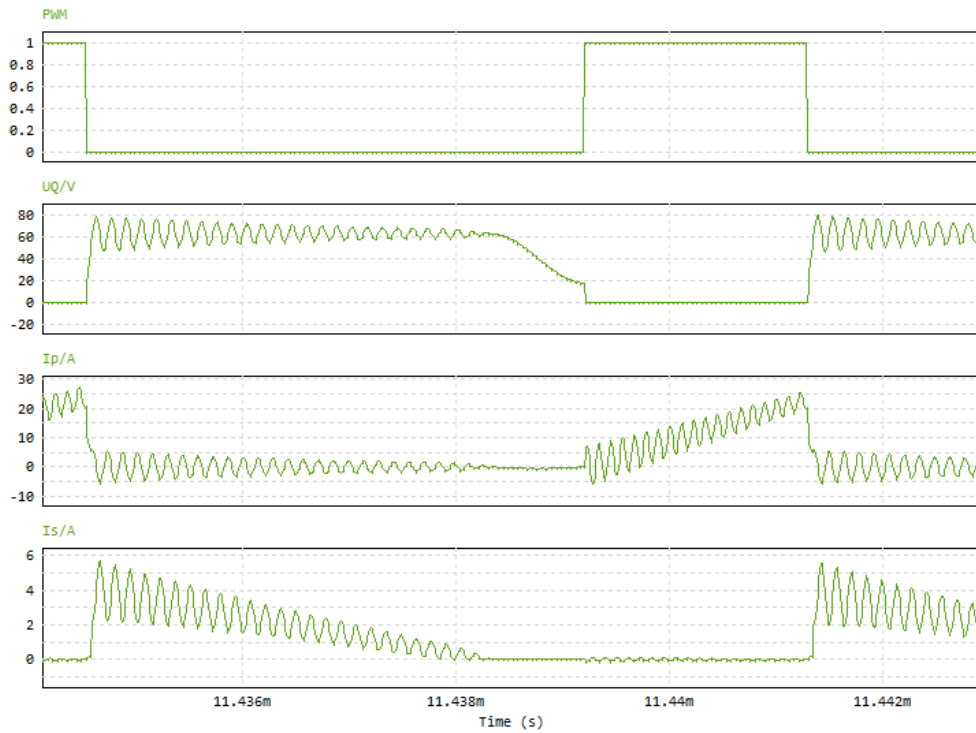
(a) Phase 1



(b) Phase 2



(c) Phase 3



(d) Phase 4

Figure 4.13: Waveforms of the Transistor Voltage and Transformer Current at Different Phases

The multi-valley turn-on control strategy proposed in this paper can accurately calculate the reference current curve, thereby controlling the turn-on and turn-off signals of the transistor in real time to achieve valley turn-on, reduce energy impact during turn-on. Overall, it reduces switching losses and thermal losses, thereby improving the operating efficiency and reliability of the microinverter.

ii. Efficiency Comparison

When using the fixed frequency control strategy, the operating temperature of the MOSFET in the microinverter reaches 186 °C after running for one hour, resulting in significant thermal losses. In contrast, with the multi-valley turn-on strategy, the MOSFET's operating temperature stabilized around 97 °C, greatly reducing thermal losses. The multi-valley turn-on control strategy addresses the issues of high switching and thermal losses, leading to a substantial increase in the operating efficiency of the microinverter. Figure 4.14 compares the efficiency between the multi-valley turn-on control strategy and the fixed-frequency control method from Hasnain et al. (2023), showing that the inverter achieved a maximum efficiency of 97.49% based on the multi-valley turn-on control strategy.

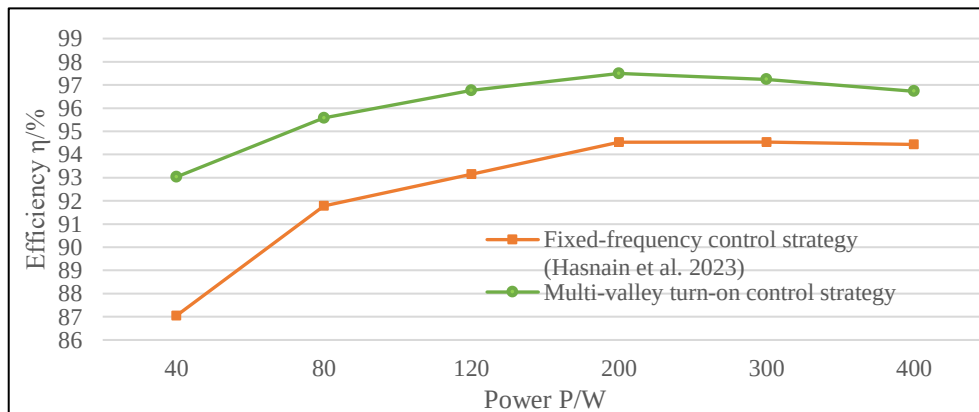
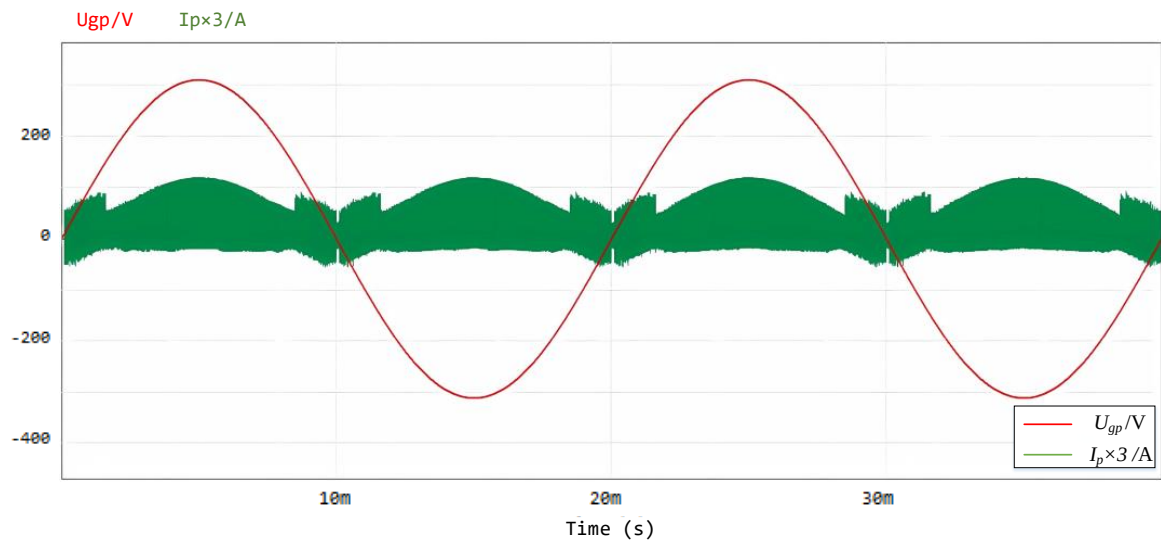


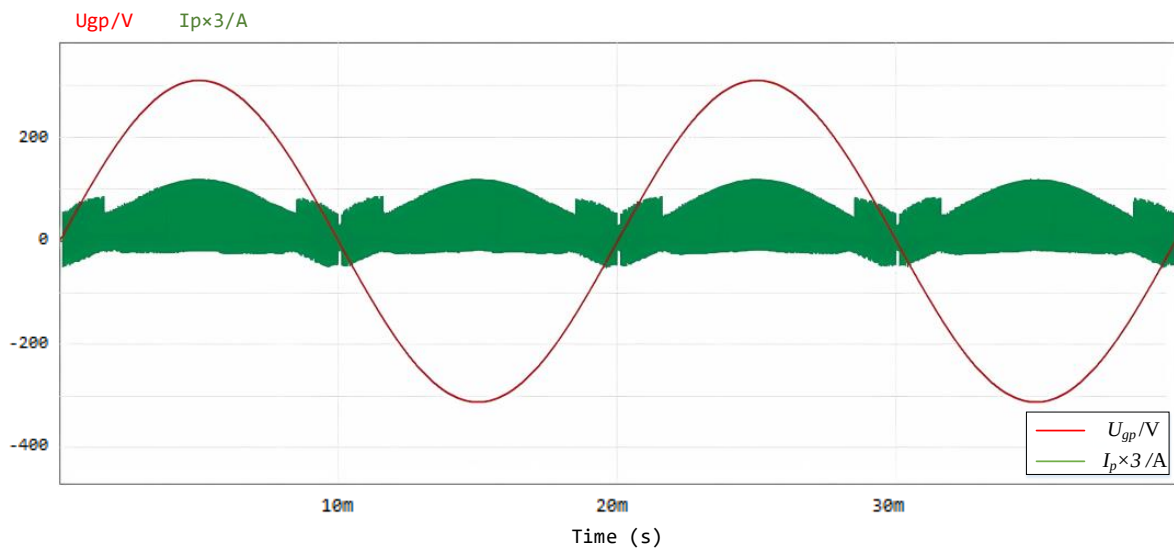
Figure 4.14: Efficiency Curves of the Two Strategies

iii. Comparison of THD values

Figure 4.15(a) shows the voltage and current waveforms of the fixed-frequency control strategy. Figure 4.15(b) shows the voltage and current waveforms of the proposed multi-valley turn-on control strategy.



(a) Fixed-Frequency Control Strategy



(b) Multi-Valley Turn-on Control Strategy

Figure 4.15: Voltage and Current Waveforms of Two Strategies

Because the primary current I_p of the transformer is much smaller than the grid voltage, for comparison convenience, I_p is amplified three times. When the grid phase is low, the envelope of the primary current using the control strategy proposed in this thesis is smoother, resulting in a smaller energy impact, and it effectively reduces the overall harmonic content of the microinverter.

Figure 4.16 shows the curve of the THD value of the grid-connected current with the change in input current under two control strategies when the photovoltaic module input voltage is 30 V. The multi-valley turn-on control strategy can effectively reduce the harmonic content, and the THD is controlled between 2.22% and 2.59%.

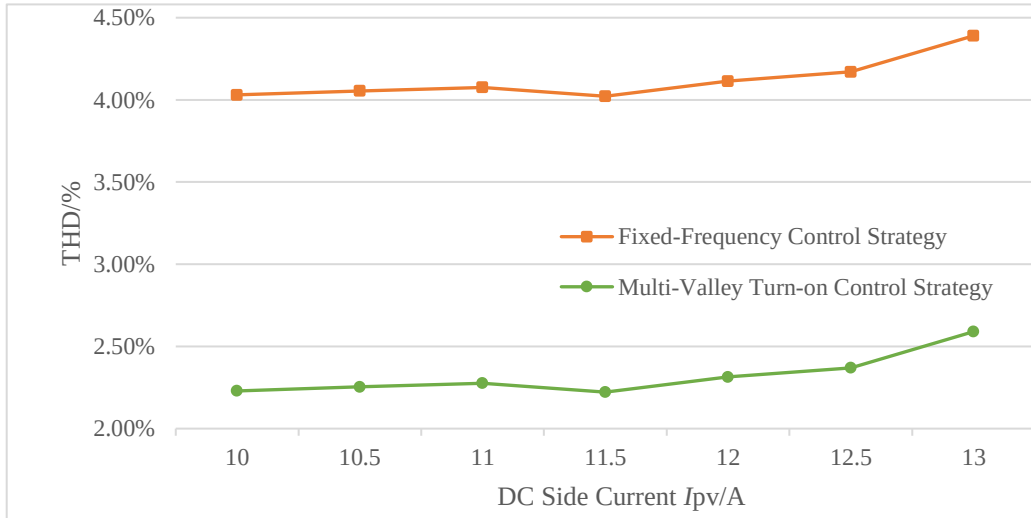


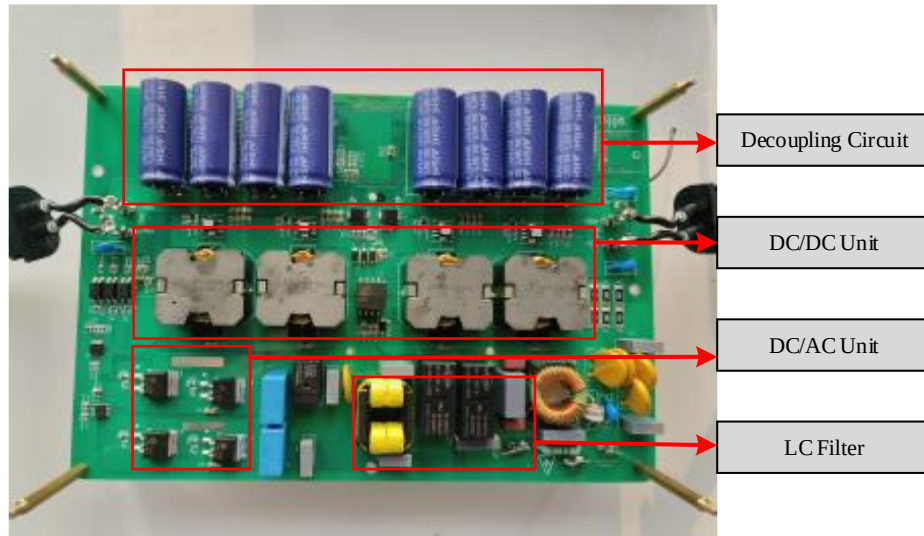
Figure 4.16: THD Values of the Two Strategies

4.4 Microinverter Experimental Platform

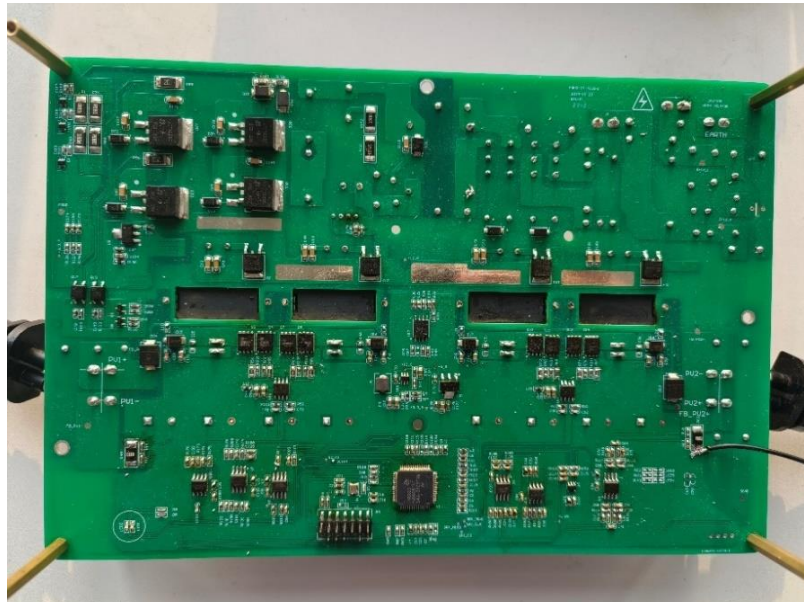
According to the system designed in Section 3.6, this section presents the final experimental prototype and platform established to experimentally verify the improved topology and novel control strategy.

4.4.1 Construction of the Experimental Prototype

As shown in Figure 4.17, a two-stage photovoltaic grid-connected microinverter experimental prototype with a power of 400 W and an output voltage of 220 V was constructed by this research team.



(a) Prototype Front



(b) Prototype Back

Figure 4.17: Microinverter Prototype

The front stage employs a passive clamping flyback circuit to achieve the boost and MPPT algorithm. The rear stage utilizes a full-bridge inverter circuit with the PLL algorithm for inversion, followed by a CL filter. The experimental parameters are consistent with the simulation settings, as shown as Table 3.2. The microinverter control chip uses a 32-bit Microprogrammed Control Unit (MCU) produced by the TI Company, with the model number TMS320F28035PNS, which has powerful floating-point computation capability, multichannel PWM control and can easily implement the control strategy proposed in this research.

Regarding the dimensions, the prototype PCB measures 232.9 mm by 162.5 mm. Including the casing and connection wires, the overall dimensions are 263.1 mm by 219.5 mm by 32.5 mm. It is mounted on the back of a photovoltaic panel measuring 1757 mm by 1134 mm, making the size very suitable.

4.4.2 Construction of the Experimental Platform

The experimental platform is shown in Figure 4.18. In addition to the microinverter prototype constructed in this research, the experimental platform also includes several other equipments, fully meeting all experimental requirements. The experimental equipment includes:

- i. The power analyser is primarily used to measure the input and output power of the inverter, allowing for further calculation of operating efficiency. Additionally, it analyses

power quality, detecting and assessing issues such as voltage fluctuations, current harmonics, and energy losses in the grid, providing specific THD values.

ii. The thermocouple is used to measure the temperature of components, and in this thesis, it is primarily utilized to monitor the temperature of the MOSFETs. When the switching frequency of the MOSFET is too high or the voltage spikes are too large, it can lead to elevated temperatures and significant switching losses. Using the thermocouple to monitor the temperature provides effective protection and oversight.

iii. The oscilloscope is used to observe signal waveforms, including voltage and current, while measuring signal parameters. It can also detect signal quality and output specific THD values.

iv. The PV simulators can simulate various lighting conditions and grid environments, serving as the input for the DC/DC flyback unit in this research, replacing actual PV modules. Since the developed experimental prototype is a one-to-two type microinverter, this experimental platform includes two PV simulators.

v. The heat gun and soldering iron are used for soldering and removing components on the PCB of the experimental prototype.

vi. The power grid simulator serves as the output for the DC/AC inverter unit, simulating parameters such as voltage, current, and frequency of the actual grid, helping to test the performance of the experimental prototype under different grid conditions.

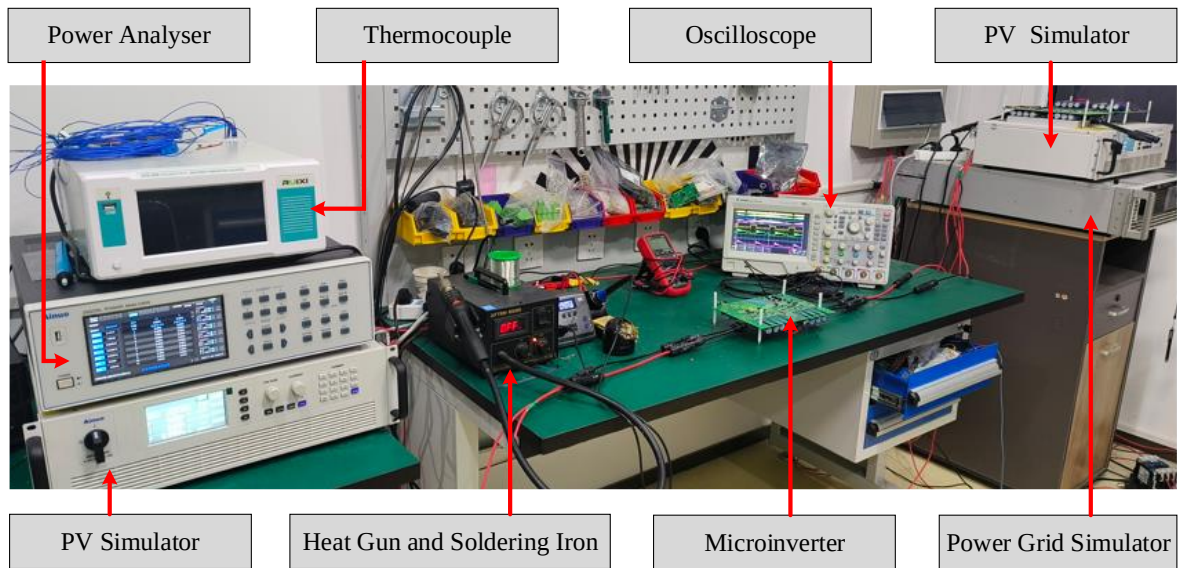


Figure 4.18: Experimental Platform

4.4.3 Experimental Results and Analysis

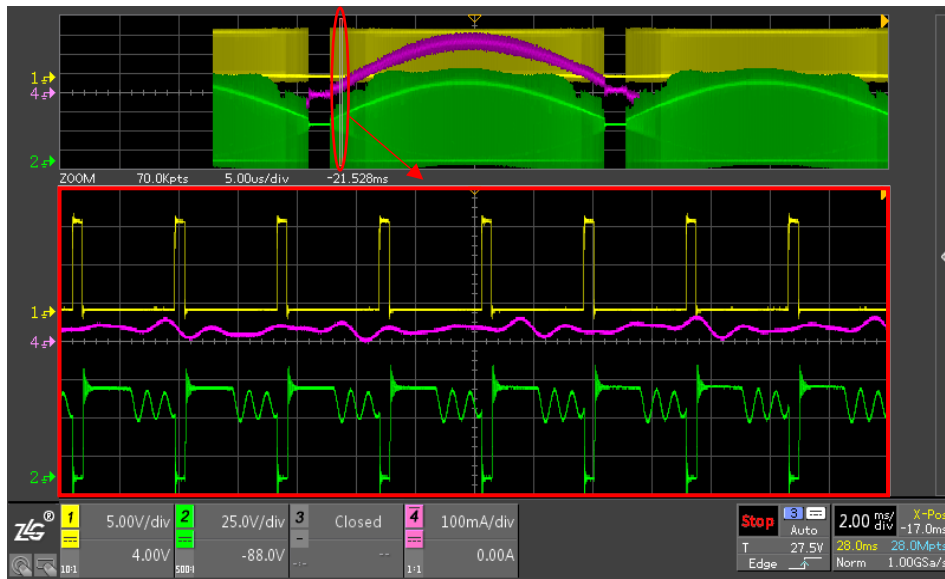
4.4.3.1 Implementation and Comparison of Control Strategies

In this section, the experimental results of the newly proposed control strategy are compared to those of the fixed-frequency turn-on control strategy.

The testing conditions for the two control strategies are essentially the same. The input voltage is controlled by a PV simulator, ranging from 25 V to 55 V, and the load is the power grid simulator. The testing temperature is normal room temperature, and the testing time is continuous operation to evaluate the stability and efficiency of the control strategies. The only difference lies in the MOSFET operating frequency: the fixed-frequency turn-on control strategy maintains a MOSFET operating frequency of 120 kHz, while the multi-valley turn-on control strategy adjusts the frequency based on the switching frequency and valley conditions, ranging from 80 kHz to 300 kHz. Next, the simulation results of the two control strategies are analysed one by one.

i. Fixed-frequency turn-on control strategy

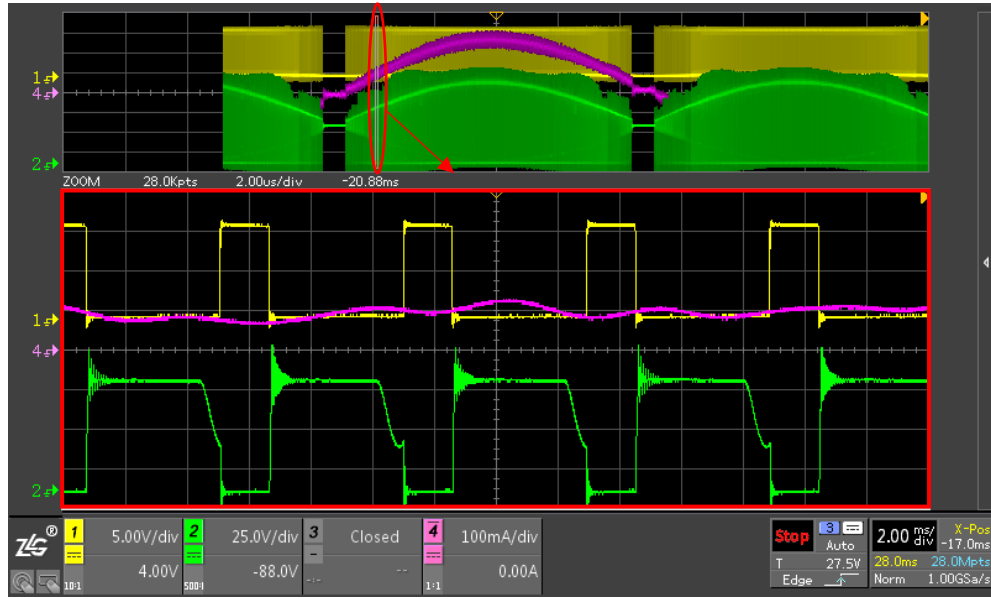
Figure 4.19 presents the waveforms of the main MOSFET Q_1 in the DCM based on a fixed-frequency turn-on control strategy with different grid phase angles, where CH1 is the driving signal PWM1 of Q_1 , CH2 is the drain-source voltage U_{Q1} of Q_1 , and CH4 is the grid-connected current I_{gp} .



(a) Phase 1



(b) Phase 2



(c) Phase 3

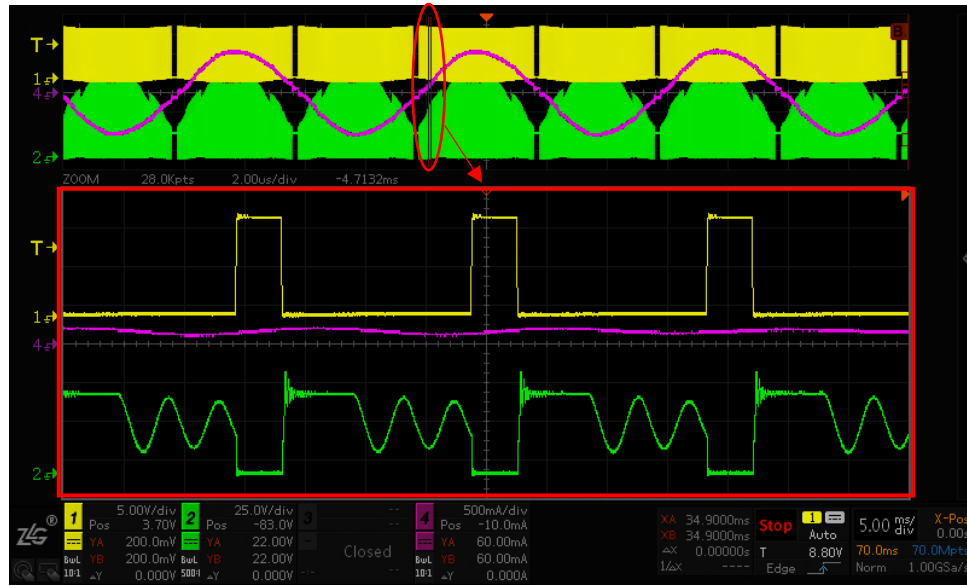
Figure 4.19: MOSFET Q Waveforms of the Fixed-Frequency Control Strategy

The fixed-frequency turn-on strategy cannot achieve valley turn-on for the MOSFET, resulting in the MOSFET bearing relatively large voltage stress at the moment of turn-on, causing component loss and a decrease in system efficiency.

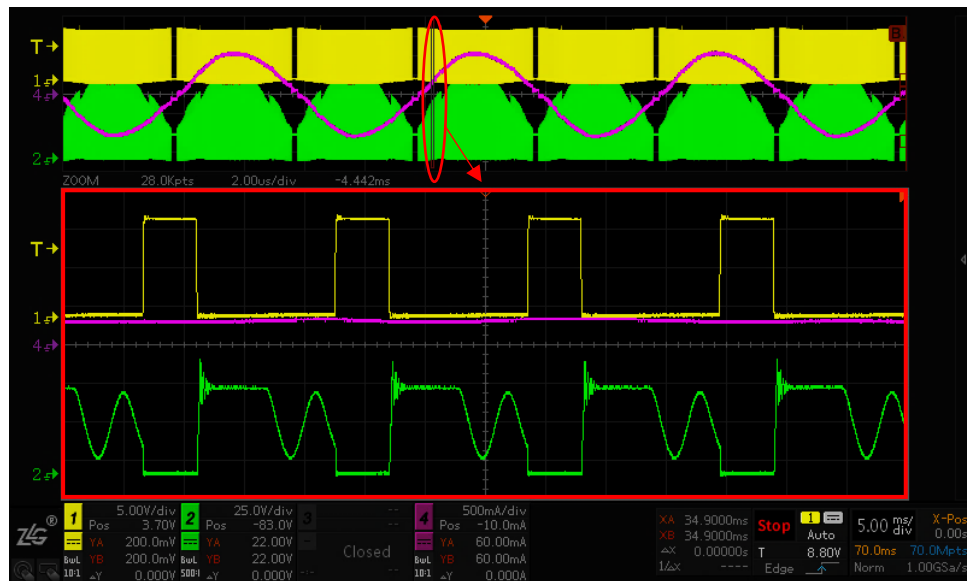
ii. Multi-valley turn-on control strategy

Figure 4.20 provides detailed waveforms of key signals in the DCM based on the multi-valley turn-on control strategy with different grid phase angles. Similarly, CH1 is the driving signal PWM1 of MOSFET Q_1 , CH2 is the drain-source voltage U_{Q1} of Q_1 , and CH4 is the grid-connected current I_{gp} . The MOSFET achieves multi-valley turn-on at each grid phase, effectively reducing the turn-on losses and heat losses of the MOSFET as much as possible, thereby improving the efficiency.

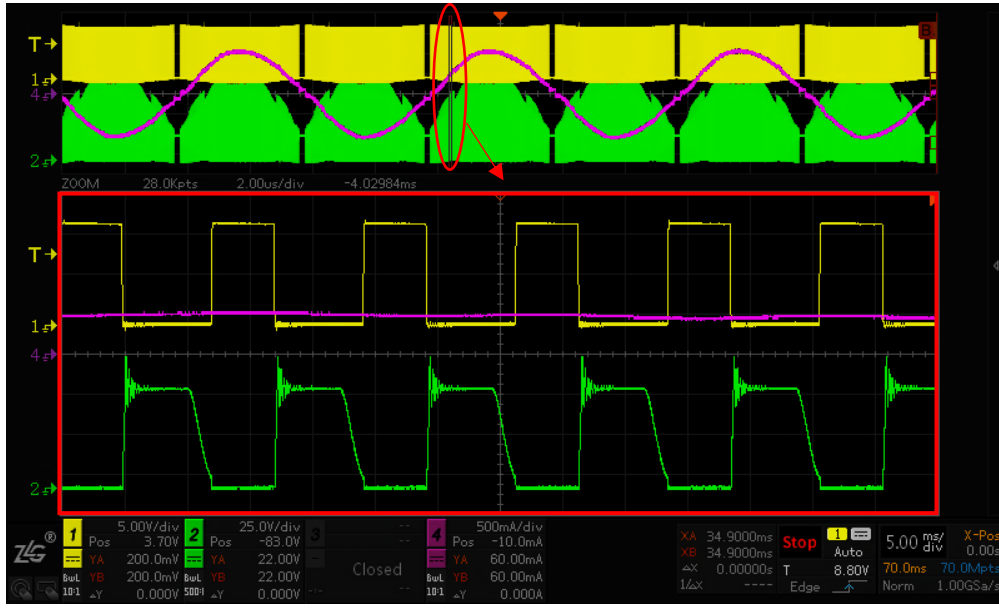
Another research by Lang et al. (2020) proposed an optimizing method based on a variable turn-off time in the DCM. However, this method requires additional comparator hardware to limit the peak inductance current, which increases the cost and volume of the inverter.



(a) Phase 1



(b) Phase 2



(c) Phase 3

Figure 4.20: Key Signal Waveforms of Multi-Valley Turn-on Control Strategy

4.4.3.2 Implementation of the DC–DC Flyback Circuit

Figure 4.21 shows the waveforms of the driving signals and primary currents. CH1 is the driving signal $PWM1$ of the main flyback circuit, CH2 is the driving signal $PWM2$ of the auxiliary flyback circuit, CH3 is the primary current of I_{p1} of the main flyback circuit, and CH4 is the primary current of I_{p2} of the auxiliary flyback circuit. The driving signals of the main flyback circuit and auxiliary flyback circuit have a phase angle difference of 180° , which reduces the current ripple. In the case of a low AC voltage, considering loss issues, it is unnecessary for both circuits to work simultaneously. Therefore, the main flyback circuit operates with full-phase wave emission, while the auxiliary flyback circuit starts operating only after reaching the programmed 90 W power level, effectively improving the operational efficiency.

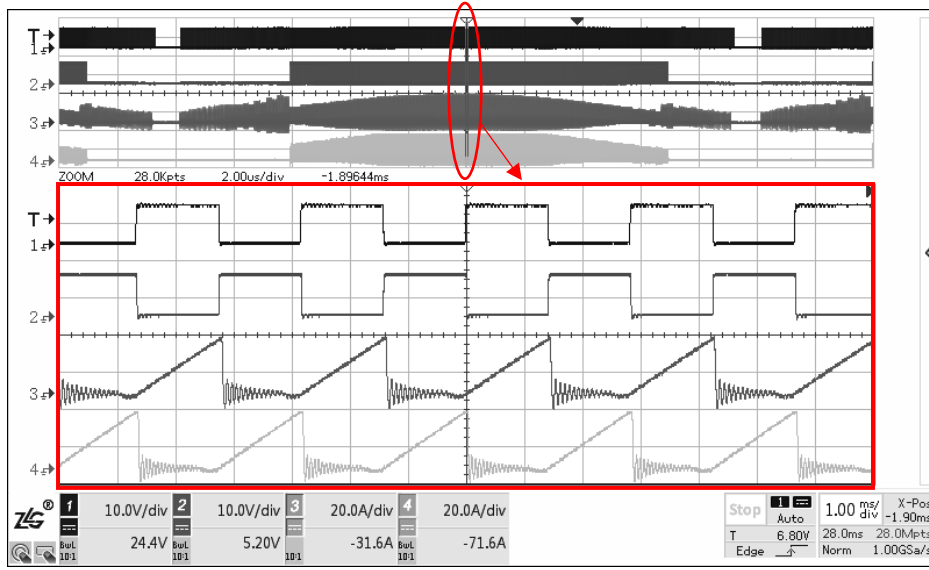


Figure 4.21: Waveforms of the Driving Signals and Primary Currents

4.4.3.3 Implementation of the DC–AC inverter circuit

Figure 4.22 shows the grid voltage and grid-connected current waveforms corresponding to the primary currents. CH1 is the primary current of I_{p1} of the main flyback circuit, CH2 is the primary current of I_{p2} of the auxiliary flyback circuit, CH3 is the grid voltage U_{gp} , and CH4 is the grid-connected current I_{gp} . The experimental waveforms completely match the simulated waveforms. The grid-connected current I_{gp} is in phase and frequency with the grid voltage U_{gp} , and the waveform I_{gp} is of high quality, with the output power factor basically reaching 1, achieving good inverter output performance.

Simultaneously, Figure 4.22 shows the THD of the grid-connected current as 2.67%, which meets the international requirement for harmonic content of grid-connected current (the international standard is below 5%), thus indicating that the proposed interleaved parallel passive clamping flyback topology can effectively control harmonic content and ensure undistorted grid-connected current.

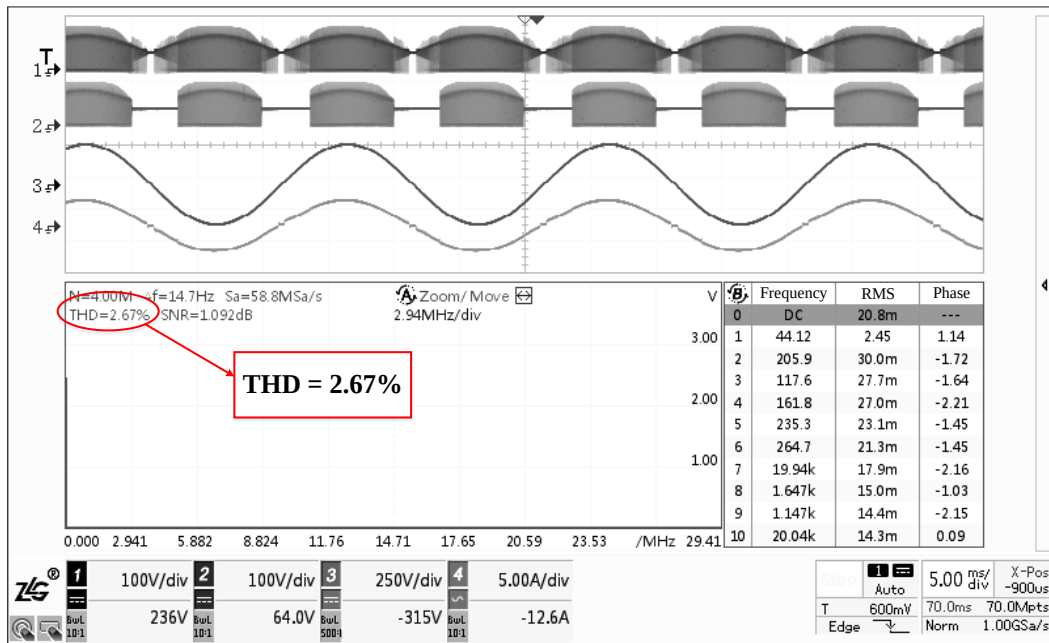


Figure 4.22: Waveforms of the Grid Voltage and Grid-Connected Current

Using a power analyser, the efficiency curve of the microinverter prototype was measured, as shown in Figure 4.23, where P_0 is the output power and η is the efficiency.

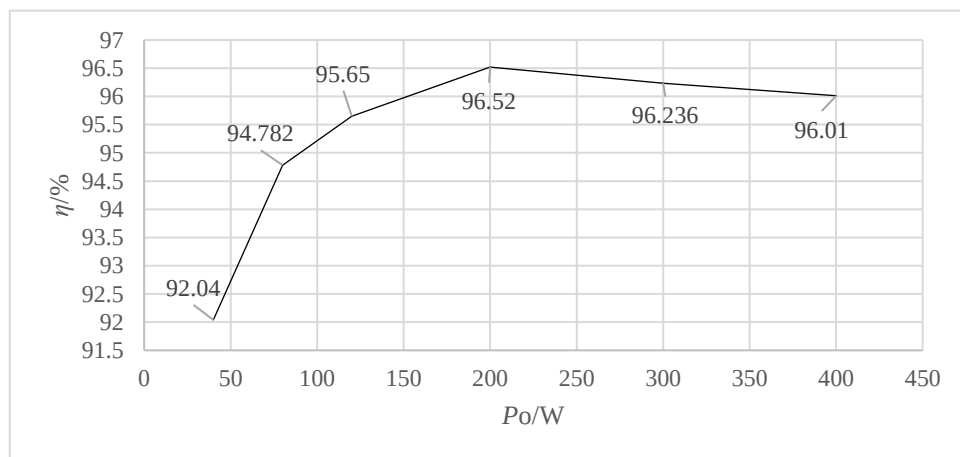


Figure 4.23: Power Curve

This further demonstrates that the microinverter achieves high efficiency throughout the entire load range, with a maximum efficiency of 96.01% at full load, verifying the effectiveness of the control strategy and the superiority of this topology in terms of efficiency.

Table 4.3 provides the performance metrics of the topologies and control strategies mentioned in other literature under full load conditions. Through comparative analysis, the superiority of the topology and control strategy proposed in this research in terms of improving efficiency and reducing harmonic content can be verified.

Table 4.3: Comparison of Different Literature Studies

Literature	Topology Structure	Control Strategy	Efficiency	THD
Yaqoob et al. (2021)	Flyback topology with a center-tapped high-frequency transformer	BCM control strategy suitable for medium and small power-level inverters	/	2.9%
Ma (2020)	RCD passive clamping flyback topology	DCM with fixed turn-off time for inductance current	93.2%	2.5%
Fantino et al. (2022)	Three-phase interleaved DC/DC converter	Bidirectional DCM constant on-time variable-frequency control strategy	96.7%	/
Zhang et al. (2018)	Conventional two-stage microinverter consists of a boost stage and an inverter stage	Variable turn-off time control method	95.4%	/
Christidis et al. (2021)	Flyback topology with a center-tapped high-frequency transformer	Hybrid DBCM operation	92.1%	/
Lang et al. (2020)	Full-bridge inverter topology	Variable turn-off time method in DCM	95.7%	3.6%
This research	Interleaved Parallel Passive Clamping Flyback Topology	Multi--valley turn-on control strategy	96.01%	2.67%

4.5 Summary

This chapter is divided into three parts: topology structure, control strategy, and experimental platform. For the topology structure, the single-ended flyback microinverter topology with compensation capacitors effectively extends the resonance period by 20.27%, and the optimal value of the compensation capacitor is determined. Secondly, adding the passive clamping circuit reduces the peak voltage of the MOSFET by 9.8%. Finally, the interleaved parallel flyback microinverter topology decreases the harmonic content by 0.91% and validates its cost superiority. In terms of the control strategy, the proposed multi-valley turn-on control strategy accurately achieves valley turn-on, reducing voltage stress and circuit losses. Compared to the fixed-frequency control strategy, this strategy improves the operating efficiency and reduces the harmonic content. For the experimental platform, an experimental prototype and platform were constructed. Through experimental comparison, the superiority of the proposed control strategy was verified, and functional experiments involving a DC-DC flyback circuit and a DC-AC inverter circuit were performed. The efficiency and THD were measured using a power analyser, verifying the stability of the microinverter.

CHAPTER 5

CONCLUSIONS AND FUTURE WORK

5.1 Concluding Remarks

This research explores the topology structure and control strategy of interleaved flyback grid-connected microinverters and presents the development and design of a 400 W experimental prototype. The main research contents are as follows:

- i. Building upon the conventional flyback topology, a compensation capacitor was added to effectively extend the resonant period by 10.78%, thereby reducing the switching frequency of the MOSFET. Through repeated experiments, the optimal value for the compensation capacitor was determined. Subsequently, passive clamping technology was introduced to eliminate voltage spikes between the high-frequency transformer leakage inductance and the parasitic capacitor of the MOSFET, resulting in a 9.8% reduction in peak voltage. This helped reduce the switching losses of the MOSFET. Finally, based on the single-ended topology, an interleaved flyback microinverter topology was proposed, resulting in smoother waveforms and a 0.91% reduction in harmonic content. Through comparison, the cost advantage of the proposed interleaved flyback microinverter topology was determined.

- ii. An optimized peak current reference curve calculation method was proposed, utilizing the MPPT algorithm to track the MPP and the SOGI-PLL algorithm to obtain the real-time grid phase angle. Considering the parasitic parameters of various components, the actual peak current reference waveform under practical engineering conditions was accurately calculated to ensure the accuracy of the MOSFET turn-off signal. Additionally, a multi-valley turn-on method was employed to minimize the voltage stress during MOSFET turn-on. Through comparison with waveform outputs by the fixed-frequency control strategy, the proposed control strategy demonstrated superior performance in terms of operating efficiency and THD, with a maximum efficiency of 97.49% and stable THD values between 2.22% and 2.59%.
- iii. The experimental platform system diagram was designed, including hardware circuits such as the main circuit, sampling circuits, and drive circuits, as well as an overall plan for the software process. Based on this, an experimental prototype and platform of the interleaved flyback microinverter for grid connection were constructed. Experimental comparisons validated the effectiveness of the multi-valley turn-on control strategy and achieved DC-DC flyback and DC-AC inverter functions. Finally, measurements showed a maximum efficiency of 96.01% under full load and a THD of 2.67% under grid-connected current, confirming the stability of the proposed topology and the effectiveness of the control strategy.

5.2 Future work

While this thesis presents significant research outcomes towards the improvement of the inverter-based control strategy and topology, a number of directions for further research have been identified as follows:

- i. This research presents a control strategy to improve the efficiency of the flyback microinverter and further enhances the efficiency using passive clamping soft-switching technology, hence increasing the number of components. Achieving higher efficiency without increasing costs is crucial for the promotion of microinverters.
- ii. The microinverter studied in this research can only output active power. To cater to the development trend of future smart grids, microinverters need to have the ability to compensate for reactive power. Due to the different circuit topologies and system structures of conventional centralized inverters, it is necessary to research corresponding reactive power compensation control strategies for microinverters.
- iii. This research focuses on a single microinverter as the research object. However, when considering a microinverter system composed of multiple modules, the issue of injecting total harmonic distortion into the grid needs to be addressed. On the other hand, due to the low output power of a single microinverter, it does not need to operate independently as a voltage source.

Nevertheless, for a microinverter system, the ability to switch to a voltage source mode in the event of grid failure through coordinated operation of the system is of significant importance for the development of microinverters.

- iv. The structure and control strategy of the single-phase microinverter analysed in this thesis can be extended to the three-phase field. However, further research is needed to address key issues such as matching between phase voltages and frequencies, as well as output grid protection.

REFERENCES

- Aamara, F., Zainuri, M. A. A. M., Yusof, Y., Alaas, Z. M., & Ahmed, M. M. R. (2023). Improved damping filter for grid connected solar PV microinverter. *2023 IEEE Industrial Electronics and Applications Conference (IEACon)*, 128–133.
- Achille, E., Martire, T., Glaize, C., & Joubert, C. (2004). Optimized DC-AC boost converters for modular photovoltaic grid-connected generators. *2004 IEEE International Symposium on Industrial Electronics*, 2, 1005–1010.
- Afshari, H., Husev, O., & Vinnikov, D. (2023). A novel isolated buck-boost DC-DC converter with wide range of voltage regulations. *2023 IEEE 17th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG)*, 1–6.
- Ahmed, M. E.-S., Orabi, M., & AbdelRahim, O. M. (2013). Two-stage micro-grid inverter with high-voltage gain for photovoltaic applications. *IET Power Electronics*, 6(9), 1812–1821.
- Aman, M. M., Solangi, K. H., Hossain, M. S., Badarudin, A., Jasmon, G. B., Mokhlis, H., Bakar, A. H. A., & Kazi, S. N. (2015). A review of safety, health and environmental (SHE) issues of solar energy system. *Renewable and Sustainable Energy Reviews*, 41, 1190–1204.
- Andersen, M., & Alvsten, B. (1995). 200 W low cost module integrated utility interface for modular photovoltaic energy systems. *Proceedings of IECON '95 - 21st Annual*

- Conference on IEEE Industrial Electronics, 1*, 572–577.
- Ansari, S. A., Hossein Hosseini, S., & Moghani, J. S. (2017). Low-voltage ride-through capability of flyback inverter under BCM operation for AC module applications. *2017 Smart Grid Conference (SGC)*, 1–6.
- Bhattacharya, A., Paul, A. R., & Chatterjee, K. (2019). A single phase single stage SEPIC-ĆUK based non-isolated high gain and efficient micro-inverter. *2019 IEEE 46th Photovoltaic Specialists Conference (PVSC)*, 0708–0715.
- Bhattar, C. L., & Chaudhari, M. A. (2023). Centralized energy management scheme for grid connected DC microgrid. *IEEE Systems Journal*, 17(3), 3741–3751.
- Bidram, A., Davoudi, A., & Balog, R. S. (2012). Control and circuit techniques to mitigate partial shading effects in photovoltaic arrays. *IEEE Journal of Photovoltaics*, 2(4), 532–546.
- Blahník, V., Peroutka, Z., Žák, J., & Talla, J. (2012). Elimination of dead-time effect causing current distortion of single-phase power converters. *2012 15th International Power Electronics and Motion Control Conference (EPE/PEMC)*, DS1e.3-1-DS1e.3-6.
- Bollipo, R. B., Mikkili, S., & Bonthagorla, P. K. (2021). Hybrid, optimal, intelligent and classical PV MPPT techniques: A review. *CSEE Journal of Power and Energy Systems*, 7(1), 9–33.
- Brindha, R., Ananthichristy, A., Poornima, P., Madhana, M., Rathish, S. A., & Ragavi, S. (2018). Application of interleaved flyback micro inverter in a grid connected system. *Journal of Physics: Conference Series*, 1000(1), 012042.

- Cao, Z., Jamai, A. B., & Li, J. (2023). Modeling and simulation of photovoltaic grid-connected flyback micro inverter. *Journal of Tonghua Normal University*, 44(4), 15–20.
- Çelik, Ö., Teke, A., & Tan, A. (2018). Overview of micro-inverters as a challenging technology in photovoltaic applications. *Renewable and Sustainable Energy Reviews*, 82, 3191–3206.
- Chen, D., Xiao, L., & Hu, W. (2014). A study on a flyback photovoltaic grid-connected microinverter. *Power Electronics*, 48(1), 9–11.
- Chen, Z., Shen, L., & Wu, Y. (2023). An improved interleaved flyback converter with reduced voltage stress and current auto-sharing. *Journal of Electrical Engineering & Technology*, 19(4), 2251-2263.
- Cheng, H.-C., Shen, Y.-H., & Chen, W.-H. (2021). Parasitic extraction and power loss estimation of power devices. *Journal of Mechanics*, 37, 134–148.
- Chiu, H., Lo, Y., Yang, C., Cheng, S., Huang, C.-M., Chuang, C., Kuo, M., Huang, Y., Jean, Y., & Huang, Y. (2013). A module-integrated isolated solar microinverter. *IEEE Transactions on Industrial Electronics*, 60(2), 781–788.
- Christidis, G., Nanakos, A., & Tatakis, E. (2021). Optimal design of a flyback microinverter operating under discontinuous-boundary conduction mode (DBCM). *Energies*, 14(22).
- Cichowski, A., & Nieznanski, J. (2005). Self-tuning dead-time compensation method for voltage-source inverters. *IEEE Power Electronics Letters*, 3(2), 72–75.

- De Souza, K., De Castro, M., & Antunes, F. (2002). A DC/AC converter for single-phase grid-connected photovoltaic systems. *IEEE 2002 28th Annual Conference of the Industrial Electronics Society. IECON 02*, 4, 3268–3273.
- Díaz, M., Muñoz, J., Rivera, M., & Rohten, J. (2023). A comprehensive control strategy for a push–pull microinverter connected to the grid. *Energies*, 16(7), 3196.
- Dwari, S., & Parsa, L. (2011). An efficient high-step-up interleaved DC–DC converter with a common active clamp. *IEEE Transactions on Power Electronics*, 26(1), 66–78.
- Eltawil, M. A., & Zhao, Z. (2013). MPPT techniques for photovoltaic applications. *Renewable and Sustainable Energy Reviews*, 25, 793–813.
- Fantino, R. A., Christian, S. F., & Balda, J. C. (2022). Synchronous-variable-frequency control of bidirectional DCM interleaved DC–DC converter for wide-range enhanced efficiency. *IEEE Transactions on Industrial Electronics*, 69(6), 5844–5853.
- G, Dileep., & Singh, S. N. (2017). Selection of non-isolated DC-DC converters for solar photovoltaic system. *Renewable and Sustainable Energy Reviews*, 76, 1230–1247.
- Gao, M., Chen, M., Zhang, C., & Qian, Z. (2013). Analysis and implementation of an improved flyback inverter for photovoltaic AC module applications. *IEEE Transactions on Power Electronics*, 29(7), 3428–3444.
- Ghavipanjeh Marangalu, M., Vosoughi Kurdkandi, N., & Babaei, E. (2021). Single-source multilevel inverter based on flyback DC-DC converter. *IET Power Electronics*, 14(7), 1237–1255.
- Ghribi, M. E. B., Ternifi, Z. E. T., Bachir, G., & Aillerie, M. (2023). Micro-inverter based

- on symmetrical boost-discharge topology for photovoltaic energy source. *Advances in Electrical and Electronic Engineering*, 21(4), 305–313.
- Giwa, A., Alabi, A., Yusuf, A., & Olukan, T. (2017). A comprehensive review on biomass and solar energy for sustainable energy generation in Nigeria. *Renewable and Sustainable Energy Reviews*, 69, 620–641.
- Goetz, S. M., Wang, C., Li, Z., Murphy, D. L. K., & Peterchev, A. V. (2019). Concept of a distributed photovoltaic multilevel inverter with cascaded double H-bridge topology. *International Journal of Electrical Power & Energy Systems*, 110, 667–678.
- Gong, X., Josifović, I., & Ferreira, J. A. (2013). Modeling and reduction of conducted EMI of inverters with SiC JFETs on insulated metal substrate. *IEEE Transactions on Power Electronics*, 28(7), 3138–3146.
- Gorji, S. A., Sahebi, H. G., Ektesabi, M., & Rad, A. B. (2019). Topologies and control schemes of bidirectional DC–DC power converters: An overview. *IEEE Access*, 7, 117997–118019.
- Guo, Q., Wu, W., Eftychios, K., Chung, H., Blaabjerg, F., & Zhu, L. (2021). A novel non-isolated micro-inverter with active power decoupling. *2021 IEEE 12th Energy Conversion Congress & Exposition - Asia (ECCE-Asia)*, 1999–2004.
- Han, B., Ledwich, G., & Karady, G. (1999). Study on resonant fly-back converter for DC distribution system. *IEEE Transactions on Power Delivery*, 14(3), 1069–1074.
- Hasan, R., Mekhilef, S., Seyedmahmoudian, M., & Horan, B. (2017). Grid-connected isolated PV microinverters: A review. *Renewable and Sustainable Energy Reviews*,

67, 1065–1080.

- Hasnain, A., D’Antonio, M., Singhabahu, C., Shen, Y., Zakzewski, D., & Khaligh, A. (2023). Optimal modulation and DM filter design for a high switching frequency single-stage microinverter. *2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 1483–1488.
- Herrmann, U., Langer, H. G., & van der Broeck, H. (1993). Low cost DC to AC converter for photovoltaic power conversion in residential applications. *Proceedings of IEEE Power Electronics Specialist Conference (PESC)*, 93, 588–594.
- Hsia, T. H., Tsai, H.-Y., Chen, D., Lee, M., & Huang, C. S. (2011). Interleaved active-clamping converter with ZVS/ZCS features. *IEEE Transactions on Power Electronics*, 26(1), 29–37.
- Hu, X., Wang, H., Xu, H., Yu, Z., Lin, X., & Wang, L. (2023). A single-phase non-isolated integrated step-up photovoltaic inverter. *Proceedings of the CSEE*, 43(16), 6429–6440.
- Huang, C., Kawajiri, T., & Ishikuro, H. (2016). A near-optimum 13.56 MHz CMOS active rectifier with circuit-delay real-time calibrations for high-current biomedical implants. *IEEE Journal of Solid-State Circuits*, 51(8), 1797–1809.
- Huang, Y., Cao, Z., & Chen, H. (2023). A control method for photovoltaic grid-connected flyback microinverter. China. Pat. ZL 2023 1 1426623.0.
- Huber, L., Jovanović, M. M., Song, H., Xu, D., Zhang, A., & Chang, C.-C. (2018). Flyback converter with hybrid clamp. *2018 IEEE Applied Power Electronics Conference and*

Exposition (APEC), 2098–2103.

- Jaber, S., & Shakir, A. (2021). Design and Simulation of a Boost-Microinverter for Optimized Photovoltaic System Performance. *Int. J. SMART GRID (ijSmartGrid)*, 5(2), 94-102.
- Jamatia, A., & Sensarma, P. (2023a). A single stage single phase micro-inverter with inherent active power decoupling mechanism for PV-grid system based EV charging station. *2023 IEEE 3rd International Conference on Sustainable Energy and Future Electric Transportation (SEFET)*, 1–6.
- Jamatia, A., & Sensarma, P. (2023b). Flux-balance equation based topology derivation of single phase single-stage transformer-less boost-buck PV micro-inverter family. *2023 IEEE 20th India Council International Conference (INDICON)*, 521–526.
- Ji, X., Wang, J., Ji, B., & Cai, S. (2014). An interleaved parallel flyback quasi single stage photovoltaic grid-connected micro inverter. *Power Electronics*, 48(6), 3.
- Juang, K., Chiang, S., & Xiao, W. (2012). A grid-tied flyback-based PV inverter with BCM variable frequency voltage mode control. *2012 International Symposium on Intelligent Signal Processing and Communications Systems*, 598–603.
- Kasa, N., & Iida, T. (2006). Zero-current transition flyback inverter for small scale wind power generation systems. *2006 India International Conference on Power Electronics*, 34–39.
- Kasa, N., Iida, T., & Bhat, A. (2005). Zero-voltage transition flyback inverter for small scale photovoltaic power system. *2005 IEEE 36th Power Electronics Specialists*

Conference, 2098–2103.

Kaundinya, D. P., Balachandra, P., & Ravindranath, N. H. (2009). Grid-connected versus stand-alone energy systems for decentralized power—A review of literature.

Renewable and Sustainable Energy Reviews, 13(8), 2041–2050.

Kavathekar, G. R., & Patil, M. D. (2020). Interleaved high power improved two-stage flyback inverter for photovoltaic applications. *Journal of Physics: Conference Series*, 1706(1), 012052.

Kim, Y.-H., Ji, Y.-H., Kim, J.-G., Jung, Y.-C., & Won, C.-Y. (2012). A new control strategy for improving weighted efficiency in photovoltaic AC module-type interleaved flyback inverters. *IEEE Transactions on Power Electronics*, 28(6), 2688–2699.

Kjaer, S. B., Pedersen, J. K., & Blaabjerg, F. (2005). A review of single-phase grid-connected inverters for photovoltaic modules. *IEEE Transactions on Industry Applications*, 41(5), 1292–1306.

Kouro, S., Leon, J. I., Vinnikov, D., & Franquelo, L. G. (2015). Grid-connected photovoltaic systems: An overview of recent research and emerging PV converter technology. *IEEE Industrial Electronics Magazine*, 9(1), 47–61.

Lai, L., Su, J., Liu, F., & Hu, A. (2012). Research on control strategy of interleaved flyback for photovoltaic grid-connected inverter. *Electrical & Energy Management Technology*, 9.

Lang, T., Du, S., Yin, H., & Hu, H. (2020). Optimizing method for light-load efficiency of a H-bridge inverter based on variable turn-off time discontinuous current mode.

Transactions of China Electrotechnical Society, 35(22):4761-4770.

- Lee, S.-J., Kang, J.-K., & Sul, S.-K. (1999). A new phase detecting method for power conversion systems considering distorted conditions in power system. *Conference Record of the 1999 IEEE Industry Applications Conference. Thirty-Forth IAS Annual Meeting (Cat. No. 99CH36370)*, 4, 2167–2172.
- Leuenberger, D., & Biela, J. (2012). Comparison of a soft switched TCM T-Type inverter to hard switched inverters for a 3 phase PV grid interface. *2012 15th International Power Electronics and Motion Control Conference (EPE/PEMC)*, LS1d.1-1-LS1d.1-8.
- Li, Q., & Wolfs, P. (2008). A review of the single phase photovoltaic module integrated converter topologies with three different DC link configurations. *IEEE Transactions on Power Electronics*, 23(3), 1320–1333.
- Li, W., & He, X. (2007). An interleaved winding-coupled boost converter with passive lossless clamp circuits. *IEEE Transactions on Power Electronics*, 22(4), 1499–1507.
- Li, Y., & Oruganti, R. (2011). A low cost flyback CCM inverter for AC module application. *IEEE Transactions on Power Electronics*, 27(3), 1295–1303.
- Lin, Z., Pan, S., Chen, Y., Lin, W., Gong, J., & Zha, X. (2024). A dual-input mismatch power processing LLC converter for microinverter application. *IEEE Transactions on Industrial Electronics*, 71(10), 12487–12498.
- Liu, Z., Wang, W.-J., Wei, H.-C., & Liu, C.-L. (2011). A novel ZVS double switch flyback inverter and pulse controlled dimming methods for flat DBD lamp. *IEEE*

- Transactions on Consumer Electronics*, 57(3), 995–1002.
- Lo, Y.-K., Lin, J.-Y., Wang, C.-F., & Lin, C.-Y. (2010). Analysis and design of a dual-mode flyback converter. *2010 IEEE International Conference on Sustainable Energy Technologies (ICSET)*, 1–3.
- Lohner, A., Meyer, T., & Nagel, A. (1996). A new panel-integratable inverter concept for grid-connected photovoltaic systems. *Proceedings of IEEE International Symposium on Industrial Electronics*, 2, 827–831.
- Martins, D. C., & Demonti, R. (2000). Interconnection of a photovoltaic panels array to a single-phase utility line from a static conversion system. *2000 IEEE 31st Annual Power Electronics Specialists Conference. Conference Proceedings (Cat. No.00CH37018)*, 3, 1207–1211.
- Meneses, D., Blaabjerg, F., García, Ó., & Cobos, J. A. (2013). Review and comparison of step-up transformerless topologies for photovoltaic AC-module application. *IEEE Transactions on Power Electronics*, 28(6), 2649–2663.
- Miao, G. (2022). Electrolytic capacitor-free photovoltaic inverter based on fly-back circuit. *Chinese Journal of Electron Devices*, 45(01), 97-101.
- Miao, Z., Tong, H., Jin, X., Yao, W., Lu, Z., & Ma, Z. (2019). DQ-frame zero-crossing effect modeling and current distortion compensation method for Vienna rectifier. *IEEE Transactions on Power Electronics*, 35(7), 7612–7623.
- Ming, X., Kuang, J.-J., Gong, X.-C., Zhang, J., Wang, Z., & Zhang, B. (2023). An NMOS LDO with TM-MOS and dynamic clamp technique handling up to sub-10- μ s short-

- period load transient. *IEEE Journal of Solid-State Circuits*, 59(2), 583-594.
- Moses, M. B., & Banu, J. B. (2015). A new isolated bidirectional full bridge buck-boost converter with LCD clamp circuit. *2015 IEEE Conference on Energy Conversion (CENCON)*, 25–30.
- Myrzik, J. M. A., & Calais, M. (2003). String and module integrated inverters for single-phase grid connected photovoltaic systems-A review. *2003 IEEE Bologna Power Tech Conference Proceedings*, 2, 8.
- Neshaastegaran, P., & Karshenas, H. R. (2013). Investigation of single-stage flyback inverter under different operating modes. *4th Annual International Power Electronics, Drive Systems and Technologies Conference*, 288–293.
- Omar, M. F., Asha'ari, N. L., & Suboh, A. (2023). Comparative study of microinverters topologies and control schemes for photovoltaic applications. *Journal of Social Sciences and Technical Education (JoSSTEd)*, 4(1), 144–158.
- Pan, H., Li, M., Jiang, X., & Qian, W. (2024). Research on hybrid control strategy for waveform stabilization of sin inverter. *Electronic Design Engineering*, 32(6), 16.
- Pashaei, R., Babaei, E., Cecati, C., & Buccella, C. (2017). Analysis of Z-source based DC/DC converter in CCM, DCM and BCM operations. *2017 14th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON)*, 777–780.
- Paul, A. R., Bhattacharya, A., & Chatterjee, K. (2023a). A novel single phase grid connected transformer-less solar micro-inverter topology with power decoupling capability.

IEEE Transactions on Industry Applications, 59(1), 949–958.

- Paul, A. R., Bhattacharya, A., & Chatterjee, K. (2023b). A single-phase grid-connected boost/buck–boost-derived solar PV micro-inverter topology having power decoupling capability. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 11(2), 2340–2349.
- Paul, P., Jose, B. R., K, S. T., Abraham, C., Mathew, J., & J, S. (2023). Push-pull based grid tied microinverter for photovoltaic applications. *2023 IEEE International Conference on Power Electronics, Smart Grid, and Renewable Energy (PESGRE)*, 1–5.
- Premkumar, M., Karthick, K., & Sowmya, R. (2018). A review on solar PV based grid connected microinverter control schemes and topologies. *International Journal of Renewable Energy Development*, 7(2), 171.
- Priewasser, R., Agostinelli, M., Unterrieder, C., Marsili, S., & Huemer, M. (2013). Modeling, control, and implementation of DC–DC converters for variable frequency operation. *IEEE Transactions on Power Electronics*, 29(1), 287–301.
- Qi, H., Chen, W., Chen, W., Cheng, R., Chen, C., & Li, L. (2023). Design of a high frequency DAB-type microinverter for photovoltaic application. *2023 IEEE 2nd International Power Electronics and Application Symposium (PEAS)*, 403–407.
- Qin, S., Cao, T., Chen, F., Gu, Y., Ying, J., Qian, W., Lu, N., Zhang, X., & Yang, G. (2024). Passive clamping driver circuit for suppressing positive and negative gate crosstalk in GaN HEMTs. *Journal of Power Electronics*, 24, 1–11.

- Qureshi, S. A., & Potdar, M. S. (2021). A comparative analysis & simulation of phase locked loop for a grid synchronized photovoltaic system. *2021 IEEE International Conference on Mobile Networks and Wireless Communications (ICMNBC)*, 1–7.
- Ramadhan, G. A. K., Alexzander, M., Setiardi, A. R., Furqani, J., & Rizqiawan, A. (2023). Modified cuk converter-based two-stage microinverter topology design. *2023 4th International Conference on High Voltage Engineering and Power Systems (ICHVEPS)*, 544–549.
- Rezaei, M. A., Lee, K.-J., & Huang, A. Q. (2015). A high-efficiency flyback micro-inverter with a new adaptive snubber for photovoltaic applications. *IEEE Transactions on Power Electronics*, 31(1), 318–327.
- Rojas, D., Muñoz, J., Rivera, M., & Rohten, J. (2021). Review of control techniques in microinverters. *Sensors*, 21(19), 6486.
- Sabi, K., & Costinett, D. (2019). Design and implementation of a bipolar-unipolar switched boundary current mode (BCM) control gan-based single-phase inverter. *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 6473–6480.
- Santos Filho, R. M., Seixas, P. F., Cortizo, P. C., Torres, L. A. B., & Souza, A. F. (2008). Comparison of three single-phase PLL algorithms for UPS applications. *IEEE Transactions on Industrial Electronics*, 55(8), 2923–2932.
- Scholten, D. M., Ertugrul, N., & Soong, W. L. (2013). Micro-inverters in small scale PV systems: A review and future directions. *2013 Australasian Universities Power Engineering Conference (AUPEC)*, 1–6.

- Sen, S., & Ganguly, S. (2017). Opportunities, barriers and issues with renewable energy development—A discussion. *Renewable and Sustainable Energy Reviews*, 69, 1170–1181.
- Shafiullah, M., Ahmed, S. D., & Al-Sulaiman, F. A. (2022). Grid integration challenges and solution strategies for solar PV systems: A review. *IEEE Access*, 10, 52233–52257.
- Sharma, R., & Ball, J. a. R. (2009). Unipolar switched inverter low-frequency harmonics caused by switching delay. *IET Power Electronics*, 2(5), 508–516.
- Shi, L., & Mou, L. (2012). The analysis and comparison in different mode of flyback microinverter for PV module. *Telecom Power Technology*, 29(4), 4.
- Shimizu, T., Wada, K., & Nakamura, N. (2006). Flyback-type single-phase utility interactive inverter with power pulsation decoupling on the DC input for an AC photovoltaic module system. *IEEE Transactions on Power Electronics*, 21(5), 1264–1272.
- Shiroyama, H., Matsuo, H., Ishizuka, Y., & Asako, Y. (2007). Analysis of the noise and efficiency characteristics in a quasi-resonant converter. *IN^{TELE}EC 07-29th International Telecommunications Energy Conference*, 899–903.
- Shu, J., Ma, J., Wang, S., Dong, Y., Liu, T., & He, Z. (2020). A new active thyristor-based DCCB with reliable opening process. *IEEE Transactions on Power Electronics*, 36(4), 3617–3621.
- Smith, K. M., & Smedley, K. M. (1999). Properties and synthesis of passive lossless soft-switching PWM converters. *IEEE Transactions on Power Electronics*, 14(5), 890–899.

- Sutikno, T., Arsadiando, W., Wangsupphaphol, A., Yudhana, A., & Facta, M. (2022). A review of recent advances on hybrid energy storage system for solar photovoltaics power generation. *IEEE Access*, *10*, 42346–42364.
- Tacca, H. E. (1998). Single-switch two-output flyback-forward converter operation. *IEEE Transactions on Power Electronics*, *13*(5), 903–911.
- Taghvae, M. H., Radzi, M. A. M., Moosavain, S. M., Hizam, H., & Hamiruce Marhaban, M. (2013). A current and future study on non-isolated DC–DC converters for photovoltaic applications. *Renewable and Sustainable Energy Reviews*, *17*, 216–227.
- Tan, S., Lin, P., Hu, C., Chen, L., & Xu, D. (2014). Interleaved flyback micro-inverter with SiC MOSFET. *2014 International Power Electronics and Application Conference and Exposition*, 285–290.
- Tang, Y., Zhang, C., Guo, Y., Sun, H., & Jiang, L. (2023). Optimization of zero-crossing distortion for unipolar BCM grid-tied inverter. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, *11*(4), 3680–3691.
- Tang, Z., Yang, Y., & Blaabjerg, F. (2022). Power electronics: The enabling technology for renewable energy integration. *CSEE Journal of Power and Energy Systems*, *8*(1), 39–52.
- Tao, H., Kotsopoulos, A., Duarte, J. L., & Hendrix, M. A. (2008). Transformer-coupled multiport ZVS bidirectional DC–DC converter with wide input range. *IEEE Transactions on Power Electronics*, *23*(2), 771–781.
- Thanikanti, S. B., Yousri, D., Allam, D., Etebia, M., & Balasubramanian, K. (2021).

- Converter/inverter topologies for standalone and grid-connected PV systems. *Renewable Energy and Future Power Systems*, 35–80.
- Tian, F., Chen, F., Rustom, K., & Batarseh, I. (2010). Pulse frequency modulation with soft-switching flyback single-stage inverter. *Intelec 2010*, 1–6.
- Trubitsyn, A., Pierquet, B. J., Hayman, A. K., Gamache, G. E., Sullivan, C. R., & Perreault, D. J. (2010). High-efficiency inverter for photovoltaic applications. *2010 IEEE Energy Conversion Congress and Exposition*, 2803–2810.
- Trujillo, C. L., Santamaría, F., & Gaona, E. E. (2016). Modeling and testing of two-stage grid-connected photovoltaic micro-inverters. *Renewable Energy*, 99, 533–542.
- Wang, C., Xu, S., Lu, S., & Sun, W. (2017). A low-cost constant current control method for DCM and CCM in digitally controlled primary-side regulation flyback converter. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 6(3), 1483–1494.
- Wang, S., Yao, R., & Yuan, X. (2018). Research on single phase SOGI-PLL technology based on photovoltaic grid connection system. *Journal of Hubei University of Technology*, 33(4), 4.
- Watson, R., Lee, F. C., & Hua, G. C. (1996). Utilization of an active-clamp circuit to achieve soft switching in flyback converters. *IEEE Transactions on Power Electronics*, 11(1), 162–169.
- Wei, X., He, Z., Xu, Q., Ma, F., Luo, A., Huang, X., & Wang, F. (2018). Parallel open-circuit fault diagnosis method for cascaded full-bridge NPC inverters with carrier phase

- shifted modulation. *Proceedings of the CSEE*, 38(24), 12.
- Wolfs, P., & Li, Q. (2002). An analysis of a resonant half bridge dual converter operating in continuous and discontinuous modes. *2002 IEEE 33rd Annual IEEE Power Electronics Specialists Conference. Proceedings (Cat. No.02CH37289)*, 3, 1313–1318 vol.3.
- Wu, D., Wu, Y., Kan, J., Tang, Y., Chen, J., & Jiang, L. (2020). Full-bridge current-fed PV microinverter with DLFCR reduction ability. *IEEE Transactions on Power Electronics*, 35(9), 9541–9552.
- Wu, J., & Wang, Q. (2020). A novel passively clamped resonant DC-link inverter. *Proceedings of the CSEE*, 6, 2.
- Xu, J., Qian, H., Hu, Y., Bian, S., & Xie, S. (2021). Overview of SOGI-based single-phase phase-locked loops for grid synchronization under complex grid conditions. *IEEE Access*, 9, 39275–39291.
- Yaqoob, S. J., & Obed, A. A. (2021). An efficient grid-tied flyback micro-inverter with DCM control strategy. *Journal of Techniques*, 3(1), 74-84.
- Yaqoob, S. J., Raham, J. K., & Sadiq, H. A. (2021). Analysis and simulation of current-source flyback inverter with efficient BCM control strategy. *WSEAS Transactions on Electronics*, 12, 132–140.
- Yatsuki, S., Wada, K., Shimizu, T., Takagi, H., & Ito, M. (2001). A novel AC photovoltaic module system based on the impedance-admittance conversion theory. *2001 IEEE 32nd Annual Power Electronics Specialists Conference (IEEE Cat. No.01CH37230)*,

4, 2191–2196.

- Yuan, X., Walder, S., & Oswald, N. (2014). EMI generation characteristics of SiC and Si diodes: Influence of reverse-recovery characteristics. *IEEE Transactions on Power Electronics*, 30(3), 1131–1136.
- Zengin, S., Deveci, F., & Boztepe, M. (2013). Decoupling capacitor selection in DCM flyback PV microinverters considering harmonic distortion. *IEEE Transactions on Power Electronics*, 28(2), 816–825.
- Zhang, B., Zhang, C., Xing, X., Li, X., & Chen, Z. (2021). Novel three-layer discontinuous PWM method for mitigating resonant current and zero-crossing distortion in vienna rectifier with an LCL filter. *IEEE Transactions on Power Electronics*, 36(12), 14478–14490.
- Zhang, C. (2023). Topology and application of microinverter based on novel semiconductors. *Journal of Technology*, 23(2), 95–102.
- Zhang, F., Xie, Y., Hu, Y., Chen, G., & Wang, X. (2019). A hybrid boost–flyback/flyback microinverter for photovoltaic applications. *IEEE Transactions on Industrial Electronics*, 67(1), 308–318.
- Zhang, L., Shi, J., Hu, X., & Luo, D. (2022). A single stage photovoltaic inverter with reactive power compensation and no electrolytic capacitance. *Renewable Energy Resources*, 003, 040.
- Zhang, Y., Li, J., Wang, J., Zhang, Q., Xiong, M., & Chen, Q. (2021). Research on single-stage isolated micro-inverter based on power decoupling. *ELECTRIC DRIVE*, 51(2),

7.

- Zhang, Z., Chen, M., Chen, W., Jiang, C., & Qian, Z. (2014). Analysis and implementation of phase synchronization control strategies for BCM interleaved flyback microinverters. *IEEE Transactions on Power Electronics*, 29(11), 5921–5932.
- Zhang, Z., Zhang, J., & Shao, S. (2018). A variable off-time control method for a single-phase DCM microinverter. *IEEE Transactions on Power Electronics*, 33(8), 7229–7239.
- Zhang, Z., Zhang, J., Shao, S., & Zhang, J. (2019). A high-efficiency single-phase T-type BCM microinverter. *IEEE Transactions on Power Electronics*, 34(1), 984–995.
- Zhang, Z., Zhang, J., & Wu, X. (2016). A single phase T-type inverter operating in boundary conduction mode. *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 1–6.
- Zhao, S., Kheirollahi, R., Wang, Y., Zhang, H., & Lu, F. (2022). Investigation of limitations in passive voltage clamping-based solid-state DC circuit breakers. *IEEE Open Journal of Power Electronics*, 3, 209–221.

APPENDICES

Appendix: Publications

1. **Z. Cao**, A. B. Jamali, A. Yassin, and Y. Huang. (2024). The quasi-resonant structure and control strategy of a photovoltaic flyback grid-connected microinverter. *Electronics (Switzerland)*, 13(10), 1903.
2. **Z. Cao**, A. B. Jamali, A. Yassin, and Y. Huang. (2024). Interleaved parallel passive clamping flyback photovoltaic grid-connected microinverter. *SSRG International Journal of Electrical and Electronics Engineering*, 11(6), 141–149.
3. Y. Huang, **Z. Cao**, H. Chen, & Z. Shen. (2023). An Interleaved Snubber System and Calculation Method for a Flyback Microinverter. China. Pat. ZL 2023 1 1251358.7. **(Chinese Invention Patent, has been granted)**
4. Y. Huang, **Z. Cao**, H. Chen, & Z. Shen. (2023). A Control Method for Photovoltaic Grid-Connected Flyback Microinverter. China. Pat. ZL 2023 1 1426623.0. **(Chinese Invention Patent, has been granted)**